Zilog - Z86D991PZ008SC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d991pz008sc

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The Z8 instruction set, consisting of 43 basic instructions, is optimized for high-code density and reduced execution time. It is similar in form to the ZiLOG Z80 instruction set. The eight instruction types and six addressing modes together with the ability to operate on bits, 4-bit nibbles or binary coded decimal (BCD) digits, 8-bit bytes, and 16-bit words, make for a code-efficient, flexible microcontroller.

Features

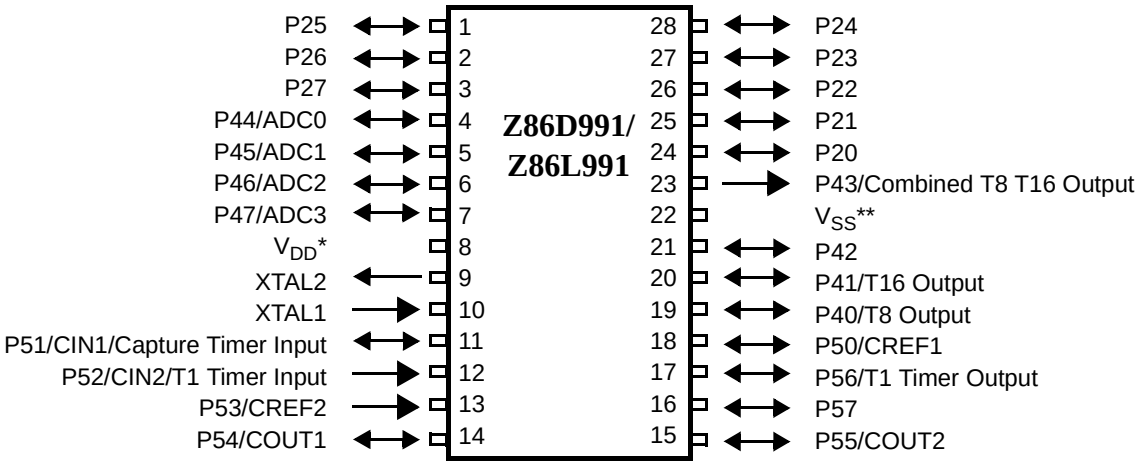
- Four-channel, 8-bit sigma delta analog-to-digital (A/D) converter with external voltage references (not available in the 28-pin configuration)
- Two independent analog comparators
- Controlled current output
- 489 bytes of RAM
  - 233 bytes of general-purpose register-based RAM
  - 256 bytes of RAM mapped into the program memory space that can be used as data RAM or executable RAM
- 32 Kbytes of OTP memory (Z86D99X)
- 16 Kbytes of ROM (Z86L99X)

Counter/Timers

- Special architecture to automate generation and reception of complex pulses or signals:
  - Programmable 8-bit counter/timer (T8) with two 8-bit capture registers and two 8-bit load registers
  - Programmable 16-bit counter/timer (T16) with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- One general-purpose 8-bit counter/timer (T1) with 6-bit prescaler

Input/Output and Interrupts

- Thirty-two I/Os, twenty-nine of which are bidirectional I/Os with programmable resistive pull-up transistors (24 I/Os are available in the 28-pin configuration)
- Sixteen I/Os are selectable as stop-mode recovery sources
- Six interrupt vectors with nine interrupt sources
  - Three external sources
  - Two comparator interrupts



Notes:

1. P43 is a controlled current output.
2. P54, P55, P56, and P57 are high drive outputs.

* $V_{DD} = V_{DD\_CORE} + V_{DD\_padring} + AV_{DD}$

Figure 4. 28-Pin SOIC/DIP Pin Assignment—User Mode

Pins Configuration

Table 2 describes the pins.

Table 2. Pin Descriptions

Symbol	Pin # 28 PDIP/SOIC	40 PDIP	48 SSOP	Direction	Description
P20	24	34	40	I/O	Port 2 Bit 0
P21	25	35	41	I/O	Port 2 Bit 1
P22	26	36	44	I/O	Port 2 Bit 2
P23	27	37	45	I/O	Port 2 Bit 3
P24	28	38	46	I/O	Port 2 Bit 4
P25	1	3	3	I/O	Port 2 Bit 5
P26	2	4	4	I/O	Port 2 Bit 6
P27	3	5	5	I/O	Port 2 Bit 7
P40	19	29	34	I/O	Port 4 Bit 0, T8 Output

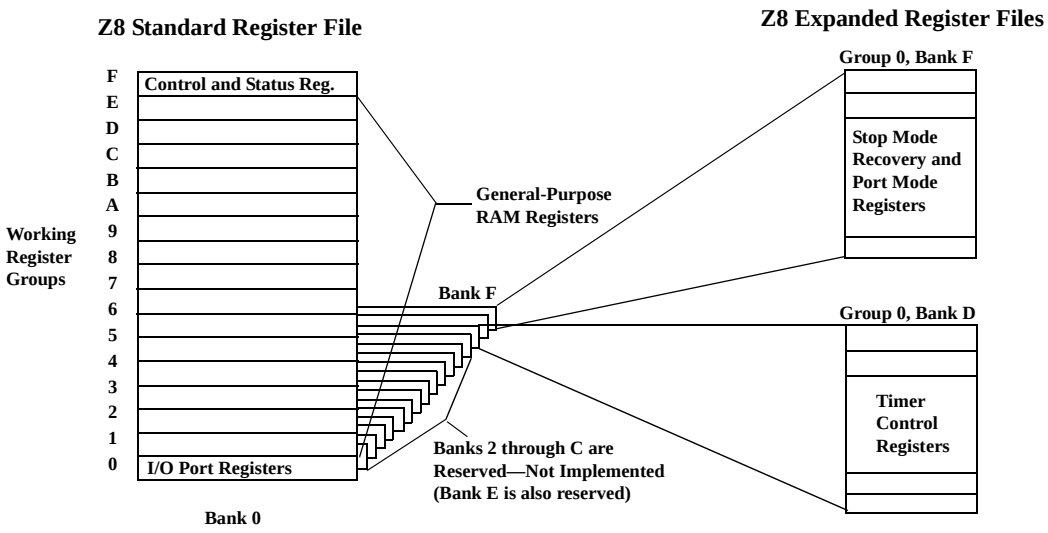


Figure 7. Z8 Expanded Register File Architecture

Clock Circuit Description

The Z8 derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a divide-by-two shaping circuit, and a clock buffer. The oscillator's input is XTAL1, and the oscillator's output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, RC, or an external clock source.

Clock Control

The Z8 offers software control of the internal system clock using programming register bits in the SMR register. This register selects the clock divide value and determines the mode of STOP Mode Recovery.

The default setting is external clock divide-by-two. When bits 1 and 0 of the SMR register are set to 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two.

When bit 1 of the SMR register is set to 1, then SCLK and TCLK equal the external clock frequency. Refer to Table 53 on page 85 for the maximum clock frequency.

A divide-by-16 prescaler of SCLK and TCLK allows the user to selectively reduce device power consumption during normal processor execution (under SCLK control) and/or HALT mode, where TCLK sources counter/timers and interrupt logic. Combining the divide-by-two circuitry with the divide-by-16 prescaler allows the external clock to be divided by 32.

Table 5. Control and Status Register Reset Conditions (Continued)

Register Function	Address Grp/Bnk Register	Symbol	R/W	Reset Value 7	6	5	4	3	2	1	0
Stop Mode Recovery	0Fh r11	SMR	R/W	0	0	1	0	0	0	0	0
Port 2 SMR Source	0Fh r1	P2SMR	R/W	0	0	0	0	0	0	0	0
Port 5 SMR Source	0Fh r5	P5SMR	R/W	0	0	0	0	0	0	0	0

Notes:
†This register is not reset following Stop Mode Recovery (SMR).
*This bit is not reset following SMR.
X means this bit is undefined at POR and is not reset following SMR.
**In OTP, the default for P43 is open-drain output at power up; you need to initialize the P43 data. In the mask part, the P43 output is disabled until it is configured as output.

Power-On Reset

A POR (cold start) always resets the Z8 control and status registers to their default conditions. A POR sets bit 7 of the Stop Mode Recovery register to 0 to indicate that a cold start has occurred.

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset Timer (TPOR) function. The POR time is specified as T_{POR}. T_{POR} time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR delay timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status including recovery from Low Voltage ($V_{LV)}$ Standby mode
- STOP-Mode Recovery (when bit 5 of the SMR register = 1)
- WDT time-out

Under normal operating conditions, a stop mode recovery event always triggers the POR delay timer. This delay is necessary to allow the external oscillator time to stabilize. When using an RC or LC oscillator (with a low Q factor), the shorter wake-up time means the delay can be eliminated.

Bit 5 of the SMR register selects whether the POR timer delay is used after Stop-Mode Recovery or is bypassed. If bit 5 =1, then the POR timer delay is used. If bit 5 = 0, then the POR timer delay is bypassed. In this case, the SMR source must be held in the recovery state for 5 TpC to pass the Reset signal internally.

Watch-Dog Timer (WDT)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. When operating in the RUN modes, a WDT reset is functionally

Mode Registers

Each port has an associated Mode Register that determines the port's functions and allows dynamic change in port functions during program execution. Port and Mode Registers are mapped into the Standard Register File. Because of their close association, Port and Mode Registers are treated like any other general-purpose register. There are no special instructions for port manipulation. Any instruction that addresses a register can address the ports. Data can be directly accessed in the Port Register, with no extra moves.

Input and Output Registers

Each of the four ports (Ports 2, 4, 5, and 6) has an input register, an output register, and associated buffer and control logic. Because there are separate input and output registers associated with each port, writing bits defined as inputs store the data in the output register. This data cannot be read as long as the bits are defined as inputs. However, if the bits are reconfigured as output, the data stored in the output register is reflected on the output pins and can then be read. This mechanism allows the user to initialize the outputs before driving their loads.

Because port inputs are asynchronous to the Z8 internal clock, a READ operation could occur during an input transition. In this case, the logic level might be uncertain (somewhere between a logic 1 and 0).

General Port I/O

The eight I/O lines of each port (except P43, P52, and P53) can be configured under software control to be either input or output, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. See Figure 12.

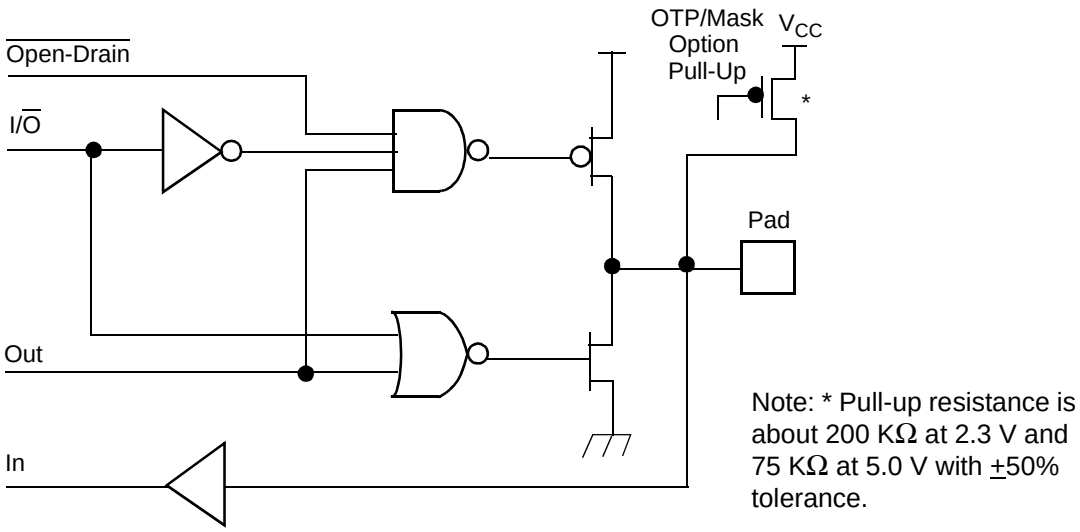


Figure 12. General Input/Output Pin

Read/Write Operations

The ports are accessed as general-purpose registers. Port registers are written by specifying the port register as an instruction's destination register. Writing to a port causes data to be stored in the output register of the port, and reflected externally on any bit configured as an output.

Ports are read by specifying the port register as the source register of an instruction. When an output bit is read, data on the external pin is returned. Under normal loading conditions, returning data on the external pin is equivalent to reading the output register. However, if a bit is defined as an open-drain output, the data returned is the value forced on the output pin by the external system. This value might not be the same as the data in the output register. Reading input bits also returns data on the external pins.

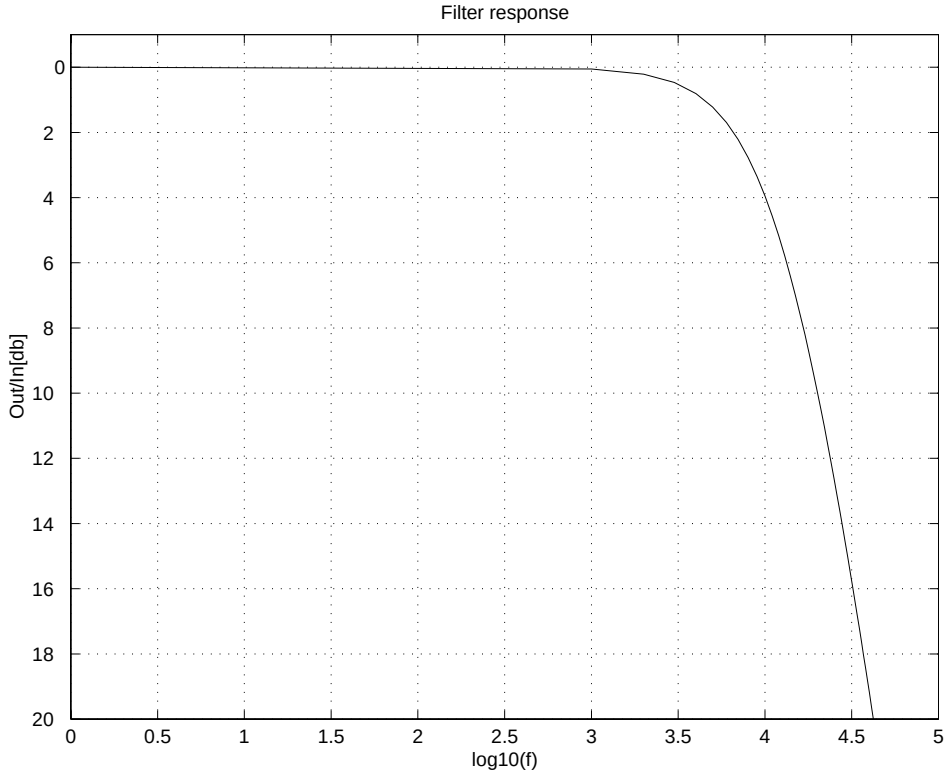


Figure 15. Low-Pass Filter (with 8-MHz Crystal)

The sampling frequency of the modulator f_{ADC} can be selected between f_{SCLK} and $f_{SCLK}/2$ (bit1 from ADCCTRL). Reducing the clock frequency lowers the power dissipated in the ADC block.

The ADC can be enabled or disabled. When enabled, the ΣΔ converter tracks the input voltage. When switching between the channels (step response), the required time to reach the final value is given by the time constant of the low-pass filter:

$$T_{delay} = \frac{2}{f_{3db}} = \frac{2}{0.0021 f_{ADC}} = \frac{952}{f_{ADC}}$$

When available, the reference for the ADC is set externally with the V_{ref+} and V_{ref-} pins. The output code represents the following ratio:

$$D_{out} = \frac{V_{in} - V_{Ref-}}{V_{Ref+} - V_{Ref-}} \times 256$$

Load and Enable Count Bits

Setting the Load bit D_2 to 1 transfers the initial values in the prescaler and the counter/timer registers into their respective down-counters. The next internal clock resets bit D_2 to 0, readying the Load bit for the next load operation. The initial values can be loaded into the down-counters at any time. If the counter/timer is running, the counter/timer continues to run and starts the count over with the initial value. Therefore, the Load bit actually functions as a software re-trigger.

The T_1 counter/timer remains at rest as long as the Enable Count bit D_3 is 0. To enable counting, the Enable Count bit D_3 must be set to 1. Counting actually starts when the Enable Count bit is written by an instruction. The first decrement occurs four internal clock periods after the Enable Count bit has been set.

The Load and Enable Count bits can be set at the same time. For example, using the instruction `OR TMR #%0C` sets both D_2 and D_3 of TMR to 1. The initial values of PRE_1 and T_1 are loaded into their respective counters, and the count is started after the M2T2 machine state after the operand is fetched as shown in Figure 23.

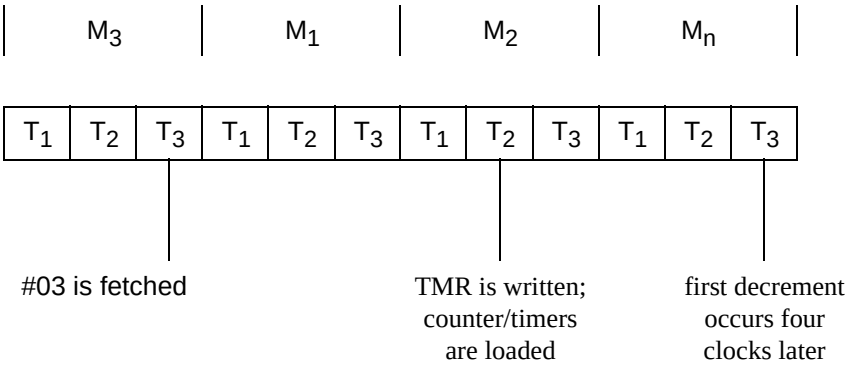


Figure 23. Starting the Count

Prescaler Operations

During counting, the programmed clock source drives the prescaler 6-bit counter. The counter is counted down from the value specified by bits D_2–D_7 of the corresponding prescaler register, PRE_0 or PRE_1 (Figure 24). When the prescaler counter reaches its end-of-count, the initial value is reloaded and counting continues. The prescaler never actually reaches zero. For example, if the prescaler is set to divide by three, the count sequence is as follows:

3-2-1-3-2-1-3-2...

The time interval (i) until end-of-count, is given by

i = t x p x v

where t is 8 divided by XTAL frequency, p is the prescaler value (1 – 64), and v is the counter/timer value (1 – 256). The prescaler and counter/timer are true divide-by-n counters.

T_{OUT} Modes

The Timer Mode register TMR (F1h) (Figure 25) is used in conjunction with the Port 5 Mode register P5M to configure $P5_6$ for T_{OUT} operation. In order for T_{OUT} to function, $P5_6$ must be defined as an output line by setting P5M bit D_6 to 0. Output is controlled by one of the counter/timers (T_0 or T_1) or the internal clock.

R241 TMR
Timer Mode Register
(F1h; Read/Write)

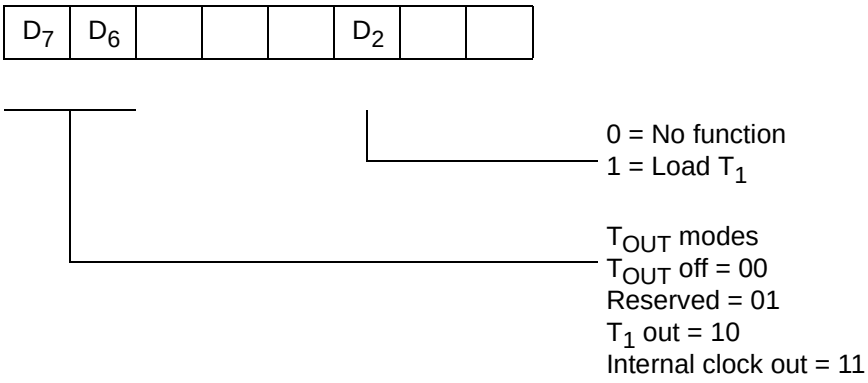


Figure 25. Timer Mode Register T_{OUT} Operation

The $P5_6$ output is selected by TMR bits D_7 and D_6. T_1 is selected by setting D_7 and D_6 to 1 and 0, respectively. The counter/timer T_{OUT} mode is turned off by setting TMR bits D_7 and D_6 both to 0, freeing $P3_6$ to be a data output line.

T_{OUT} is initialized to a logic 1 whenever the TMR Load bit D_2 is set to 1.

At end-of-count, the interrupt request line IRQ_5 clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line $P5_6$. In all cases, when the counter/timer reaches its end-of-count, T_{OUT} toggles to its opposite state (see Figure 26). If, for example, the counter/timer is in continuous counting mode, T_{OUT} has a 50% duty cycle output. You can control the duty cycle by varying the initial values after each end-of-count.

Note: Do not use the same instructions for stopping the counter/timers and setting the status bits. Two successive commands are necessary—the first command for stopping counter/timers and the second command for resetting the status bits—because one counter/timer clock interval must complete for the initiated event to actually occur.

T8 Demodulation Mode

Program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both, depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both, depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If T8 is a positive edge, data is placed in LO8. If T8 is a negative edge, data is placed in H18. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with TC8H and starts counting again. If T8 reaches 0, the time-out status bit (CTR0 D5) is set, and an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 35).

Analog-to-Digital Converter Control Registers

The Z86D99/Z86L99 family features an 8-bit analog-to-digital converter with external voltage references. The output of the ADC is stored in the ADC Data Register, as shown in Table 20. The ADC is configured using the ADC Control Register, as shown in Table 19.

Table 19. ADCCTRL Register (Group/Bank 0Fh, Register 8)

Bit	7	6	5	4	3	2	1	0
Bit/Field	P47_ A/D	P46_ A/D	P45_ A/D	P44_ A/D	Channel Selection		A/D Pwr On	ADC Clock Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	P47_A/D	R/W	1 0	P47 configured as A/D Input P47 configured as digital input
_6_____	P46_A/D	R/W	1 0	P46 configured as A/D Input P46 configured as digital input
__5____	P45_A/D	R/W	1 0	P45 configured as A/D Input P45 configured as digital input
___4___	P44_A/D	R/W	1 0	P44 configured as A/D Input P44 configured as digital input
____32__	Channel Selection	R/W	11 10 01 00	Channel 3 (P47) Channel 2 (P46) Channel 1 (P45) Channel 0 (P44)
_____1_	A/D_PowerON	R/W	1 0	ON OFF
_____0	ADC Clock Select	R/W	1 0	SCLK/2 SCLK

ADC Control Register (ADCCTRL)

The ADCCTRL register controls the operation of the analog-to-digital converter. Bits 2 and 3 of the ADCCTRL register determine which of the four analog input channels feeds into the ADC at any given time. Bits 4 through 7 enable or disable the digital input buffer. When configured as an ADC input channel, the port has to be configured in Input Mode and with the digital input buffer disabled.

Interrupt Request Register

The IRQ, as described in Table 23, is a read/write register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt request is made by any of the six interrupts, the corresponding bit in the IRQ is set to 1.

Table 23. IRQ (Group/Bank 0Fh, Register A)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Interrupt Edge		Set IRQ5	Set IRQ4	Set IRQ3	Set IRQ2	Set IRQ1	Set IRQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	Interrupt Edge Trigger	R/W	11 10 01 00	P51 Rise/FallingP52 Rise/Falling P51 Rising P52 Falling P51 FallingP52 Rising P51 FallingP52 Falling
__5_____	Set IRQ_5	R R W W	1 0 1 0	IRQ_5 Inactive IRQ_5 Active Set IRQ_5 Reset IRQ_5
___4____	Set IRQ_4	R R W W	1 0 1 0	IRQ_4 Inactive IRQ_4 Active Set IRQ_4 Reset IRQ_4
____3___	Set IRQ_3	R R W W	1 0 1 0	IRQ_3 Inactive IRQ_3 Active Set IRQ_3 Reset IRQ_3
_____2__	Set IRQ_2	R R W W	1 0 1 0	IRQ_2 Inactive IRQ_2 Active Set IRQ_2 Reset IRQ_2
______1_	Set IRQ_1	R R W W	1 0 1 0	IRQ_1 Inactive IRQ_1 Active Set IRQ_1 Reset IRQ_1
_______0	Set IRQ_0	R R W W	1 0 1 0	IRQ_0 Inactive IRQ_0 Active Set IRQ_0 Reset IRQ_0

Whenever a power-on reset is executed, the IRQ is reset to 00h and disabled. Before the IRQ accepts requests, it must be enabled by executing an enable interrupts instruction.

Note: IRQ is always cleared to 00h and is in read-only mode until the first EI instruction that enables the IRQ to be read/write. Setting the Global Interrupt Enable bit in the Interrupt Mask Register (IMR bit 7) does not enable the IRQ. Execution of an EI instruction is required.

For polled processing, IRQ must be initialized by an EI instruction. To properly initialize the IRQ, the following code is provided:

```
CLR   IMR   ; make sure vectored interrupts are disabled
EI          ; enable IRQ, otherwise it is read only
            ; not necessary, if interrupts were previously
            ; enabled
DI          ; disable interrupt handling
```

IMR is cleared before the IRQ enabling sequence to ensure no unexpected interrupts occur when EI is executed. This code sequence must be executed before programming the application required values for IPR and IMR.

I/O Port Control Registers

Each of the four ports (Ports 2, 4, 5, and 6) has an input register, an output register, and an associated buffer and control logic. Because there are separate input and output registers associated with each port, writing bits defined as inputs stores the data in the output register. This data cannot be read as long as the bits are defined as inputs. However, if the bits are reconfigured as output, the data stored in the output register is reflected on the output pins and can then be read. This mechanism allows the user to initialize the outputs before driving their loads.

T8 Control Register (CTR0)

As shown in Table 40, the T8 Control Register, known as CTR0, controls the operation of the 8-bit T_8 timer.

Table 40. CTR0 Register (Group/Bank 0Dh, Register 0)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T8_ Enable	Single/ Modulo-n	Time_ Out	T8_Clock		Capture INT_ Mask	Counter INT_ Mask	P40_ Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	T_8 Enable	R	1	Counter Enabled
		R	0	Counter Disabled
		W	1	Enable Counter
		W	0	Stop Counter
_6_____	Single/ Modulo-n	R/W	1	Single Pass
			0	Modulo-n
__5____	Time_Out	R	1	Counter Timeout Occurred
		R	0	No Counter Timeout
		W	1	Reset Flag to 0
		W	0	No Effect
___43___	T_8 Clock	R/W	11	SCLK/8
			10	SCLK/4
			01	SCLK/2
			00	SCLK
_____2__	Capture Interrupt Mask	R/W	1	Enable Data Capture Interrupt
			0	Disable Data Capture Interrupt
______1_	Counter Interrupt Mask	R/W	1	Enable Time_Out Interrupt
			0	Disable Time_Out Interrupt
_______0	P40_Out	R/W	1	P40 configured as T_8 Output
			0	P40 configured as I/O

T8 High Capture Register (HI8)

The T8 High Capture Register, as described in Table 41, holds the captured data from the output of the T_8 counter/timer. This register is typically used to hold the number of counts when the input signal is high (or 1).

Table 41. HI8 Register (Group/Bank 0Dh, Register B)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T8_Capture_HI							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_8 Capture High Value	R W	Data	Captured Data No Effect

T8 Low Capture Register (LO8)

The T8 Low Capture Register, as described in Table 42, holds the captured data from the output of the T_8 counter/timer. This register is typically used to hold the number of counts when the input signal is low (or 0).

Table 42. LO8 Register (Group/Bank 0Dh, Register A)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T8_Capture_LO							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_8 Capture Low Value	R W	Data	Captured Data No Effect

Electrical Characteristics

This section covers the absolute maximum ratings, standard test conditions, DC characteristics, and AC characteristics.

Absolute Maximum Ratings

Table 53 lists the absolute maximum ratings.

Table 53. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C
V_{RAM}	Minimum RAM Voltage	1.0 V**		

Note:
*Voltage on all pins with respect to GND.
†See “Ordering Information” on page 95.
** Estimated value, not tested.

Stresses greater than those listed in the preceding table can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 36).

Table 54. DC Characteristics for the Z86D99X (OTP Only)

Symbol	Parameter	V_{DD}	Min	Max	Units	Comments
V_{DD}	Power Supply Voltage		3	5.5		
V_{CH}	Clock Input High Voltage	3.0 V 5.5 V	0.8Vdd 0.8Vdd	Vdd+0.3 Vdd+0.3	V V	Driven by Ext. clock generator
V_{CL}	Clock Input Low Voltage	3.0 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd		Driven by Ext. clock generator
V_{IH}	Input High Voltage	3.0 V 5.5 V	0.7Vdd 0.7Vdd	Vdd+0.3 Vdd+0.3	V V	
V_{IL}	Input Low Voltage	3.0 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd	V V	
V_{OH1}	Output High Voltage Regular I/O	3.0 V 5.5 V	V_{DD}–0.8 V_{DD}–0.8		V V	–1.2 mA
V_{OH2}	High Drive Pins (P54, P55, P56, P57)	3.0 V 5.5 V	V_{DD}–0.8 V_{DD}–0.8		V V	–5.0 mA
V_{OL1}	Regular I/O Output low voltage	3.0 V 5.5 V		0.4 0.8	V V	2 mA 4.0 mA
V_{OL2}	High Drive Pins (P54, P55, P56, P57)	3.0 V 5.5 V		0.4 0.8	V V	4 mA 7.0 mA
I_{CCO}	Controlled Current Output (P43)	3.0 V 5.5 V	70 70	120 120	mA mA	Vout = 1.2 V to VDD (see Figure 17)
I_{IL}	Input Leakage	3.0 V 5.5 V	–1 –1	1 µA 1 µA	µA µA	Vin=0 V, Vdd Vin=0 V, Vdd
I_{CC}	Supply Current	3.0 V 5.5 V 3.0 V 5.5 V		10 15 250 850	mA mA µA µA	at 8 MHz at 8 MHz at 32 KHz at 32 KHz ADC is off.
I_{CC1}	Standby Current (Halt Mode)	3.0 V 5.5 V 3.0 V 5.5 V		3 5 2 4	mA mA mA mA	Vin=0 V, Vdd at 8 MHz Clock divided by 16 XTAL running ADC is off.
I_{CC2}	Standby Current (STOP Mode)	3.0 V 5.5 V		20 30	µA µA	Vin=0 V, Vdd; ADC is off. P43=1 or high impedance WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.
I_{ADC}	Current with A/D Running	3.0 V 5.5 V		500 900	µA µA	
V_{LV}	Vdd Low-Voltage Protection			2.90	V	Low voltage protection is also known as brownout. Typical is 2.6 V.
V_{LB}	Low-Battery Detection			VLV+ 0.5	V V	

Analog-to-Digital Converter Characteristics

Table 56 lists the analog-to-digital converter characteristics.

Table 56. Analog-to-Digital Converter Characteristics

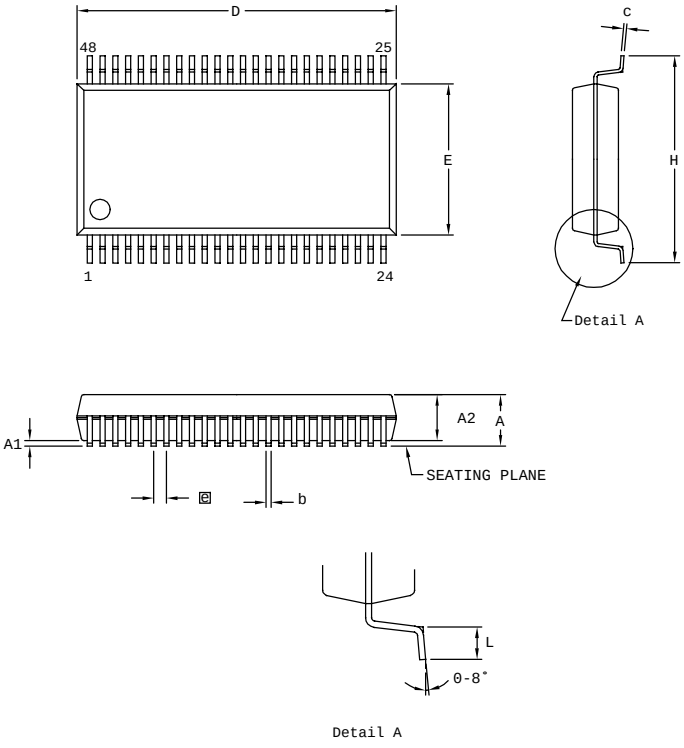
Parameter	Minimum	Typical	Maximum	Units
Resolution		8		bits
Integral Nonlinearity		0.5	1	LSB
Differential Nonlinearity		0.5	1	LSB
Zero Error at 25 °C			7.8	mV
Supply Voltage Range (OTP)	3.0		5.5	V
Supply Voltage Range (ROM)	2.3		5.5	V
Power Dissipation (No Load)			1.2	mW
Clock Frequency (f ADC)			4	MHz
Input Voltage Range	V_{Ref-}		V_{Ref+}	V
Step Response			2/(0.0021 X f ADC)	s
ADC Input Capacitance	25		40	pF
Vref Input Capacitance	25		40	pF
V_{Ref+} Range	V_{Ref-}+2.0		AV_{DD}	V
V_{Ref-} Range	AGND		V_{Ref+}–2.0	V
$(V_{Ref+})–(V_{Ref-})$	2.0		AV_{DD}	V
Temperature Range	0		70	°C
3-db Frequency		(0.0021 X f ADC)		Hz
Signal to Noise	47			db
ADC Output Code		Dout		
Vref Input Source Impedance			1.0	kOhms
ADC Input Source Impedance			1.0	kOhms

Notes: Dout= $[(Vin–V_{Ref-})/(V_{Ref+}–V_{Ref-})]$ X 256
f ADC = set in ADCCTRL configuration register
Step Response is the time to track the input if a step from V_{Ref-} to V_{Ref+} is applied.

The ADC input is a switching capacitor that charges up to the applied input voltage whenever it is configured as an ADC input. If you switch it from digital mode to

Packaging

Figure 37 through Figure 40 show the available packages.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 37. 48-Pin SSOP