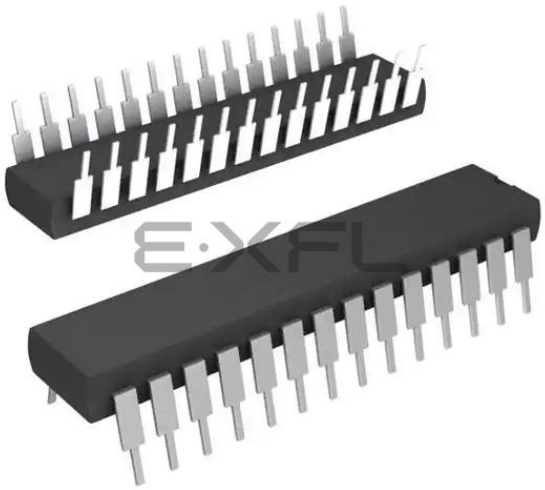

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d991pz008sg

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Interrupts

The Z86D99/Z86L99 family allows up to six different interrupts, three external and three internal, from nine possible sources. The six interrupts are assigned as follows:

- Three edge-triggered external interrupts (P51, P52, and P53), two of which are shared with the two analog comparators
- One internal interrupt assigned to the T8 Timer
- One internal interrupt assigned to the T16 Timer
- One internal interrupt shared between the Low-Battery Detect flag and the T1 Timer

Table 3 presents the interrupt types, the interrupt sources, and the location of the specific interrupt vectors.

Table 3. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ_0	P52 (F/R), Comparator 2	0,1	External interrupt (P52) is triggered by either rising or falling edge; internal interrupt generated by Comparator 2 is mapped into IRQ_0
IRQ_1	P53 (F)	2,3	External interrupt (P53) is triggered by a falling edge
IRQ_2	P51 (R/F), Comparator 1	4,5	External interrupt (P51) is triggered by either a rising or falling edge; internal interrupt generated by Comparator 1 is mapped into IRQ_2
IRQ_3	T16 Timer	6,7	Internal interrupt
IRQ_4	T8 Timer	8,9	Internal interrupt
IRQ_5	LVD, T1 Timer	10,11	Internal interrupt, LVD flag is multiplexed with T1 Timer End-of-Count interrupt
Notes:	F = Falling-edge triggered; R = Rising-edge triggered. When LVD is enabled, IRQ5 is triggered only by low-voltage detection. Timer 1 does not generate an interrupt.		

These interrupts can be masked and their priorities set by using the Interrupt Mask Register (IMR) and Interrupt Priority Register (IPR) (Figure 8.) When more than one interrupt is pending, priorities are resolved by a priority encoder, controlled by the IPR.

Mode Registers

Each port has an associated Mode Register that determines the port's functions and allows dynamic change in port functions during program execution. Port and Mode Registers are mapped into the Standard Register File. Because of their close association, Port and Mode Registers are treated like any other general-purpose register. There are no special instructions for port manipulation. Any instruction that addresses a register can address the ports. Data can be directly accessed in the Port Register, with no extra moves.

Input and Output Registers

Each of the four ports (Ports 2, 4, 5, and 6) has an input register, an output register, and associated buffer and control logic. Because there are separate input and output registers associated with each port, writing bits defined as inputs store the data in the output register. This data cannot be read as long as the bits are defined as inputs. However, if the bits are reconfigured as output, the data stored in the output register is reflected on the output pins and can then be read. This mechanism allows the user to initialize the outputs before driving their loads.

Because port inputs are asynchronous to the Z8 internal clock, a READ operation could occur during an input transition. In this case, the logic level might be uncertain (somewhere between a logic 1 and 0).

General Port I/O

The eight I/O lines of each port (except P43, P52, and P53) can be configured under software control to be either input or output, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. See Figure 12.

Peripherals

Analog Comparators

The Z86D99/Z86L99 family includes two independent on-chip general-purpose analog comparators as shown in Figure 13. The comparators are multiplexed with a digital input signal by the P456CON register. They can also be used to generate interrupts IRQ0 and IRQ2. The comparators are turned off in STOP mode.

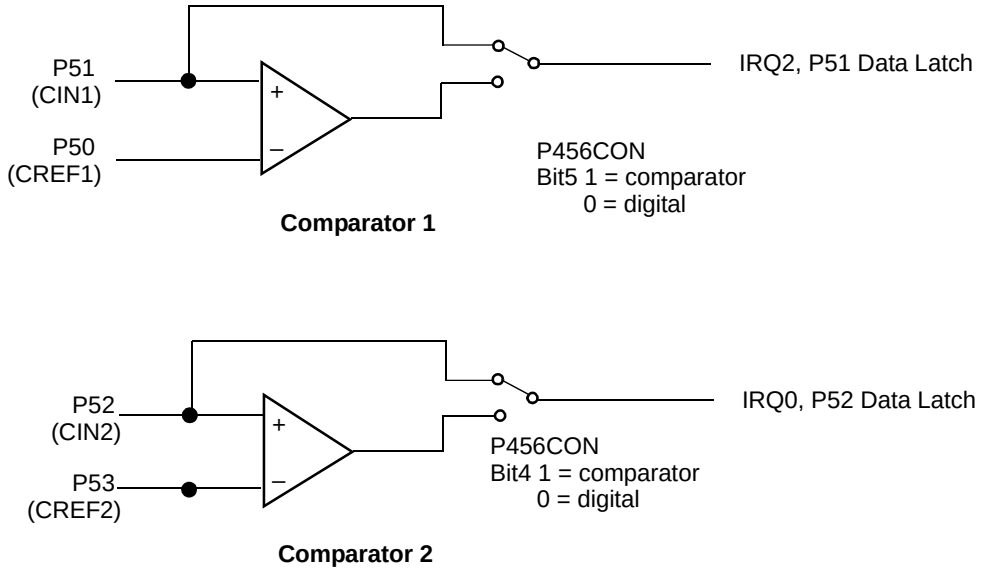


Figure 13. Analog Comparators

Analog/Digital Converter (ADC)

The Z86D99/Z86L99 family incorporates an 8-bit ADC that uses a sigma delta architecture (Figure 14) comprised of a modulator and a digital filter. The input is selected (bit 3,2 from ADCCTRL) with an analog mux from 4 (P47–P44) pins that can be configured as analog inputs (bit 7–4 from ADCCTRL).

Note: Whenever an input pin has an analog value, the digital input buffer has to be disabled in order to reduce the current through the device.

Controlled Current Output

P43 is an open-drain output-only pin on the Z86D990/D991, but it can be configured as output or Tristate High Impedance on the Z86L990/L991. To function properly, Bit 3 of P4M must be set to zero to configure the pin as an open-drain output. For the Z86L990/L991 after reset, P43 defaults to Tristate High Impedance while the Z86D990/D991 P43 is always configured as output. The data at Port 4 must be initialized as it is undefined at power-on reset.

The current output is a controlled current source that is controlled by the output of the value of P43 (see Table 9). P43 *cannot* be configured as input, and if P43 is read, P43 always returns the state of the output value (1 for no sink and 0 for sink).

P43 uses internal current reference and will draw current if it outputs a low logic even without external connection. This applies to both Run mode and Stop mode.

Table 9. Current Sink Pad P43 Specifications (Preliminary)

Parameter	Min	Max	Conditions
Rise time		0.4 µ	LED load
Fall time		0.02 µ	LED load
V_{outmin}		0.54 V	@27C
Comparator response		0.2 µ	
Regulated current	80 mA	120 mA	
Internal resistance		80 Ω	

The pad driver can function in two modes:

- controlled current output, when the voltage on the pad is over a minimum value

$$V_{pad} > V_{outmin}$$

- resistive pull down when the driver cannot regulate the current; in this mode, the gate of the NMOS pull down is raised to the power rail.

The I-V characteristics of the pad are presented in Figure 17.

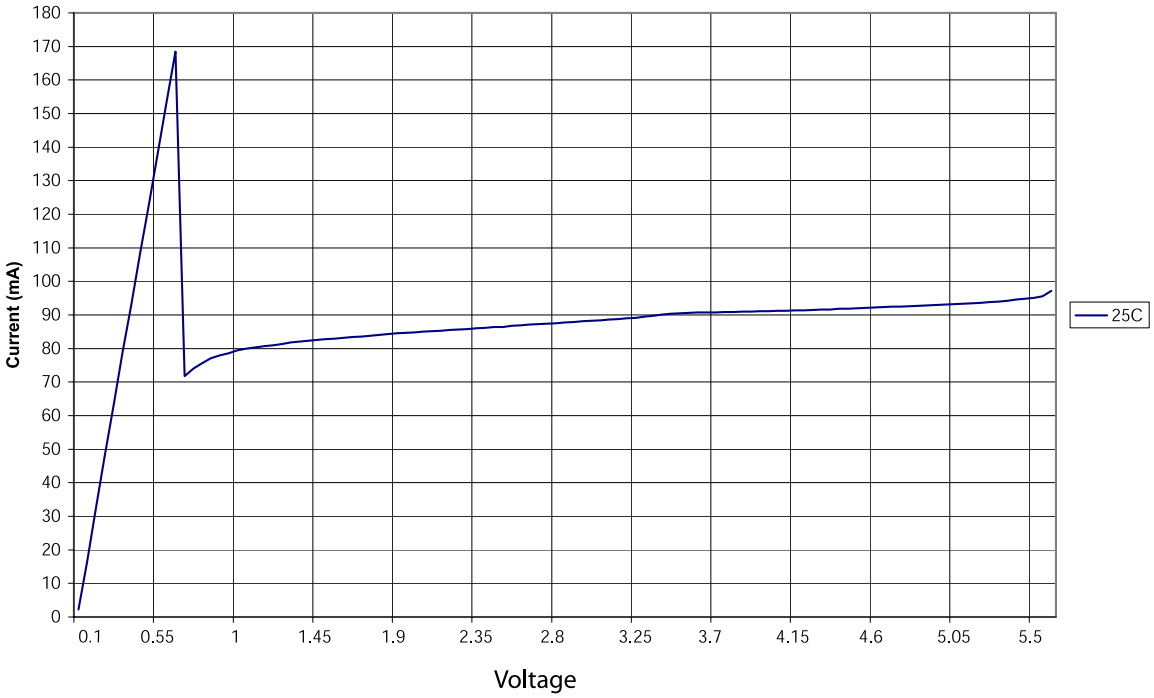


Figure 17. I-V Characteristics for the Current Sink Pad P43

The CPU reads the mode of the pad driver by reading bit number 2 from the LB register. This bit is the output of a Set-Reset flip-flop that sets whenever the voltage on the pad is lower than V_{outmin} and is reset by a CPU write to the respective register.

T1 Timer

The Z86D99/Z86L99 family provides one general-purpose 8-bit counter/timer, T_1, driven by its own 6-bit prescaler, PRE_1. The T_1 counter/timer is independent of the processor instruction sequence, which relieves software from time-critical operations such as interval timing and event counting.

The T_1 counter/timer operates in either single-pass or continuous mode. At the end-of-count, counting either stops or the initial value is reloaded and counting continues. Under software control, new values are loaded immediately or when the end-of-count is reached. Software also controls the counting mode, how the counter/timer is started or stopped, and the counter/timer's use of I/O lines. Both the counter and prescaler registers can be altered while the counter/timer is running.

Table 11. Control and Status Registers (Group F, Bank 0, Registers 0–F)

Grp/Bnk Reg		Register Function	Identifier
(F0h)	rF	Stack Pointer	SP
(F0h)	rE	General-purpose RAM Register	GPR
(F0h)	rD	Register Pointer	RP
(F0h)	rC	Program Control Flag Register	Flags
(F0h)	rB	Interrupt Mask Register	IMR
(F0h)	rA	Interrupt Request Register	IRQ
(F0h)	r9	Interrupt Priority Register	IPR
(F0h)	r8	Reserved	
(F0h)	r7	Port 3 Mode Register	P3M
(F0h)	r6	Port 2 Mode Register	P2M
(F0h)	r5	Reserved	
(F0h)	r4	Reserved	
(F0h)	r3	T1 Prescale Register	PRE1
(F0h)	r2	T1 Data Register	T1
(F0h)	r1	T1 Mode Register	TMR
(F0h)	r0	Reserved	

Table 12. Timer Control Registers (Group 0, Bank D, Registers 0–F)

Grp/Bnk Reg		Register Function	Identifier
(0Dh)	rF	Reserved	
(0Dh)	rE	Reserved	
(0Dh)	rD	Reserved	
(0Dh)	rC	Low-Battery Detect Flag	LB
(0Dh)	rB	T16 MS-Byte Capture Register	HI8
(0Dh)	rA	T16 LS-Byte Capture Register	LO8
(0Dh)	r9	T8 High Capture Register	HI16
(0Dh)	r8	T8 Low Capture Register	LO16
(0Dh)	r7	T16 MS-Byte Hold Register	TC16H
(0Dh)	r6	T16 LS-Byte Hold Register	TC16L
(0Dh)	r5	T8 High Hold Register	TC8H
(0Dh)	r4	T8 Low Hold Register	TC8L
(0Dh)	r3	T8/T16 Control Register B	CTR3
(0Dh)	r2	T16 Control Register	CTR2
(0Dh)	r1	T8/T16 Control Register A	CTR1
(0Dh)	r0	T8 Control Register	CTR0

Table 13. SMR and Port Mode Registers (Group 0, Bank F, Registers 0–F)

Grp/Bnk	Reg	Register Function	Identifier
(0Fh)	rF	Reserved	
(0Fh)	rE	Reserved	
(0Fh)	rD	Reserved	
(0Fh)	rC	Reserved	
(0Fh)	rB	Stop Mode Recovery Register	SMR
(0Fh)	rA	Reserved	
(0Fh)	r9	Reserved	
(0Fh)	r8	ADC Control Register	ADCCTRL
(0Fh)	r7	Reserved	
(0Fh)	r6	Port 6 Mode	P6M
(0Fh)	r5	Port 5 Stop Mode Recovery	P5SMR
(0Fh)	r4	Port 5 Mode Register	P5M
(0Fh)	r3	Reserved	
(0Fh)	r2	Port 4 Mode Register	P4M
(0Fh)	r1	Port 2 Stop Mode Recovery	P2SMR
(0Fh)	r0	Port Configuration Register	P456CON

Register Error Conditions

Registers in the Z8 Standard Register File must be used correctly because certain conditions produce inconsistent results and must be avoided.

- Registers F5h–F9h are write-only registers. If an attempt is made to read these registers, FFh is returned. Reading any write-only register returns FFh.
- When the Register Pointer (register FDH) is read, the least significant four bits (lower nibble) indicate the current Expanded Register File Bank. (For example, 0000 indicates the Standard Register File, while 1010 indicates Expanded Register File Bank A.)
- Writing to bits that are selected as timer outputs changes the I/O register but has no effect on the pin signal.
- The Z8 instruction DJNZ uses any general-purpose working register as a counter.
- Logical instructions such as OR and AND require that the current contents of the operand be read. They do not function properly on write-only registers.

Table 14. Register Description Locations (Continued)

Address Grp/Bnk Register		Register Function	Symbol	Location
0Dh	r11	T8 High Capture	HI8†	page 78
0Dh	r12	Low Battery Detect	LB	page 60
0Fh	r0	Port Configuration (A)	P456CON	page 67
0Fh	r1	Port 2 SMR Source	P2SMR	page 84
0Fh	r2	Port 4 Mode	P4M	page 69
0Fh	r4	Port 5 Mode	P5M	page 70
0Fh	r5	Port 5 SMR Source	P5SMR	page 84
0Fh	r6	Port 6 Mode	P6M	page 71
0Fh	r8	ADC Control	ADCCTRL	page 61
0Fh	r11	Stop Mode Recovery	SMR	page 83
F0h	r1 (R241)	T1 Timer Mode	TMR	page 72
F0h	r2 (R242)	T1 Timer Data	T1	page 72
F0h	r3 (R243)	T1 Timer Prescale	PRE1	page 73
F0h	r6 (R246)	Port 2 Mode	P2M	page 68
F0h	r7 (R247)	Port Configuration (B)	P3M	page 67
F0h	r9 (R249)	Interrupt Priority	IPR	page 64
F0h	r10 (R250)	Interrupt Request	IRQ	page 65
F0h	r11 (R251)	Interrupt Mask	IMR	page 63
F0h	r12 (R252)	Program Control Flags	Flags	page 57
F0h	r13 (R253)	Register Pointer	RP	page 58
F0h	r15 (R255)	Stack Pointer	SP	page 59

Note: †This register is not reset following Stop Mode Recovery (SMR).

Flags and Pointer Registers

In addition to the three standard Z8 flag and pointer registers (Program Control Register Pointer, and Stack Pointer), the Z86D99/Z86L99 family includes a Low-Battery Detect Flag register.

Table 15. FLAGS Register [Group/Bank F0h, Register C (R252)] (Continued)

____3___	Decimal Adjust Flag (D)	R/W	1 0	Used for BCD arithmetic—after a subtraction, the flag is set to 1; following an addition, it is cleared to 0
_____2__	Half Carry Flag (H)	R/W	1 0	Set to 1, whenever an addition generates a “carry out” of bit position 3 (overflow) of an accumulator; or subtraction generates a “borrow into” bit 3
______1_	User Flag (F2)	R/W	1 0	User definable
_______0	User Flag (F1)	R/W	1 0	User definable

Register Pointer (RP)

Z8 instructions can access registers directly or indirectly using either a 4-bit or 8-bit address field. The upper nibble of the Register Pointer, as described in Table 16, contains the base address of the active Working Register GROUP. The lower nibble contains the base address of the Expanded Register File BANK. When using 4-bit addressing, the 4-bit address of the working register (r0 to rF) is combined with the upper nibble of the Register Pointer (identifying the WR GROUP), thus forming the 8-bit actual address.

Table 16. RP Register [Group/Bank F0h, Register D (R253)]

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit/Field	**Working Register Group**				**Expanded Register File Bank**			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	**Bit/Field**	**R/W**	**Value**	**Description**
7654_____	Working Register Group Pointer	R/W	X	Identifies 1 of 16 possible WR Groups, each containing 16 Working Registers
_____3210	Expanded Register File Bank Pointer	R/W	X	Identifies 1 of 16 possible ERF Banks; only Banks 0, D, and F are valid for the Z86D99/Z86L99 family

Port Configuration Registers (P456CON and P3M)

The port configuration register (described in Table 24) switches the comparator inputs from digital to analog and allows Ports 4, 5, and/or 6 to be switched from push/pull active outputs to open drain outputs. In ZiLOG Test Mode, bit 3 of this register is used to enable the Address Strobe/Data Strobe. Bit 3 is not available in User Mode.

Table 24. P456CON Register (Group/Bank 0Fh, Register 0)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Not Used		P51_ Mode	P52_ Mode	Reserved	P6_ Output	P5_ Output	P4_ Output
R/W	R/W	R/W	R/W	R/W	R/W	W	W	W
Reset	0	0	0	0	0	1	1	1†

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	Not Used	R/W		These bits exist but do not have any function assigned to them; they are reserved for future extensions and must not be used.
__5_____	Comparator 1 Mode	R/W	1 0	Analog (P50, P51 as Inputs) Digital inputs
___4____	Comparator 2 Mode	R/W	1 0	Analog comparator inputs (P52, P53 configured as Inputs) Digital inputs
____3___	Reserved			
_____2__	Port 6 Output Configuration	W	1 0	Push-Pull Active Open Drain Outputs Always reads back 1*
______1_	Port 5 Output Configuration	W	1 0	Push-Pull Active Open Drain Outputs Always reads back 1*
_______0	Port 4 Output Configuration	W	1 0	Push-Pull Active Open Drain Outputs Always reads back 1*†

Note: *Do not use the read-modify-write instructions (for example, OR and AND) with this register. Bits 0, 1, and 2 always read back 1.

Note: †For Z86L990/L991, P43 can never be configured as push-pull. After any reset, P43 is configured as tristate high impedance.

Port 2 outputs are configured using the P3M Register, shown in Table 25. Bit 0 of the P3M Register switches Port 2 from push/pull active to open drain outputs. No other bits in this register are implemented.

T8/T16 Control Register B (CTR3)

The T8/T16 Control Register B, known as CTR3, is a new register to the Z86D99/ Z86L99 family. This register allows the T_8 and T_{16} counters to be synchronized. The settings of CTR3 are described in Table 39.

Table 39. CTR3 Register (Group/Bank 0Dh, Register 3)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_ Enable	T8_ Enable	Sync Mode	Reserved				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	X	X	X	X	X

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	T_{16} Enable	R	1	Counter Enabled
		R	0	Counter Disabled
		W	1	Enable Counter
		W	0	Stop Counter
_6_____	T_8 Enable	R	1	Counter Enabled
		R	0	Counter Disabled
		W	1	Enable Counter
		W	0	Stop Counter
__5____	Sync Mode	R/W	1	Enable Sync Mode
			0	Diable Sync Mode
___43210	Reserved	R	1	Always reads 11111
		W	X	No Effect

T16 Control Register (CTR2)

The T16 Control Register, known as CTR2, controls the operation of the 16-bit T_{16} timer (see Table 45).

Table 45. CTR2 Register (Group/Bank 0Dh, Register 2)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_ Enable	Single/ Mod-ulo-n	Time_ Out	T16_Clock		Capture INT_ Mask	Counter INT_ Mask	P41_ Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	T_{16} Enable	R	1	Counter Enabled
		R	0	Counter Disabled
		W	1	Enable Counter
		W	0	Stop Counter
_6_____	Single/ Modulo-n	R/W		In Transmit Mode:
			1	Single Pass
			0	Modulo-n
				In Demodulation Mode:
			1	T_{16} Does Not Recognize Edge
			0	T_{16} Recognizes Edge
__5_____	Time_Out	R	1	Counter Timeout Occurred
		R	0	No Counter Timeout
		W	1	Reset Flag to 0
		W	0	No Effect
___43___	T_{16} Clock	R/W	11	SCLK/8
			10	SCLK/4
			01	SCLK/2
			00	SCLK
_____2__	Capture Interrupt Mask	R/W	1	Enable Data Capture Interrupt
			0	Disable Data Capture Interrupt
______1_	Counter Interrupt Mask	R/W	1	Enable Time_Out Interrupt
			0	Disable Time_Out Interrupt
_______0	P41_Out	R/W	1	P41 configured as T_{16} Output
			0	P41 configured as I/O

Table 54. DC Characteristics for the Z86D99X (OTP Only)

Symbol	Parameter	V_{DD}	Min	Max	Units	Comments
V_{DD}	Power Supply Voltage		3	5.5		
V_{CH}	Clock Input High Voltage	3.0 V 5.5 V	0.8Vdd 0.8Vdd	Vdd+0.3 Vdd+0.3	V V	Driven by Ext. clock generator
V_{CL}	Clock Input Low Voltage	3.0 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd		Driven by Ext. clock generator
V_{IH}	Input High Voltage	3.0 V 5.5 V	0.7Vdd 0.7Vdd	Vdd+0.3 Vdd+0.3	V V	
V_{IL}	Input Low Voltage	3.0 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd	V V	
V_{OH1}	Output High Voltage Regular I/O	3.0 V 5.5 V	V_{DD}–0.8 V_{DD}–0.8		V V	–1.2 mA
V_{OH2}	High Drive Pins (P54, P55, P56, P57)	3.0 V 5.5 V	V_{DD}–0.8 V_{DD}–0.8		V V	–5.0 mA
V_{OL1}	Regular I/O Output low voltage	3.0 V 5.5 V		0.4 0.8	V V	2 mA 4.0 mA
V_{OL2}	High Drive Pins (P54, P55, P56, P57)	3.0 V 5.5 V		0.4 0.8	V V	4 mA 7.0 mA
I_{CCO}	Controlled Current Output (P43)	3.0 V 5.5 V	70 70	120 120	mA mA	Vout = 1.2 V to VDD (see Figure 17)
I_{IL}	Input Leakage	3.0 V 5.5 V	–1 –1	1 µA 1 µA	µA µA	Vin=0 V, Vdd Vin=0 V, Vdd
I_{CC}	Supply Current	3.0 V 5.5 V 3.0 V 5.5 V		10 15 250 850	mA mA µA µA	at 8 MHz at 8 MHz at 32 KHz at 32 KHz ADC is off.
I_{CC1}	Standby Current (Halt Mode)	3.0 V 5.5 V 3.0 V 5.5 V		3 5 2 4	mA mA mA mA	Vin=0 V, Vdd at 8 MHz Clock divided by 16 XTAL running ADC is off.
I_{CC2}	Standby Current (STOP Mode)	3.0 V 5.5 V		20 30	µA µA	Vin=0 V, Vdd; ADC is off. P43=1 or high impedance WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.
I_{ADC}	Current with A/D Running	3.0 V 5.5 V		500 900	µA µA	
V_{LV}	Vdd Low-Voltage Protection			2.90	V	Low voltage protection is also known as brownout. Typical is 2.6 V.
V_{LB}	Low-Battery Detection			VLV+ 0.5	V V	

Analog-to-Digital Converter Characteristics

Table 56 lists the analog-to-digital converter characteristics.

Table 56. Analog-to-Digital Converter Characteristics

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		bits
Integral Nonlinearity		0.5	1	LSB
Differential Nonlinearity		0.5	1	LSB
Zero Error at 25 °C			7.8	mV
Supply Voltage Range (OTP)	3.0		5.5	V
Supply Voltage Range (ROM)	2.3		5.5	V
Power Dissipation (No Load)			1.2	mW
Clock Frequency (f ADC)			4	MHz
Input Voltage Range	V_{Ref-}		V_{Ref+}	V
Step Response			2/(0.0021 X f ADC)	s
ADC Input Capacitance	25		40	pF
Vref Input Capacitance	25		40	pF
V_{Ref+} Range	V_{Ref-}+2.0		AV_{DD}	V
V_{Ref-} Range	AGND		V_{Ref+}–2.0	V
$(V_{Ref+})–(V_{Ref-})$	2.0		AV_{DD}	V
Temperature Range	0		70	°C
3-db Frequency		(0.0021 X f ADC)		Hz
Signal to Noise	47			db
ADC Output Code		Dout		
Vref Input Source Impedance			1.0	kOhms
ADC Input Source Impedance			1.0	kOhms

Notes: Dout= $[(Vin–V_{Ref-})/(V_{Ref+}–V_{Ref-})]$ X 256
f ADC = set in ADCCTRL configuration register
Step Response is the time to track the input if a step from V_{Ref-} to V_{Ref+} is applied.

The ADC input is a switching capacitor that charges up to the applied input voltage whenever it is configured as an ADC input. If you switch it from digital mode to

the ADC input mode, the switching capacitor starts to charge up from 0 V. For the maximum swing (Dout = 0 to FF), it takes 2/(0.0021x f ADC). For an 8-MHz MCU crystal (with clock divide-by-two mode), the internal system clock is 4 MHz. In ADCCTRL, if you select the ADC frequency = system clock divided by 1 option, f ADC = 4 MHz. The step response = 238 uS.

AC Characteristics

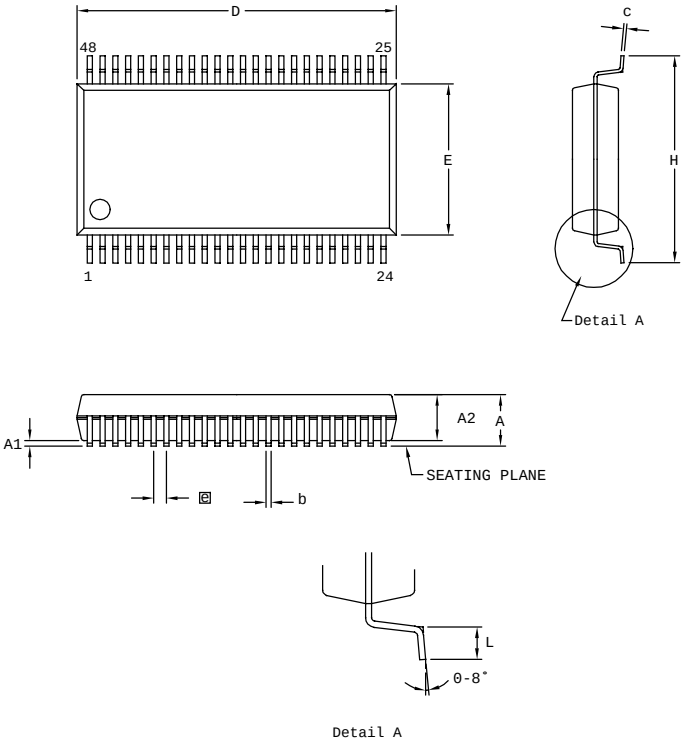
Table 57 lists the AC characteristics.

Table 57. AC Characteristics

No.	Symbol	Parameter	VDD	Min	Max	Units
1	TpC	Input Clock Period	2.3 V 5.5 V	120 120	DC DC	ns
2	TrC, TfC	Clock Input Rise and Fall Times	2.3 V 5.5 V		25 ns 25 ns	
3	TwC	Input Clock Width	2.3 V 5.5 V	5.0 5.0		ns ns
4	TwTinL	Timer Input Low Width	2.3 V 5.5 V	2TPC 2TPC		 ns
5	TwTinH	Timer Input High Width	2.3 V 5.5 V	2 2		TpC TpC
6	TpT1in	Timer 1 Input Period	2.3 V 5.5 V	8 8		TpC TpC
7	TrTin, TfTin	Timer Input Rise and Fall Time	2.3 V 5.5 V		100 100	ns ns
8	TwIL	Interrupt Request Low Time	2.3 V 5.5 V	100 70		ns ns
9	TwIH	Interrupt Request Input High Time	2.3 V 5.5 V	5 5		TpC TpC
10	Twsm	Stop-Mode Recovery Width Spec	2.3 V 5.5 V	12 12		ns ns
12	Twdt	Watch-Dog Timer Time Out	2.3 V 5.5 V	25 10		ms ms

Packaging

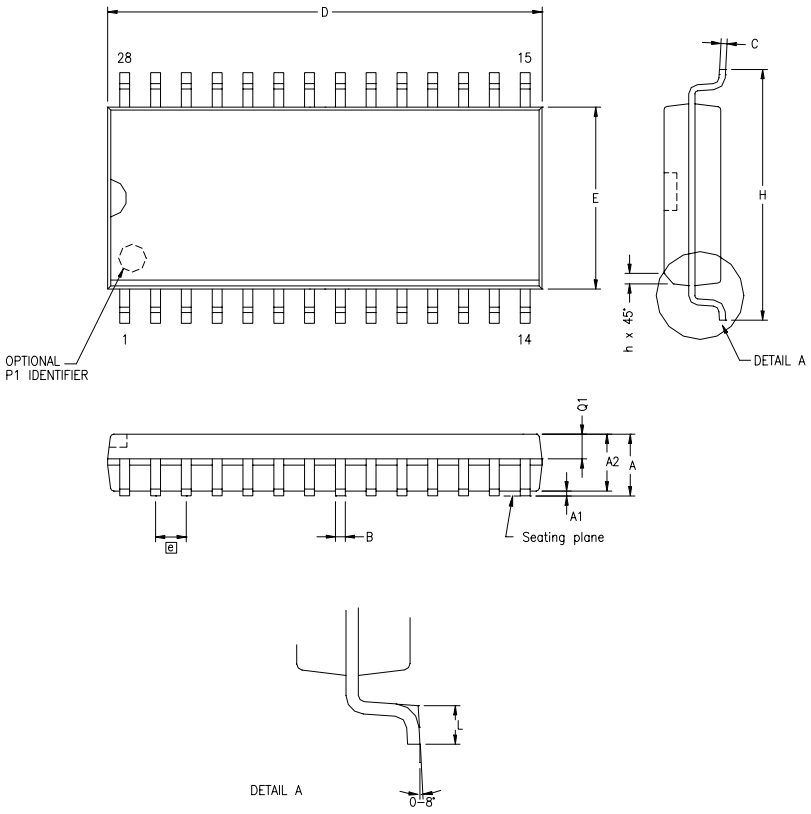
Figure 37 through Figure 40 show the available packages.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 37. 48-Pin SSOP



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40. 28-Pin SOIC