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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d991sz008sc

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Architectural Overview

The Z86D99 is a low-voltage general-purpose one-time programmable (OTP) Z8® microcontroller with an integrated four-channel 8-bit sigma delta analog-to-digital converter. The Z86L99 is the read-only memory (ROM) version of this controller.

The Z86D99/Z86L99 family is designed to be used in a wide variety of embedded control applications including battery chargers, home appliances, infrared (IR) remote controls, security systems, and wireless keyboards.

It has three counter/timers, a general-purpose 8-bit counter/timer with a 6-bit prescaler and an 8-bit/16-bit counter/timer pair that can be used individually for general-purpose timing or as a pair to automate the generation and reception of complex pulses or signals. Unique features of the Z86D99/Z86L99 family of products include 489 bytes of general-purpose random-access memory (RAM), 256 bytes of which are mapped into the program memory space and can be used to store data variables or as executable RAM, a low-battery detection flag, and a controlled current output pin, which is a regulated current source that sinks a predefined current (I_{CCO}). Table 1 highlights the basic product features of these microcontrollers.

Table 1. Z86L99/Z86D99 Feature Comparison

	Pins	I/O	Memory (Bytes)	Operating Voltage (V)	ADC	Timers	Watch-Dog Timer
Z86D990	40/48	32	32K OTP	3.0–5.5	4 channel	3	Yes
Z86D991	28	24	32K OTP	3.0–5.5	—	3	Yes
Z86L990	40/48	32	16K ROM	2.3–5.5	4 channel	3	Yes
Z86L991	28	24	16K ROM	2.3–5.5	—	3	Yes
Z86L996	28	24	4K ROM	2.3–5.5	—	3	Yes
Z86L997	28	24	8K ROM	2.3–5.5	—	3	Yes

The Z8 microcontroller core offers more flexibility and performance than accumulator-based microcontrollers. All 256 general-purpose registers, including dedicated input/output (I/O) port registers, can be used as accumulators. This unique register-to-register architecture avoids accumulator bottlenecks for high code efficiency. The registers can be used as address pointers for indirect addressing, as index registers, or for implementing an on-chip stack.

The Z8 has a sophisticated interrupt structure and automatically saves the program counter and status flags on the stack for fast context-switching. Speed of execution and smooth programming are also supported by a “working register area” with short 4-bit register addresses.

- Interrupt Control (IPR, IMR, and IRQ)
- Stop Mode Recovery (SMR, P2SMR, and P5SMR)
- Low-Battery Detect (LB) Flag

The Z8 uses a 16-bit Program Counter (PC) to determine the sequence of current program instructions. The PC is not an addressable register.

Peripheral registers are used to transfer data, configure the operating mode, and control the operation of the on-chip peripherals. Any instruction that references the register file can access the peripheral registers. The following are peripheral control registers:

- Analog/Digital Converter (ADCCTRL and ADCDATA)
- T1 Timer/Counter (TMR, T1, and PRE1)
- T8 Timer/Counter (CTR0, HI8, LO8, TC8H, and TC8L)
- T16 Timer/Counter (CTR2, HI16, LO16, TC16H, and TC16L)
- T8/T16 Control Registers (CTR1and CTR3)

In addition, the four port registers are considered to be peripheral registers. The following are port control registers:

- Port Configuration Registers (P456CON and P3M)
- Port 2 Control and Mode Registers (P2 and P2M)
- Port 4 Control and Mode Registers (P4 and P4M)
- Port 5 Control and Mode Registers (P5 and P5M)
- Port 6 Control and Mode Registers (P6 and P6M)

The functions and applications of the control and peripheral registers are explained in “Control and Status Registers” on page 52.

Memory (ROM/OTP and RAM)

There are four basic address spaces available to support a wide range of configurations:

- Program memory (on-chip)
- Standard register file
- Expanded register file
- Executable RAM

The Z8 standard register file totals up to 256 consecutive bytes organized as 16 groups of 16 eight-bit registers. These registers consist of I/O port registers,

general-purpose RAM registers, and control and status registers. Every RAM register acts like an accumulator, speeding instruction execution and maximizing coding efficiency. Working register groups allow fast context switching.

The standard register file of the Z8 (known as Bank 0) has been expanded to form 16 expanded register file (ERF) banks. The expanded register file allows for additional system control registers and for the mapping of additional peripheral devices into the register area. Each ERF bank can potentially consist of up to 256 registers (the same amount as in the standard register file) that can then be divided into 16 working register groups. Currently, only Group 0 of ERF Banks F and D (0Fh and 0Dh) has been implemented.

In addition to the standard program memory and the RAM register files, the Z86D99/Z86L99 family also has 256 bytes of executable RAM that has been mapped into the upper 256 bytes of the program memory address space (FF00h–FFFFh). Data can be written to the executable RAM by using the LDC instruction.

Program Memory Structure

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts (IRQ_0 through IRQ_5.) Address 12 (0Ch) up to 32,767 (7FFFh) consists of on-chip one-time programmable memory. The Z86L99X only has the 4K/8K/16K ROM size.

After any reset operation (power-on reset, watch-dog timer time out, and stop mode recovery), program execution resumes with the initial instruction fetch from location 000Ch. After a reset, the first routine executed must be one that initializes the control registers to the required system configuration.

A unique feature of the Z86D99/Z86L99 family is the presence of 256 bytes of on-chip executable RAM. This random-access memory is in addition to the standard Z8 register file memory available on all Z8 microcontrollers. As illustrated in Figure 5, the executable RAM is mapped into the upper 256 bytes of the 64K program memory address space (FF00h–FFFFh). Data can be written to the executable RAM by using the LDC instruction.

Memory locations between 8000h and FEFFh have not been implemented on the Z86D99X microcontrollers.

The Z86D99/Z86L99 family does not have the capability of accessing external memory.

Location (Hex)	
FFFF FF00	256 bytes **Executable RAM**
	Not Implemented
3FFF/7FFF (ROM)/(OTP) 000C	**PROGRAM MEMORY** Location of the first byte of the initial instruction executed after RESET
000B	IRQ_5 (lower byte)
000A	IRQ_5 (upper byte)
0009	IRQ_4 (lower byte)
0008	IRQ_4 (upper byte)
0007	IRQ_3 (lower byte)
0006	IRQ_3 (upper byte)
0005	IRQ_2 (lower byte)
0004	IRQ_2 (upper byte)
0003	IRQ_1 (lower byte)
0002	IRQ_1 (upper byte)
0001	IRQ_0 (lower byte)
0000	IRQ_0 (upper byte)

Figure 5. Program Memory Map

Z8 Standard Register File (Bank 0)

Bank 0 of the Z8 expanded register file architecture is known as the standard register file of the Z8. As shown in Figure 6, the Z8 standard register file consists of 16 groups of sixteen 8-bit registers known as Working Register (WR) groups. Working Register Group F contains various control and status registers. The lower half of Working Register Group 0 consists of I/O port registers (R0 to R7), the upper eight registers are available for use as general-purpose RAM registers. Working Register Group 1 through Group E of the standard register file are available to be used as general-purpose RAM registers. The user can use 233 bytes of general-purpose RAM registers in the standard Z8 register file (Bank 0).

Interrupts

The Z86D99/Z86L99 family allows up to six different interrupts, three external and three internal, from nine possible sources. The six interrupts are assigned as follows:

- Three edge-triggered external interrupts (P51, P52, and P53), two of which are shared with the two analog comparators
- One internal interrupt assigned to the T8 Timer
- One internal interrupt assigned to the T16 Timer
- One internal interrupt shared between the Low-Battery Detect flag and the T1 Timer

Table 3 presents the interrupt types, the interrupt sources, and the location of the specific interrupt vectors.

Table 3. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ_0	P52 (F/R), Comparator 2	0,1	External interrupt (P52) is triggered by either rising or falling edge; internal interrupt generated by Comparator 2 is mapped into IRQ_0
IRQ_1	P53 (F)	2,3	External interrupt (P53) is triggered by a falling edge
IRQ_2	P51 (R/F), Comparator 1	4,5	External interrupt (P51) is triggered by either a rising or falling edge; internal interrupt generated by Comparator 1 is mapped into IRQ_2
IRQ_3	T16 Timer	6,7	Internal interrupt
IRQ_4	T8 Timer	8,9	Internal interrupt
IRQ_5	LVD, T1 Timer	10,11	Internal interrupt, LVD flag is multiplexed with T1 Timer End-of-Count interrupt
Notes:	F = Falling-edge triggered; R = Rising-edge triggered. When LVD is enabled, IRQ5 is triggered only by low-voltage detection. Timer 1 does not generate an interrupt.		

These interrupts can be masked and their priorities set by using the Interrupt Mask Register (IMR) and Interrupt Priority Register (IPR) (Figure 8.) When more than one interrupt is pending, priorities are resolved by a priority encoder, controlled by the IPR.

start the interrupt process. However, the IPR does not have to be initialized for polled processing.

Interrupts must be globally enabled using the EI instruction. Setting bit 7 of the IMR is not sufficient. Subsequent to this EI instruction, interrupts can be enabled either by IMR manipulation or by use of the EI instruction, with equivalent effects.

Additionally, interrupts must be disabled by executing a DI instruction before the IPRs or IMRs can be modified. Interrupts can then be enabled by executing an EI instruction.

IRQ Software Interrupt Generation

IRQ can be used to generate software interrupts by specifying IRQ as the destination of any instruction referencing the Z8 Standard Register File. These Software Interrupts (SWIs) are controlled in the same manner as hardware-generated requests (the IPR and the IMR control the priority and enabling of each SWI level).

To generate a SWI, the request bit in the IRQ is set as follows:

```
OR    IRQ, #NUMBER
```

where the immediate data, *NUMBER*, has a 1 in the bit position corresponding to the appropriate level of the SWI.

For example, for an SWI on IRQ5, *NUMBER* has a 1 in bit 5. With this instruction, if the interrupt system is globally enabled, IRQ5 is enabled, and there are no higher priority pending requests, control is transferred to the service routine pointed to by the IRQ5 vector.

Reset Conditions

A system reset overrides all other operating conditions and puts the Z8 into a known state. The control and status registers are reset to their default conditions after a power-on reset (POR) or a Watch-Dog Timer (WDT) time-out while in RUN mode. The control and status registers are not reset to their default conditions after Stop Mode Recovery (SMR) while in HALT or STOP mode.

General-purpose registers are undefined after the device is powered up. Resetting the Z8 does not affect the contents of the general-purpose registers. The registers keep their most recent value after any reset, as long as the reset occurs in the specified V_{CC} operating range. Registers do not keep their most recent state from a V_{LV} reset, if V_{CC} drops below V_{RAM} (see Table 54 on page 87).

Following a reset (see Table 5), the first routine executed must be one that initializes the control registers to the required system configuration.

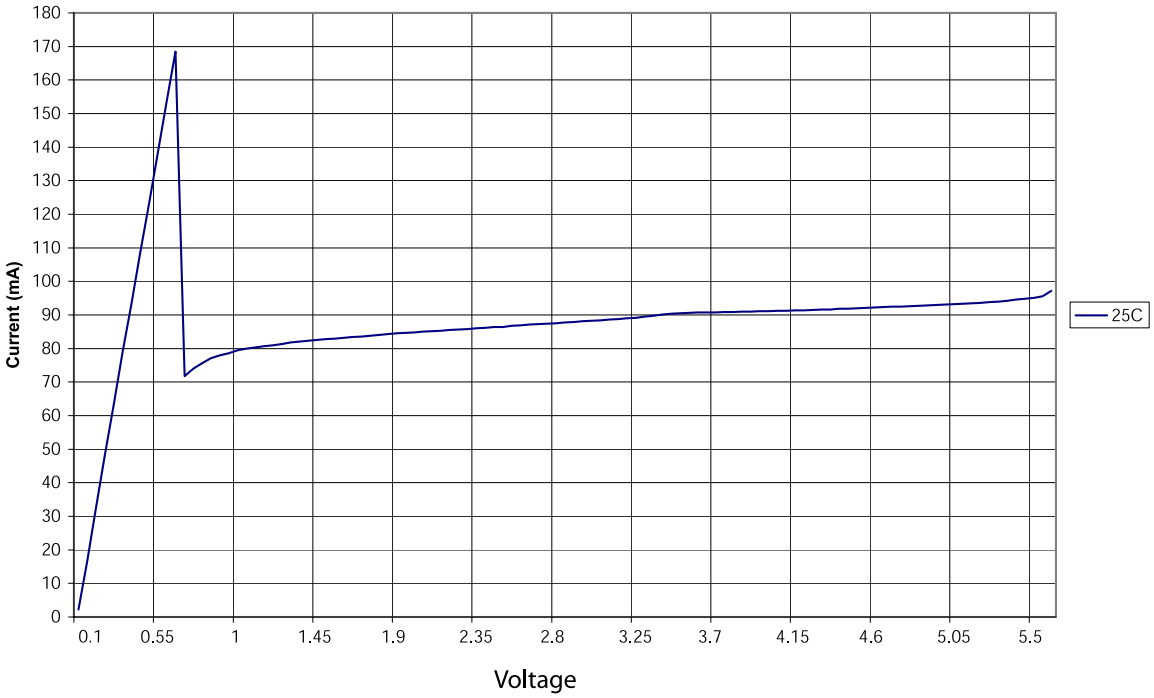

Figure 17. I-V Characteristics for the Current Sink Pad P43

The CPU reads the mode of the pad driver by reading bit number 2 from the LB register. This bit is the output of a Set-Reset flip-flop that sets whenever the voltage on the pad is lower than V_{outmin} and is reset by a CPU write to the respective register.

T1 Timer

The Z86D99/Z86L99 family provides one general-purpose 8-bit counter/timer, T_1, driven by its own 6-bit prescaler, PRE_1. The T_1 counter/timer is independent of the processor instruction sequence, which relieves software from time-critical operations such as interval timing and event counting.

The T_1 counter/timer operates in either single-pass or continuous mode. At the end-of-count, counting either stops or the initial value is reloaded and counting continues. Under software control, new values are loaded immediately or when the end-of-count is reached. Software also controls the counting mode, how the counter/timer is started or stopped, and the counter/timer's use of I/O lines. Both the counter and prescaler registers can be altered while the counter/timer is running.

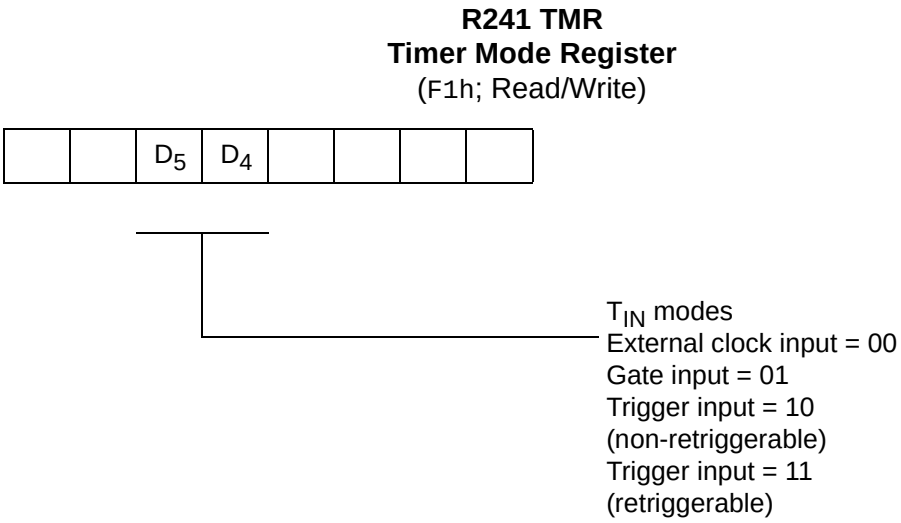

Figure 28. Timer Mode Register T_{IN} Operation

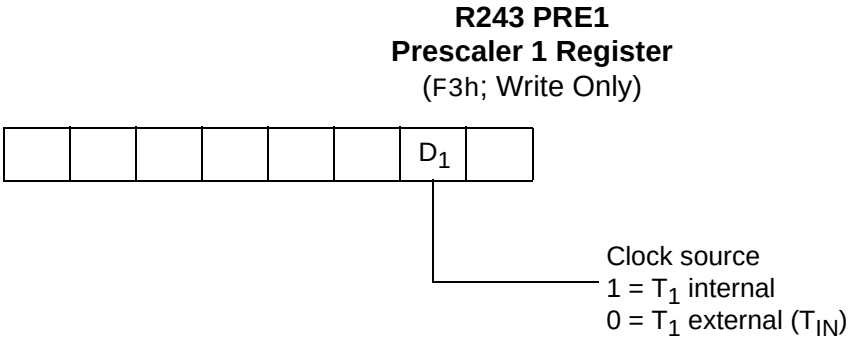

Figure 29. Prescaler 1 T_{IN} Operation

The T_1 counter/timer clock source must be configured for external by setting PRE_1 bit D_2 to 0. The Timer Mode register bits D_5 and D_4 can then be used to select the T_{IN} operation.

For T_1 to start counting as a result of a T_{IN} input, the Enable Count bit D_3 in TMR must be set to 1. When using T_{IN} as an external clock or a gate input, the initial values must be loaded into the down-counters by setting the Load bit D_2 in TMR to 1 before counting begins. Initial values are automatically loaded in Trigger and Retrigger modes, so software loading is unnecessary.

Configure $P5_2$ as an input line by setting P5M bit D_2 to 1.

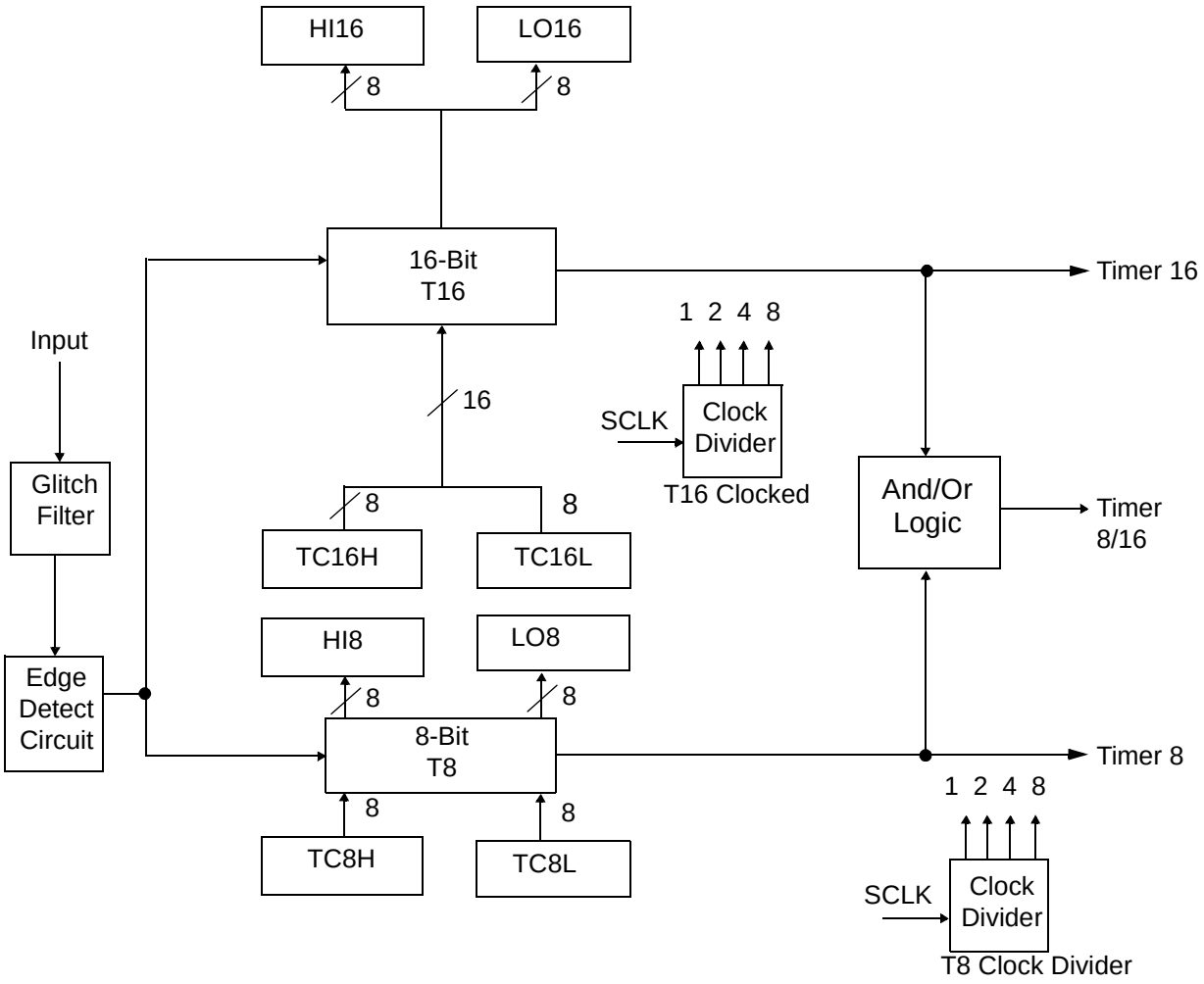

Figure 33. Counter/Timer Architecture

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If CTR1, D1 is 0, T8_OUT is 1. If CTR1, D1 is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In single-pass mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1). In modulo-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if T8_OUT level is 0), TC8L is loaded; if T8_OUT is 1, TC8H is loaded.

T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5), and generates an interrupt if enabled (CTR0 D1). This completes one cycle. T8 then loads from TC8H or TC8L, according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time.The new values take effect when they are loaded. Do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed. An initial count of 0 causes TC8 to count from 0 to FFh to FEh. Transition from 0 to FFh is not a time-out condition (see Figure 34).

Registers (Grouped by Function)

The following is a summary of the 37 special-purpose registers of the Z86D99/ Z86L99 family grouped by function. The following are the functional groups:

- Flags and Pointers
- Analog-to-Digital Converter Control
- Interrupt Control
- I/O Port Control
- Timer Control—General-Purpose Timer (T1)
- Timer Control—T8 and T16 Timers
- Stop-Mode Recovery Control

For any of the registers described in this section (see Table 14), bits identified as “Reserved” either do not exist (meaning they have not been implemented in this design) or have a special purpose in a ZiLOG engineering or test environment.

Caution: Do not attempt to use these bits as the results are unpredictable and meaningless.

Table 14. Register Description Locations

Address Grp/Bnk Register	Register Function	Symbol	Location
00h r2 (R2)	Port 2 Data	P2	page 68
00h r4 (R4)	Port 4 Data	P4	page 69
00h r5 (R5)	Port 5 Data	P5	page 70
00h r6 (R6)	Port 6 Data	P6	page 71
00h r7 (R7)	ADC Data	ADCDATA	page 62
0Dh r0	T8 Timer Control	CTR0	page 77
0Dh r1	T8/T16 Control (A)	CTR1	page 74
0Dh r2	T16 Timer Control	CTR2	page 80
0Dh r3	T8/T16 Control (B)	CTR3	page 76
0Dh r4	T8 Low Load	TC8L†	page 79
0Dh r5	T8 High Load	TC8H†	page 79
0Dh r6	T16 Low Load	TC16L†	page 82
0Dh r7	T16 High Load	TC16H†	page 82
0Dh r8	T16 Low Capture	LO16†	page 81
0Dh r9	T16 High Capture	HI16†	page 81
0Dh r10	T8 Low Capture	LO8†	page 78

Program Control Flag Register (Flags)

The Program Control Flag register (see Table 15) reflects the current status of the Z8 as shown in Table 15. The FLAGS register contains six bits of status information that are set or cleared by CPU operations. Four of the bits (C, V, Z, and S) can be tested for use with conditional jump instructions. Two flags (H and D) cannot be tested and are used for BCD arithmetic. The two remaining flags in the register (F1 and F2) are available to the user, but they must be set or cleared by instructions and are not usable with conditional jumps.

Table 15. FLAGS Register [Group/Bank F0h, Register C (R252)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**C**	**Z**	**S**	**V**	**D**	**H**	**F2**	**F1**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	Carry Flag (C)	R/W	1	Indicates the “carry out” of bit 7 position of a register being used as an accumulator; on Rotate and Shift instructions this bit contains the most recent value shifted out of the specified register
_6_____	Zero Flag (Z)	R/W	1	Indicates that the contents of an accumulator register is zero following an arithmetic or logical operation
__5_____	Sign Flag (S)	R/W	X	Stores the value of the most significant bit of a result following an arithmetic, logical, Rotate, or Shift operation; in arithmetic operations on signed numbers, a positive number is identified by a 0, and a negative number is identified by a 1
___4____	Overflow Flag (V)	R/W	1	For signed arithmetic, Rotate, and Shift operations, the flag is set to 1 when the result is greater than the maximum possible number (>127) or less than the minimum possible number (<-128) that can be represented in two’s complement form; following logical operations, this flag is set to 0

Port 5 Control and Mode Registers (P5 and P5M)

Port 5 is a general-purpose 8-bit, bidirectional I/O port, as shown in Table 30. Each of the eight Port 5 I/O lines can be independently programmed as either input or output using the Port 5 Mode Register (see Table 31.)

Table 30. P5 Register [Group/Bank 00h, Register 5 (R5)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**Port 5 Data**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X
R = Read, W = Write, X = Indeterminate								

Bit Position	Bit/Field	R/W	Value	Description
76543210	Port 5 Data	R/W	Data	Port 5 Input/Output Register

Table 31. P5M Register (Group/Bank 0Fh, Register 4)

Bit	7	6	5	4	3	2	1	0
Bit/Field	**P57M**	**P56M**	**P55M**	**P54M**	**P53M**	**P52M**	**P51M**	**P50M**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
R = Read, W = Write, X = Indeterminate								

Bit Position	Bit/Field	R/W	Value	Description
7654__10 (by bit)	Port 5 Mode Select	R/W	1 0	Input Output
____32__	P53, P52 Mode Select	R/W	1	Input Regardless of what is written to this pin, P53 and P52 are always in input mode.

A bit set to a 1 in the P5M Register configures the corresponding bit in Port 5 as an input, while a bit set to 0 configures an output line.

Note: Regardless of how P5M bits 2 and 3 are set, P52 and P53 are always in input mode.

T16 MS-Byte Capture Register (HI16)

The T16 MS-Byte Capture Register, as described in Table 46, holds the captured data from the output of the T_{16} counter/timer. This register holds the most significant byte of the data.

Table 46. HI16 Register (Group/Bank 0Dh, Register 9)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_Capture_HI							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_{16} Capture HI	R W	Data	MS-Byte of Captured Data No Effect

T16 LS-Byte Capture Register (LO16)

The T16 LS-Byte Capture Register, as described in Table 47, holds the captured data from the output of the T_{16} counter/timer. This register holds the least significant byte of the data.

Table 47. LO16 Register (Group/Bank 0Dh, Register 8)

Bit	7	6	5	4	3	2	1	0
Bit/Field	T16_Capture_LO							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_{16} Capture LO	R W	Data	LS-Byte of Captured Data No Effect

Table 54. DC Characteristics for the Z86D99X (OTP Only)

Symbol	Parameter	V_{DD}	Min	Max	Units	Comments
V_{DD}	Power Supply Voltage		3	5.5		
V_{CH}	Clock Input High Voltage	3.0 V 5.5 V	0.8Vdd 0.8Vdd	Vdd+0.3 Vdd+0.3	V V	Driven by Ext. clock generator
V_{CL}	Clock Input Low Voltage	3.0 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd		Driven by Ext. clock generator
V_{IH}	Input High Voltage	3.0 V 5.5 V	0.7Vdd 0.7Vdd	Vdd+0.3 Vdd+0.3	V V	
V_{IL}	Input Low Voltage	3.0 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd	V V	
V_{OH1}	Output High Voltage Regular I/O	3.0 V 5.5 V	V_{DD}–0.8 V_{DD}–0.8		V V	–1.2 mA
V_{OH2}	High Drive Pins (P54, P55, P56, P57)	3.0 V 5.5 V	V_{DD}–0.8 V_{DD}–0.8		V V	–5.0 mA
V_{OL1}	Regular I/O Output low voltage	3.0 V 5.5 V		0.4 0.8	V V	2 mA 4.0 mA
V_{OL2}	High Drive Pins (P54, P55, P56, P57)	3.0 V 5.5 V		0.4 0.8	V V	4 mA 7.0 mA
I_{CCO}	Controlled Current Output (P43)	3.0 V 5.5 V	70 70	120 120	mA mA	Vout = 1.2 V to VDD (see Figure 17)
I_{IL}	Input Leakage	3.0 V 5.5 V	–1 –1	1 µA 1 µA	µA µA	Vin=0 V, Vdd Vin=0 V, Vdd
I_{CC}	Supply Current	3.0 V 5.5 V 3.0 V 5.5 V		10 15 250 850	mA mA µA µA	at 8 MHz at 8 MHz at 32 KHz at 32 KHz ADC is off.
I_{CC1}	Standby Current (Halt Mode)	3.0 V 5.5 V 3.0 V 5.5 V		3 5 2 4	mA mA mA mA	Vin=0 V, Vdd at 8 MHz Clock divided by 16 XTAL running ADC is off.
I_{CC2}	Standby Current (STOP Mode)	3.0 V 5.5 V		20 30	µA µA	Vin=0 V, Vdd; ADC is off. P43=1 or high impedance WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.
I_{ADC}	Current with A/D Running	3.0 V 5.5 V		500 900	µA µA	
V_{LV}	Vdd Low-Voltage Protection			2.90	V	Low voltage protection is also known as brownout. Typical is 2.6 V.
V_{LB}	Low-Battery Detection			VLV+ 0.5	V V	

Table 55. DC Characteristics for the Z86L99X (Mask Only)

Symbol	Parameter	V_{DD}	Min	Max	Units	Comments
V_{DD}	Power Supply Voltage		2.3	5.5		
V_{CH}	Clock Input High Voltage	2.3 V 5.5 V	0.8Vdd 0.8Vdd	Vdd+0.3 Vdd+0.3	V V	Driven by Ext. clock generator
V_{CL}	Clock Input Low Voltage	2.3 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd		Driven by Ext. clock generator
V_{IH}	Input High Voltage	2.3 V 5.5 V	0.7Vdd 0.7Vdd	Vdd+0.3 Vdd+0.3	V V	
V_{IL}	Input Low Voltage	2.3 V 5.5 V	Vss–0.3 Vss–0.3	0.2Vdd 0.2Vdd	V V	
V_{OH1}	Output High Voltage Regular I/O	2.3 V 5.5 V	2.0 5.0		V V	–0.5 mA
		2.3 V 5.5 V	1.9 5.0		V V	–1.2 mA
V_{OH2}	High Drive Pins (P54, P55, P56, P57)	2.3 V 5.5 V	1.9 5.1		V V	–3 mA
		2.3 V 5.5 V	1.7 4.7		V V	–5 mA
V_{OL1}	Regular I/O Output low voltage	2.3 V 5.5 V		0.4 V 0.4 V	V V	2 mA
		2.3 V 5.5 V		0.8 V 0.8 V	V V	4 mA
V_{OL2}	High Drive Pins (P54, P55, P56, P57)	2.3 V 5.5 V		0.4 V 0.4 V	V V	4 mA
		2.3 V 5.5 V		0.8 V 0.8 V	V V	7 mA
I_{CCO}	Controlled Current Output (P43)	2.3 V 5.5 V	70 70	120 120	mA mA	Vout = 1.2 V to VDD at room temperature (see Figure 17)
I_{IL}	Input Leakage	2.3 V 5.5 V	–1 –1	1 µA 1 µA	µA µA	Vin=0 V, Vdd Vin=0 V, Vdd
I_{CC}	Supply Current	2.3 V 5.5 V 2.3 V 5.5 V		3 8 250 850	mA mA µA µA	at 8 MHz at 8 MHz at 32 KHz at 32 KHz ADC is off.
I_{CC1}	Standby Current (Halt Mode)	2.3 V 5.5 V		2 5	mA mA	Vin=0 V, Vdd at 8 MHz
I_{CC2}	Standby Current (STOP Mode)	2.3 V 5.5 V		8 25.0	µA µA	Vin=0 V, Vdd;ADC is off. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.
I_{CC2}	Standby Current (STOP Mode)	5.5 V		15	µA	at 30 °C
I_{LV}	Standby Current (Low Voltage)			20	µA	Measured at V_{DD}=V_{LV}–0.2 V.
I_{ADC}	Current with A/D Running	2.3 V 5.5 V		500 900	µA µA	
V_{LV}	Vdd Low-Voltage Protection			2.2	V	Low voltage protection is also known as brownout. Typical is around 1.7 V at room temperature.
V_{LB}	Low-Battery Detection			3.0	V	Typical is around 2.4 V at room temperature.

Design Considerations

The Z8 uses a Pierce oscillator with an internal feedback circuit. The advantages of this circuit are low cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects.)

One drawback is the requirement for high gain in the amplifier to compensate for feedback path losses. Traces connecting crystal, capacitors, and the Z8 oscillator pins must be as short and wide as possible. Short and wide traces reduce parasitic inductance and resistance. The components (capacitors, crystal, and resistors) must be placed as close as possible to the oscillator pins of the Z8.

The traces from the oscillator pins of the integrated circuit (IC) and the ground side of the lead capacitors must be guarded from all other traces (clock, V_{CC}, and system ground) to reduce cross-talk and noise injection. Guarding the traces is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit and by placing a Z8 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead capacitors must be connected to a single trace to the Z8 V_{SS} (GND) pin. It must not be shared with any other system ground trace or components except at the Z8 device V_{SS} pin. Not sharing the ground side of the oscillator lead capacitors is to prevent differential system ground noise injection into the oscillator.

Ordering Information

Part	PSI	Description
Z86D99 (OTP)	Z86D990PZ008SC	40-pin PDIP
	Z86D990HZ008SC	48-pin SSOP
	Z86D991PZ008SC	28-pin PDIP
	Z86D991SZ008SC	28-pin SOIC
Z86L99 (Mask ROM)	Z86L990PZ008SC	40-pin PDIP
	Z86L990HZ008SC	48-pin SSOP
	Z86L991PZ008SC	28-pin PDIP
	Z86L991SZ008SC	28-pin SOIC
	Z86L996PZ008SC	28-pin PDIP
	Z86L996SZ008SC	28-pin SOIC
	Z86L997PZ008SC	28-pin PDIP
	Z86L997SZ008SC	28-pin SOIC
Emulator	Z86L9900100ZEM	Emulator/Programmer
Adapter	Z86D9900100ZDH	48 SSOP Adapter
Evaluation Board	Z86L9900100ZCO	Evaluation Board

For fast results, contact your local ZiLOG sale offices for assistance in ordering part(s). Updated information can be found on the ZiLOG website: HTTP://WWW.ZILOG.COM

Precharacterization Product

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