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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d991sz008sc00tr

Interrupts

The Z86D99/Z86L99 family allows up to six different interrupts, three external and three internal, from nine possible sources. The six interrupts are assigned as follows:

- Three edge-triggered external interrupts (P51, P52, and P53), two of which are shared with the two analog comparators
- One internal interrupt assigned to the T8 Timer
- One internal interrupt assigned to the T16 Timer
- One internal interrupt shared between the Low-Battery Detect flag and the T1 Timer

Table 3 presents the interrupt types, the interrupt sources, and the location of the specific interrupt vectors.

Table 3. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ_0	P52 (F/R), Comparator 2	0,1	External interrupt (P52) is triggered by either rising or falling edge; internal interrupt generated by Comparator 2 is mapped into IRQ_0
IRQ_1	P53 (F)	2,3	External interrupt (P53) is triggered by a falling edge
IRQ_2	P51 (R/F), Comparator 1	4,5	External interrupt (P51) is triggered by either a rising or falling edge; internal interrupt generated by Comparator 1 is mapped into IRQ_2
IRQ_3	T16 Timer	6,7	Internal interrupt
IRQ_4	T8 Timer	8,9	Internal interrupt
IRQ_5	LVD, T1 Timer	10,11	Internal interrupt, LVD flag is multiplexed with T1 Timer End-of-Count interrupt
Notes:	F = Falling-edge triggered; R = Rising-edge triggered. When LVD is enabled, IRQ5 is triggered only by low-voltage detection. Timer 1 does not generate an interrupt.		

These interrupts can be masked and their priorities set by using the Interrupt Mask Register (IMR) and Interrupt Priority Register (IPR) (Figure 8.) When more than one interrupt is pending, priorities are resolved by a priority encoder, controlled by the IPR.

start the interrupt process. However, the IPR does not have to be initialized for polled processing.

Interrupts must be globally enabled using the EI instruction. Setting bit 7 of the IMR is not sufficient. Subsequent to this EI instruction, interrupts can be enabled either by IMR manipulation or by use of the EI instruction, with equivalent effects.

Additionally, interrupts must be disabled by executing a DI instruction before the IPRs or IMRs can be modified. Interrupts can then be enabled by executing an EI instruction.

IRQ Software Interrupt Generation

IRQ can be used to generate software interrupts by specifying IRQ as the destination of any instruction referencing the Z8 Standard Register File. These Software Interrupts (SWIs) are controlled in the same manner as hardware-generated requests (the IPR and the IMR control the priority and enabling of each SWI level).

To generate a SWI, the request bit in the IRQ is set as follows:

```
OR    IRQ, #NUMBER
```

where the immediate data, *NUMBER*, has a 1 in the bit position corresponding to the appropriate level of the SWI.

For example, for an SWI on IRQ5, *NUMBER* has a 1 in bit 5. With this instruction, if the interrupt system is globally enabled, IRQ5 is enabled, and there are no higher priority pending requests, control is transferred to the service routine pointed to by the IRQ5 vector.

Reset Conditions

A system reset overrides all other operating conditions and puts the Z8 into a known state. The control and status registers are reset to their default conditions after a power-on reset (POR) or a Watch-Dog Timer (WDT) time-out while in RUN mode. The control and status registers are not reset to their default conditions after Stop Mode Recovery (SMR) while in HALT or STOP mode.

General-purpose registers are undefined after the device is powered up. Resetting the Z8 does not affect the contents of the general-purpose registers. The registers keep their most recent value after any reset, as long as the reset occurs in the specified V_{CC} operating range. Registers do not keep their most recent state from a V_{LV} reset, if V_{CC} drops below V_{RAM} (see Table 54 on page 87).

Following a reset (see Table 5), the first routine executed must be one that initializes the control registers to the required system configuration.

Table 5. Control and Status Register Reset Conditions

Register Function	Address Grp/Bnk	Register	Symbol	R/W	Reset Value 7	6	5	4	3	2	1	0
Register Pointer	F0h	r13 (R253)	RP	R/W	0	0	0	0	0	0	0	0
Stack Pointer	F0h	r15 (R255)	SP	R/W	X	X	X	X	X	X	X	X
Program Control Flags	F0h	r12 (R252)	Flags	R/W	X	X	X	X	X	X	X	X
Low Battery Detect	0Dh	r12	LB	R/W	1	1	1	1	1	X	0	0
ADC Control	0Fh	r8	ADCCTRL	R/W	0	0	0	0	0	0	0	0
ADC Data	00h	r7 (R7)	ADCDATA	R	0	0	0	0	0	0	0	0
Interrupt Mask	F0h	r11 (R251)	IMR	R/W	0	0	0	0	0	0	0	0
Interrupt Priority	F0h	r9 (R249)	IPR	W	0	0	0	0	0	0	0	0
Interrupt Request	F0h	r10 (R250)	IRQ	R/W	0	0	0	0	0	0	0	0
Port Configuration (A)	0Fh	r0	P456CON	R/W	0	0	0	0	0	1	1	1
Port Configuration (B)	F0h	r7 (R247)	P3M	W	1	1	1	1	1	1	1	1
Port 2 Data	00h	r2 (R2)	P2	R/W	X	X	X	X	X	X	X	X
Port 2 Mode	F0h	r6 (R246)	P2M	W	1	1	1	1	1	1	1	1
Port 4 Data	00h	r4 (R4)	P4	R/W	X	X	X	X	X	X	X	X
Port 4 Mode	0Fh	r2	P4M	R/W	1	1	1	1	1**	1	1	1
Port 5 Data	00h	r5 (R5)	P5	R/W	X	X	X	X	X	X	X	X
Port 5 Mode	0Fh	r4	P5M	R/W	1	1	1	1	1	1	1	1
Port 6 Data	00h	r6 (R6)	P6	R/W	X	X	X	X	X	X	X	X
Port 6 Mode	0Fh	r6	P6M	R/W	1	1	1	1	1	1	1	1
T1 Timer Data	F0h	r2 (R242)	T1	R/W	0	0	0	0	0	0	0	0
T1 Timer Mode	F0h	r1 (R241)	TMR	R/W	0	0	0	0	0	0	1	1
T1 Timer Prescale	F0h	r3 (R243)	PRE1	R/W	0	0	0	0	0	0	0	0
T8/T16 Control (A)	0Dh	r1	CTR1	R/W	0	0	0*	0*	0	0	0	0
T8/T16 Control (B)	0Dh	r3	CTR3	R/W	0	0	0*	X	X	X	X	X
T8 Timer Control	0Dh	r0	CTR0	R/W	0	0	0*	0*	0*	0*	0*	0
T8 High Capture	0Dh	r11	HI8†	RW	0	0	0	0	0	0	0	0
T8 Low Capture	0Dh	r10	LO8†	R/W	0	0	0	0	0	0	0	0
T8 High Load	0Dh	r5	TC8H†	R/W	0	0	0	0	0	0	0	0
T8 Low Load	0Dh	r4	TC8L†	R/W	0	0	0	0	0	0	0	0
T16 Timer Control	0Dh	r2	CTR2	R/W	0	0	0	0	0	0	0	0
T16 High Capture	0Dh	r9	HI16†	R/W	0	0	0	0	0	0	0	0
T16 Low Capture	0Dh	r8	LO16†	R/W	0	0	0	0	0	0	0	0
T16 High Load	0Dh	r7	TC16H†	R/W	0	0	0	0	0	0	0	0
T16 Low Load	0Dh	r6	TC16L†	R/W	0	0	0	0	0	0	0	0

instruction pipeline by executing a NOP (Op Code = FFh) immediately before the appropriate sleep instruction. For example:

Mnemonic	Comment	Op Code
NOP	; clear the pipeline	FFh
STOP	; enter STOP mode	6Fh

or

Mnemonic	Comment	Op Code
NOP	; clear the pipeline	FFh
HALT	; enter HALT mode	7Fh

HALT

HALT mode suspends instruction execution and turns off the internal CPU clock (SCLK). The on-chip oscillator circuit remains active, so the internal Timer clock (TCLK) continues to run and is applied to the counter/timers and interrupt logic.

An interrupt request, either internally or externally generated, must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction immediately following the HALT.

The HALT mode can also be exited by a POR. In this case, the program execution restarts at the reset address 000Ch.

STOP

STOP mode provides the lowest possible device standby current. This instruction turns off both the internal CPU clock (SCLK) and internal Timer clock (TCLK) and reduces the standby current to the minimum.

The STOP mode is terminated by a POR or SMR source. Terminating the STOP mode causes the processor to restart the application program at address 000Ch.

Note: When the STOP instruction is executed, the microcontroller goes into the STOP mode despite any state/change of the state of the port. The ports need to be checked immediately before the NOP and STOP instructions to ensure the right input logic before waiting for the change of the ports.

Stop Mode Recovery Sources

Exiting STOP mode using an SMR source is greatly simplified in the Z86D99/Z86L99 family. The Z86D99/Z86L99 family of products allows 16 individual I/O

Peripherals

Analog Comparators

The Z86D99/Z86L99 family includes two independent on-chip general-purpose analog comparators as shown in Figure 13. The comparators are multiplexed with a digital input signal by the P456CON register. They can also be used to generate interrupts IRQ0 and IRQ2. The comparators are turned off in STOP mode.

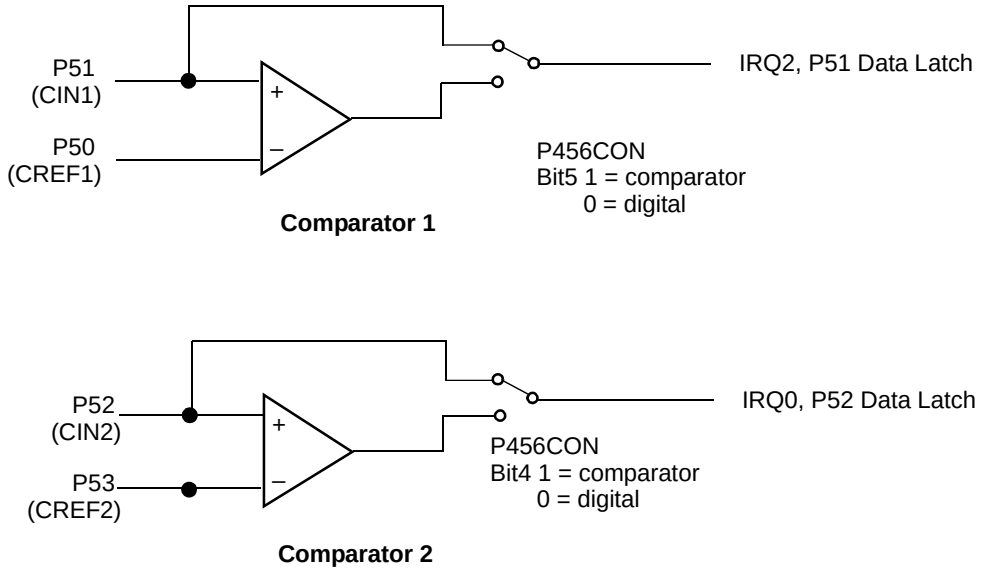

Figure 13. Analog Comparators

Analog/Digital Converter (ADC)

The Z86D99/Z86L99 family incorporates an 8-bit ADC that uses a sigma delta architecture (Figure 14) comprised of a modulator and a digital filter. The input is selected (bit 3,2 from ADCCTRL) with an analog mux from 4 (P47–P44) pins that can be configured as analog inputs (bit 7–4 from ADCCTRL).

Note: Whenever an input pin has an analog value, the digital input buffer has to be disabled in order to reduce the current through the device.

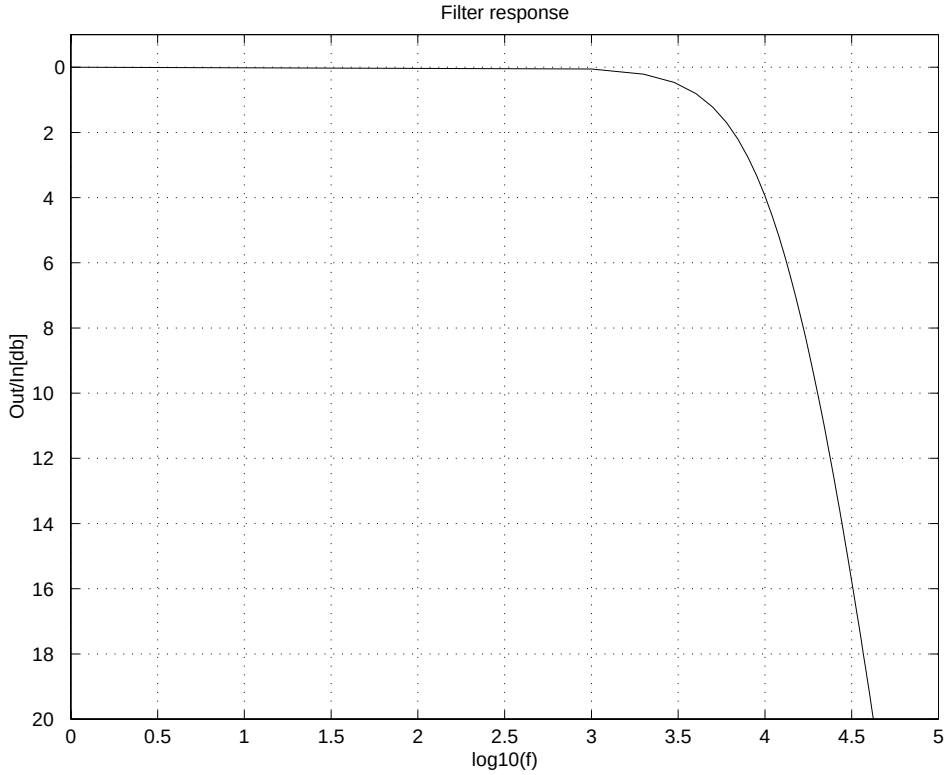

Figure 15. Low-Pass Filter (with 8-MHz Crystal)

The sampling frequency of the modulator f_{ADC} can be selected between f_{SCLK} and $f_{SCLK}/2$ (bit1 from ADCCTRL). Reducing the clock frequency lowers the power dissipated in the ADC block.

The ADC can be enabled or disabled. When enabled, the ΣΔ converter tracks the input voltage. When switching between the channels (step response), the required time to reach the final value is given by the time constant of the low-pass filter:

$$T_{delay} = \frac{2}{f_{3db}} = \frac{2}{0.0021 f_{ADC}} = \frac{952}{f_{ADC}}$$

When available, the reference for the ADC is set externally with the V_{ref+} and V_{ref-} pins. The output code represents the following ratio:

$$D_{out} = \frac{V_{in} - V_{Ref-}}{V_{Ref+} - V_{Ref-}} \times 256$$

Counter/timer 1 is driven by a timer clock generated by dividing the internal clock by four. The divide-by-four stage, the 6-bit prescaler, and the 8-bit counter/timer form a synchronous 16-bit divide chain. Counter/timer T_1 can also be driven by an external input (T_{IN}) using Port P52. Port $P5_6$ can serve as a timer output (T_{OUT}) through which T_1 or the internal clock can be output. The timer output toggles at the end-of-count. Figure 18 is a block diagram of the counter/timer.

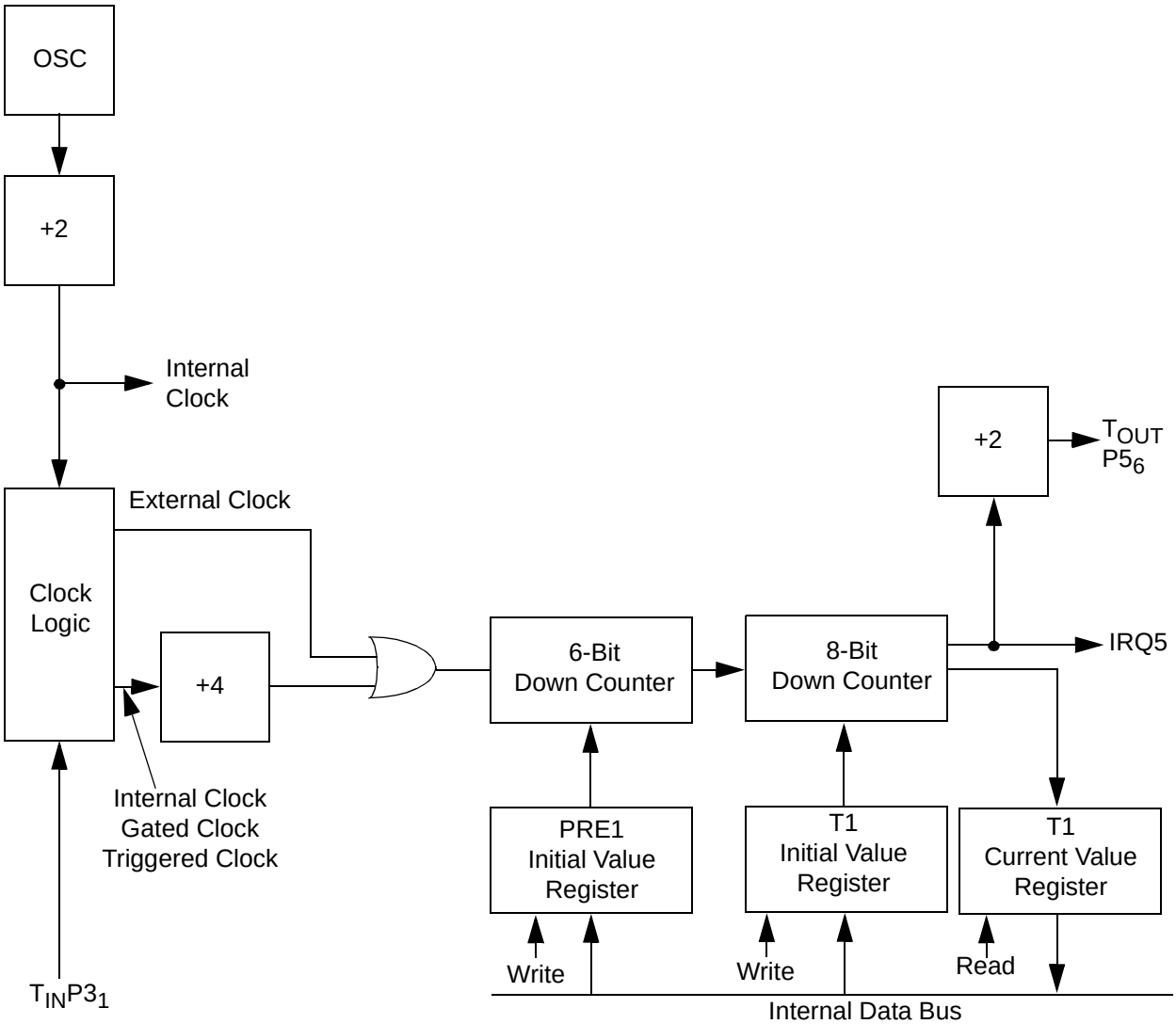

Figure 18. T_1 Counter/Timer Block Diagram

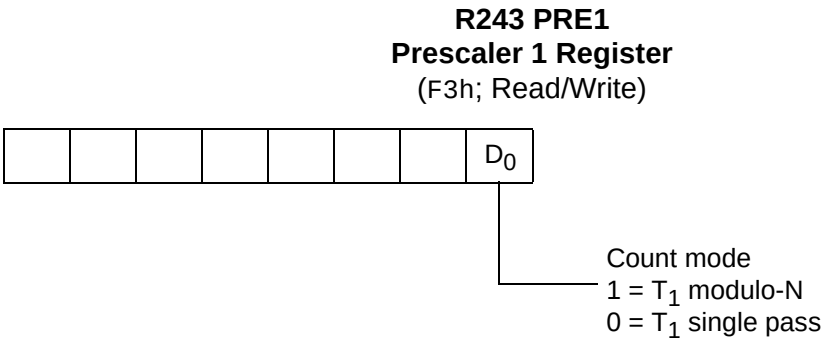

Figure 24. Counting Modes

When the PRE_1 register is loaded with 000000 in the six most significant bits, the prescaler divides by 64. If that number is 000001, the prescaler does not divide and passes its clock on to T_1.

Each time the prescaler reaches its end-of-count, a carry is generated, which allows the counter/timer to decrement by one on the next timer clock input. When T_1 and PRE_1 both reach their end-of-count, an interrupt request is generated—IRQ_5 for T_1. Depending on the counting mode selected, the counter/timer either comes to rest with its value at 00h (single-pass mode), or the initial value is automatically reloaded and counting continues (continuous mode). In single-pass mode, the prescaler still continues to decrement when the timer T_1 has reached its end-of-count. The prescaler always starts from its programmed value upon restarting the counter.

The counting modes are controlled by bit D_0 of PRE_1, with D_0 cleared to 0 for single-pass counting mode or set to 1 for continuous mode.

The counter/timer can be stopped at any time by setting the Enable Count bit to 0 and restarted by setting the Enable Count bit back to 1. The T_1 counter/timer continues its count value at the time it was stopped. The current value in the T_1 counter/timer can be read at any time without affecting the counting operation.

New initial values can be written to the prescaler or the counter/timer registers at any time. These values are transferred to their respective down-counters on the next load operation. If the counter/timer mode is continuous, the next load occurs on the timer clock following an end-of-count. New initial values must be written before the load operation because the prescaler always effectively operates in continuous count mode.

If the value loaded in the T_1 register is 01h, the timer is actually not timing or counting at all; the timer is passing the prescaler end-of-count through. Because the prescaler is continuously running, regardless of the single-pass/continuous mode operation, the 8-bit timer continuously times out at the rate of the prescaler end-of-count if the T_1 timer value is programmed to 01h.

The time interval (i) until end-of-count, is given by

i = t x p x v

where t is 8 divided by XTAL frequency, p is the prescaler value (1 – 64), and v is the counter/timer value (1 – 256). The prescaler and counter/timer are true divide-by-n counters.

T_{OUT} Modes

The Timer Mode register TMR (F1h) (Figure 25) is used in conjunction with the Port 5 Mode register P5M to configure $P5_6$ for T_{OUT} operation. In order for T_{OUT} to function, $P5_6$ must be defined as an output line by setting P5M bit D_6 to 0. Output is controlled by one of the counter/timers (T_0 or T_1) or the internal clock.

R241 TMR
Timer Mode Register
(F1h; Read/Write)

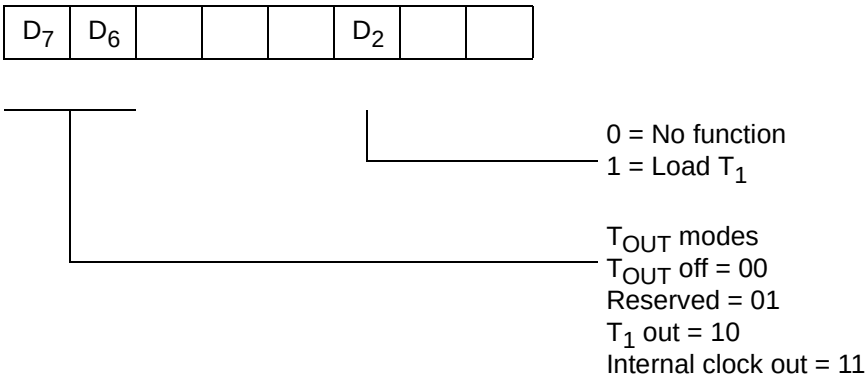

Figure 25. Timer Mode Register T_{OUT} Operation

The $P5_6$ output is selected by TMR bits D_7 and D_6. T_1 is selected by setting D_7 and D_6 to 1 and 0, respectively. The counter/timer T_{OUT} mode is turned off by setting TMR bits D_7 and D_6 both to 0, freeing $P3_6$ to be a data output line.

T_{OUT} is initialized to a logic 1 whenever the TMR Load bit D_2 is set to 1.

At end-of-count, the interrupt request line IRQ_5 clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line $P5_6$. In all cases, when the counter/timer reaches its end-of-count, T_{OUT} toggles to its opposite state (see Figure 26). If, for example, the counter/timer is in continuous counting mode, T_{OUT} has a 50% duty cycle output. You can control the duty cycle by varying the initial values after each end-of-count.

T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5), and generates an interrupt if enabled (CTR0 D1). This completes one cycle. T8 then loads from TC8H or TC8L, according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time.The new values take effect when they are loaded. Do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed. An initial count of 0 causes TC8 to count from 0 to FFh to FEh. Transition from 0 to FFh is not a time-out condition (see Figure 34).

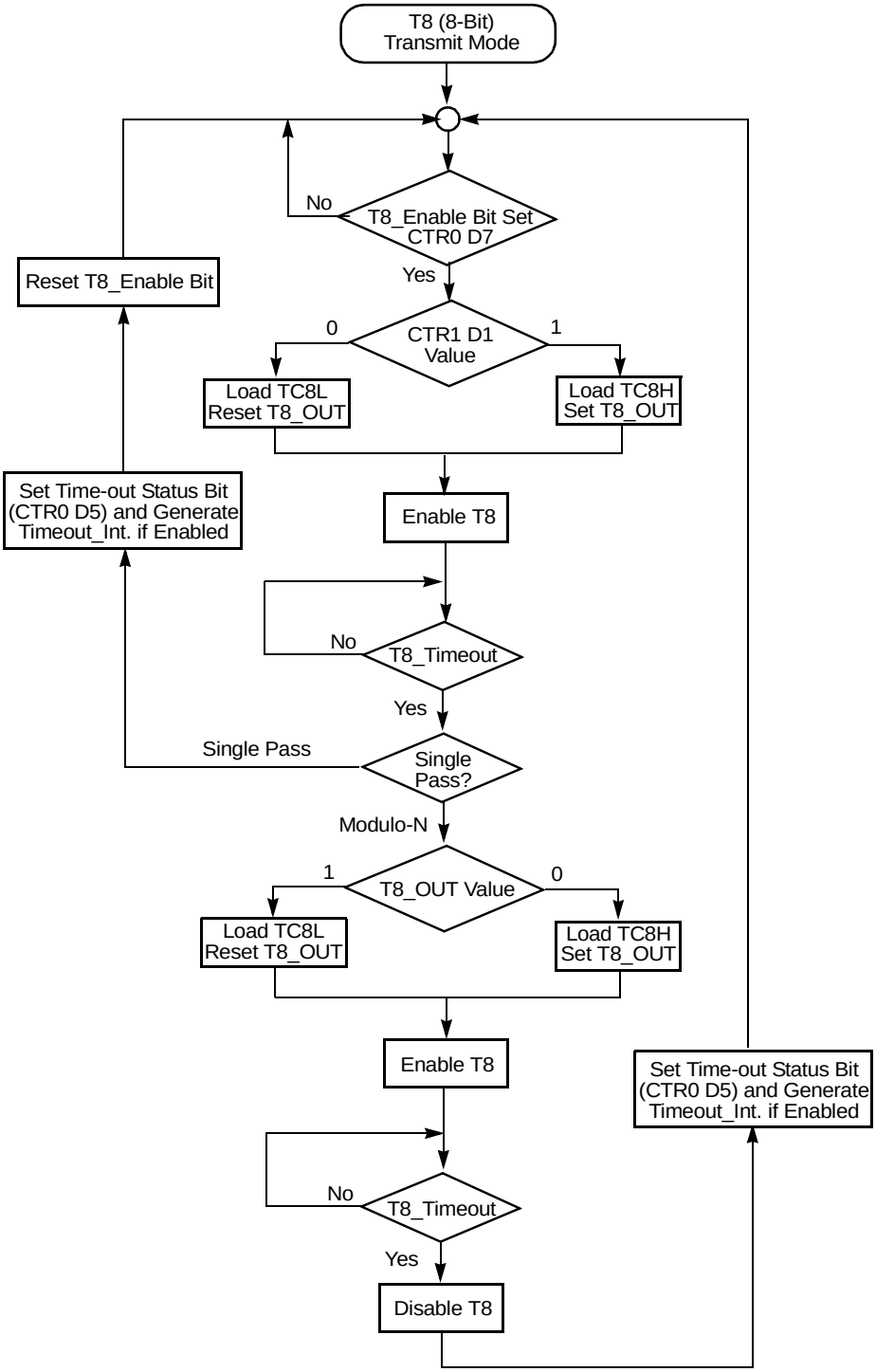

Figure 34. Transmit Mode Flowchart

Control and Status Registers

The Z86D99/Z86L99 family has 4 I/O port registers, 33 status and control registers, and 233 general-purpose RAM registers. The I/O port and control registers are included in the general-purpose register memory to allow any Z8 instruction to process I/O or control information directly, thus eliminating the requirement for special I/O or control instructions. The Z8 instruction set permits direct access to any of these 37 registers. In addition, each of the 233 general-purpose registers can also function as an accumulator, an address pointer, or an index register. Registers identified as “Reserved” do not exist or have not been implemented in this design.

Register Summary

Table 10 through Table 13 summarize the name and location of all registers. The register-by-register descriptions follow this section.

Table 10. I/O Port Registers (Group 0, Bank 0, Registers 0–F)

Grp/Bnk Reg		Register Function	Identifier
(00h)	rF	General-Purpose RAM Register	GPR
(00h)	rE	General-Purpose RAM Register	GPR
(00h)	rD	General-Purpose RAM Register	GPR
(00h)	rC	General-Purpose RAM Register	GPR
(00h)	rB	General-Purpose RAM Register	GPR
(00h)	rA	General-Purpose RAM Register	GPR
(00h)	r9	General-Purpose RAM Register	GPR
(00h)	r8	General-Purpose RAM Register	GPR
(00h)	r7	Analog/Digital Converted Data	ADCDATA
(00h)	r6	Port 6 Control Register	P6
(00h)	r5	Port 5 Control Register	P5
(00h)	r4	Port 4 Control Register	P4
(00h)	r3	Reserved	
(00h)	r2	Port 2 Control Register	P2
(00h)	r1	Reserved	
(00h)	r0	Reserved	

Table 14. Register Description Locations (Continued)

Address Grp/Bnk Register		Register Function	Symbol	Location
0Dh	r11	T8 High Capture	HI8†	page 78
0Dh	r12	Low Battery Detect	LB	page 60
0Fh	r0	Port Configuration (A)	P456CON	page 67
0Fh	r1	Port 2 SMR Source	P2SMR	page 84
0Fh	r2	Port 4 Mode	P4M	page 69
0Fh	r4	Port 5 Mode	P5M	page 70
0Fh	r5	Port 5 SMR Source	P5SMR	page 84
0Fh	r6	Port 6 Mode	P6M	page 71
0Fh	r8	ADC Control	ADCCTRL	page 61
0Fh	r11	Stop Mode Recovery	SMR	page 83
F0h	r1 (R241)	T1 Timer Mode	TMR	page 72
F0h	r2 (R242)	T1 Timer Data	T1	page 72
F0h	r3 (R243)	T1 Timer Prescale	PRE1	page 73
F0h	r6 (R246)	Port 2 Mode	P2M	page 68
F0h	r7 (R247)	Port Configuration (B)	P3M	page 67
F0h	r9 (R249)	Interrupt Priority	IPR	page 64
F0h	r10 (R250)	Interrupt Request	IRQ	page 65
F0h	r11 (R251)	Interrupt Mask	IMR	page 63
F0h	r12 (R252)	Program Control Flags	Flags	page 57
F0h	r13 (R253)	Register Pointer	RP	page 58
F0h	r15 (R255)	Stack Pointer	SP	page 59

Note: †This register is not reset following Stop Mode Recovery (SMR).

Flags and Pointer Registers

In addition to the three standard Z8 flag and pointer registers (Program Control Register Pointer, and Stack Pointer), the Z86D99/Z86L99 family includes a Low-Battery Detect Flag register.

Low-Battery Detect Flag (LB)

When the Z86D99/Z86L99 is used in a battery-operated application, one of the on-chip comparators can be used to check that the V_{CC} is at the required level for correct operation of the device. When voltage begins to approach the V_{BO} point, an on-chip low-battery detection circuit is tripped, which in turn sets a user-readable flag. The LB register, as described in Table 18, is used to set and reset the LB flag.

Table 18. LB Register (Group/Bank 0Dh, Register C)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Reserved					Pad LVD	LVD_ Flag	LVD_ Enable
R/W	W	W	W	W	W	R/W	R/W	R/W
Reset	1	1	1	1	1	X	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543___	Reserved	R	1	Always reads 11111
		W	X	No Effect
_____2__	Pad LVD	R	1	Pad is not regulated when P43=0 (V_{pad}<V_{min}; see page 33)
		R	0	Pad is regulating the current when P43=0 (V_{pad}>V_{min}; see page 33)
		W	X	Reset Pad LB flag
______1_	LVD_Flag	R	1	LB Flag Set if V_{DD}<V_{LV}
		R	0	LB Flag Reset
		W	X	No Effect
_______0	LVD_Enable	R/W	1	Enable LB *
			0	Disable LB

Note: * When LVD is enabled, IRQ5 is set only for low-voltage detection. Timer 1 will not generate an interrupt request.

Note: The LB flag will be valid after enabling the detection for 20 µS (design estimation, not tested in production). LB does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

Interrupt Request Register

The IRQ, as described in Table 23, is a read/write register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt request is made by any of the six interrupts, the corresponding bit in the IRQ is set to 1.

Table 23. IRQ (Group/Bank 0Fh, Register A)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Interrupt Edge		Set IRQ5	Set IRQ4	Set IRQ3	Set IRQ2	Set IRQ1	Set IRQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	Interrupt Edge Trigger	R/W	11 10 01 00	P51 Rise/FallingP52 Rise/Falling P51 Rising P52 Falling P51 FallingP52 Rising P51 FallingP52 Falling
__5_____	Set IRQ_5	R R W W	1 0 1 0	IRQ_5 Inactive IRQ_5 Active Set IRQ_5 Reset IRQ_5
___4____	Set IRQ_4	R R W W	1 0 1 0	IRQ_4 Inactive IRQ_4 Active Set IRQ_4 Reset IRQ_4
____3___	Set IRQ_3	R R W W	1 0 1 0	IRQ_3 Inactive IRQ_3 Active Set IRQ_3 Reset IRQ_3
_____2__	Set IRQ_2	R R W W	1 0 1 0	IRQ_2 Inactive IRQ_2 Active Set IRQ_2 Reset IRQ_2
______1_	Set IRQ_1	R R W W	1 0 1 0	IRQ_1 Inactive IRQ_1 Active Set IRQ_1 Reset IRQ_1
_______0	Set IRQ_0	R R W W	1 0 1 0	IRQ_0 Inactive IRQ_0 Active Set IRQ_0 Reset IRQ_0

Table 25. P3M Register [Group/Bank F0h, Register 7 (R247)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	Reserved							P2_ Output
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7654321_	Reserved	R	1	Always reads 1111111
		W	X	No Effect
_____0	Port 2 Output Configuration	W	1	Push-Pull Active
			0	Open Drain Outputs

Port 2 Control and Mode Registers (P2 and P2M)

Port 2 is a general-purpose 8-bit, bidirectional I/O port, as shown in Table 26. Each of the eight Port 2 I/O lines can be independently programmed as either input or output using the Port 2 Mode Register (see Table 27.)

Table 26. P2 Register [Group/Bank 00h, Register 2 (R2)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	Port 2 Data							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	Port 2 Data	R/W	Data	Port 2 Input/Output Register

Table 27. P2M Register [Group/Bank F0h, Register 6 (R246)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	P27M	P26M	P25M	P24M	P23M	P22M	P21M	P20M
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210 (by bit)	Port 2 Mode Select	R	1	Always reads 11111111
		W	1	Input
		W	0	Output

A bit set to 1 in the P2M Register configures the corresponding bit in Port 2 as an input, while a bit set to 0 configures an output line.

Port 4 Control and Mode Registers (P4 and P4M)

Port 4 is a general-purpose 8-bit, bidirectional I/O port, as shown in Table 28. Each of the eight Port 4 I/O lines can be independently programmed as either input or output using the Port 4 Mode Register (see Table 29.)

Table 28. P4 Register [Group/Bank 00h, Register 4 (R4)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**Port 4 Data**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	Port 4 Data	R/W	Data	Port 4 Input/Output Register

Table 29. P4M Register (Group/Bank 0Fh, Register 2)

Bit	7	6	5	4	3	2	1	0
Bit/Field	**P47M**	**P46M**	**P45M**	**P44M**	**P43M**	**P42M**	**P41M**	**P40M**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7654_210 (by bit)	Port 4 Mode Select	R/W	1 0	Input Output
____3___	P43 Mode Select	R/W	0 1	Output Tristate High Impedance (available on Z86L990/L991 only)

A bit set to 1 in the P4M Register configures the corresponding bit in Port 4 as an input, while a bit set to 0 configures an output line.

Note: P43, the controlled current output pad, cannot be configured as an input. (P43 read = P43 out)

T1 Data Register (T1)

The counter/timer register (T1) consists of an 8-bit down counter, a write-only register that holds the initial count value, and a read-only register that holds the current count value. The initial value of T1 can range from 1 to 255 (0 represents 256) (see Table 34.)

Table 34. T1 Register [Group/Bank F0h, Register 2 (R242)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**T1_Value**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_1 Value	R	Data	Current Value
		W	Data	Initial Value (Range 1 to 256 Decimal)

T1 Mode Register (TMR)

Under software control, T1 counter/timer is started and stopped using the T1 Mode Register as shown in Table 35.

Table 35. TMR Register [Group/Bank F0h, Register 1 (R241)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**TOUT_Mode**		**TIN_Mode**		**T1_ Count**	**T1_ Load**	**Reserved**	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	T_{OUT} Mode	R/W	11	Internal Clock OUT on P56
			10	T_1OUT on P56
			01	Reserved
			00	Not used (P56 configured as I/O)
__54____	T_{IN} Mode	R/W	11	Trigger Input (Retriggerable)
			10	Trigger Input (Not-retriggerable)
			01	Gate Input
			00	External Clock Input (T_{IN} on P52)
____3___	T_1 Count	R/W	1	Enable T_1 Count
			0	Disable T_1 Count

consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

Port 2 Stop Mode Recovery (P2SMR)

The P2SMR register, as described in Table 51, defines which I/O lines in Port 2 are to be used as stop mode recovery sources.

Table 51. P2SMR Register (Group/Bank 0Fh, Register 1)

Bit	7	6	5	4	3	2	1	0
Bit/Field	**P27RS**	**P26RS**	**P25RS**	**P24RS**	**P23RS**	**P22RS**	**P21RS**	**P20RS**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210 (by bit)	Port 2 Stop Mode Recovery	R/W	1 0	Recovery Source Not

Port 5 Stop-Mode Recovery (P5SMR)

The P5SMR register, as described in Table 52, defines which I/O lines in Port 5 are to be used as stop-mode recovery sources.

Table 52. P5SMR Register (Group/Bank 0Fh, Register 5)

Bit	7	6	5	4	3	2	1	0
Bit/Field	**P57RS**	**P56RS**	**P55RS**	**P54RS**	**P53RS**	**P52RS**	**P51RS**	**P50RS**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210 (by bit)	Port 5 Stop Mode Recovery	R/W	1 0	Recovery Source Not

the ADC input mode, the switching capacitor starts to charge up from 0 V. For the maximum swing (Dout = 0 to FF), it takes 2/(0.0021x f ADC). For an 8-MHz MCU crystal (with clock divide-by-two mode), the internal system clock is 4 MHz. In ADCCTRL, if you select the ADC frequency = system clock divided by 1 option, f ADC = 4 MHz. The step response = 238 uS.

AC Characteristics

Table 57 lists the AC characteristics.

Table 57. AC Characteristics

No.	Symbol	Parameter	VDD	Min	Max	Units
1	TpC	Input Clock Period	2.3 V 5.5 V	120 120	DC DC	ns
2	TrC, TfC	Clock Input Rise and Fall Times	2.3 V 5.5 V		25 ns 25 ns	
3	TwC	Input Clock Width	2.3 V 5.5 V	5.0 5.0		ns ns
4	TwTinL	Timer Input Low Width	2.3 V 5.5 V	2TPC 2TPC		 ns
5	TwTinH	Timer Input High Width	2.3 V 5.5 V	2 2		TpC TpC
6	TpT1in	Timer 1 Input Period	2.3 V 5.5 V	8 8		TpC TpC
7	TrTin, TfTin	Timer Input Rise and Fall Time	2.3 V 5.5 V		100 100	ns ns
8	TwIL	Interrupt Request Low Time	2.3 V 5.5 V	100 70		ns ns
9	TwIH	Interrupt Request Input High Time	2.3 V 5.5 V	5 5		TpC TpC
10	Twsm	Stop-Mode Recovery Width Spec	2.3 V 5.5 V	12 12		ns ns
12	Twdt	Watch-Dog Timer Time Out	2.3 V 5.5 V	25 10		ms ms