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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	489 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d991sz008sg

List of Tables

- Interrupt Control (IPR, IMR, and IRQ)
- Stop Mode Recovery (SMR, P2SMR, and P5SMR)
- Low-Battery Detect (LB) Flag

The Z8 uses a 16-bit Program Counter (PC) to determine the sequence of current program instructions. The PC is not an addressable register.

Peripheral registers are used to transfer data, configure the operating mode, and control the operation of the on-chip peripherals. Any instruction that references the register file can access the peripheral registers. The following are peripheral control registers:

- Analog/Digital Converter (ADCCTRL and ADCDATA)
- T1 Timer/Counter (TMR, T1, and PRE1)
- T8 Timer/Counter (CTR0, HI8, LO8, TC8H, and TC8L)
- T16 Timer/Counter (CTR2, HI16, LO16, TC16H, and TC16L)
- T8/T16 Control Registers (CTR1and CTR3)

In addition, the four port registers are considered to be peripheral registers. The following are port control registers:

- Port Configuration Registers (P456CON and P3M)
- Port 2 Control and Mode Registers (P2 and P2M)
- Port 4 Control and Mode Registers (P4 and P4M)
- Port 5 Control and Mode Registers (P5 and P5M)
- Port 6 Control and Mode Registers (P6 and P6M)

The functions and applications of the control and peripheral registers are explained in “Control and Status Registers” on page 52.

Memory (ROM/OTP and RAM)

There are four basic address spaces available to support a wide range of configurations:

- Program memory (on-chip)
- Standard register file
- Expanded register file
- Executable RAM

The Z8 standard register file totals up to 256 consecutive bytes organized as 16 groups of 16 eight-bit registers. These registers consist of I/O port registers,

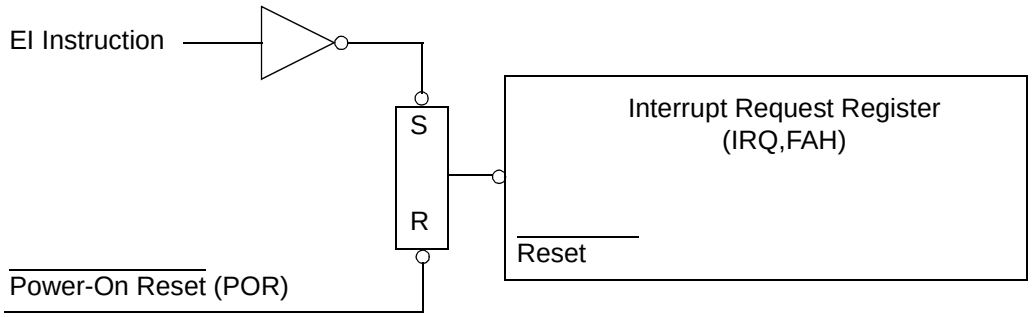


Figure 8. Interrupt Block Diagram

Interrupt requests are stored in the Interrupt Request Register (IRQ), which can also be used for polling. When an interrupt request is granted, the Z8 enters an "interrupt machine cycle" that globally disables all other interrupts, saves the program counter (the address of the next instruction to be executed) and status flags, and finally branches to the vector location for the interrupt granted. It is only at this point that control passes to the interrupt service routine for the specific interrupt.

All six interrupts can be globally disabled by resetting the master Interrupt Enable (bit 7 of the IMR) with a Disable Interrupts (DI) instruction. Interrupts are globally enabled by setting the same bit with an Enable Interrupts (EI) instruction.

Descriptions of three interrupt control registers—the Interrupt Request Register, the Interrupt Mask Register, and the Interrupt Priority Register—are provided in "Register Summary" on page 52. The Z8 family supports both vectored and polled interrupt handling.

External Interrupt Sources

External sources involve interrupt request lines P51, P52, and P53 (IRQ_2, IRQ_0, and IRQ_1, respectively.) IRQ_0, IRQ_1, and IRQ_2 are generated by a transition on the corresponding port pin. As shown in Figure 9, when the appropriate port pin (P51, P52, or P53) transitions, the first flip-flop is set. The next two flip-flops synchronize the request to the internal clock and delay it by two internal clock periods. The output of the most recent flip-flop (IRQ_0, IRQ_1, or IRQ_2) sets the corresponding Interrupt Request Register bit.

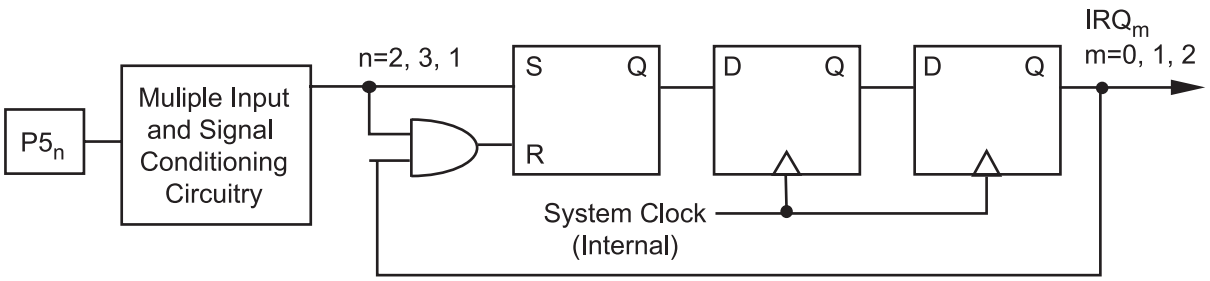


Figure 9. External Interrupt Sources IRQ_0–IRQ_2 Block Diagram

The programming bits for the Interrupt Edge Select function are located in the IRQ register, bits 6 and 7. The configuration of these bits and the resulting interrupt edge is shown in Table 4.

Table 4. Interrupt Edge Select for External Interrupts

Interrupt Request Register		Interrupt Edge	
Bit 7	Bit 6	IRQ_2 (P51)	IRQ_0 (P52)
0	0	Falling	Falling
0	1	Falling	Rising
1	0	Rising	Falling
1	1	Rising/Falling	Rising/Falling

Note: Although interrupts are edge triggered, minimum interrupt request Low and High times must be observed for proper operation. See “Electrical Characteristics” on page 85 for exact timing requirements (T_WIL, T_WIH) on external interrupt requests.

Internal Interrupt Sources

Internal sources are ORed with the external sources, so that either an internal or external source can trigger the interrupt.

Interrupt Request Register Logic and Timing

Figure 10 shows the logic diagram for the Interrupt Request Register. The leading edge of an interrupt request sets the first flip-flop. It remains set until the interrupt requests are sampled.

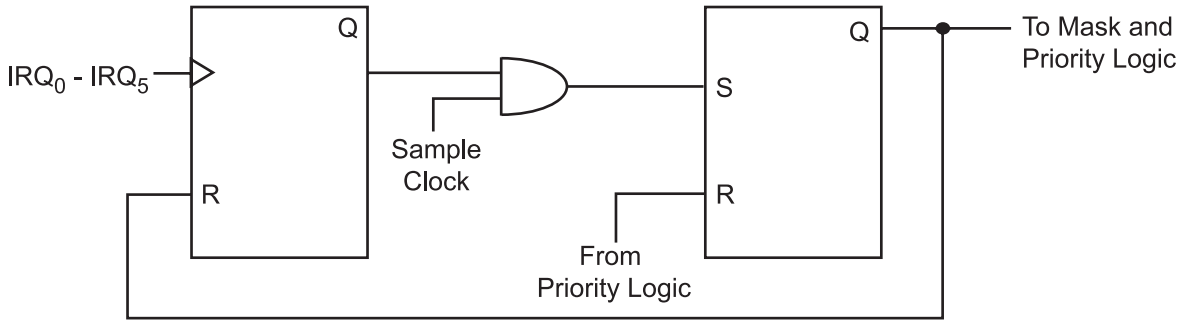


Figure 10. IRQ Logic

Internal interrupt requests are sampled during the most recent clock cycle before an Op Code fetch (see Figure 11.) External interrupt requests are sampled two internal clocks earlier than internal interrupt requests because of the synchronizing flip-flops shown in Figure 9.

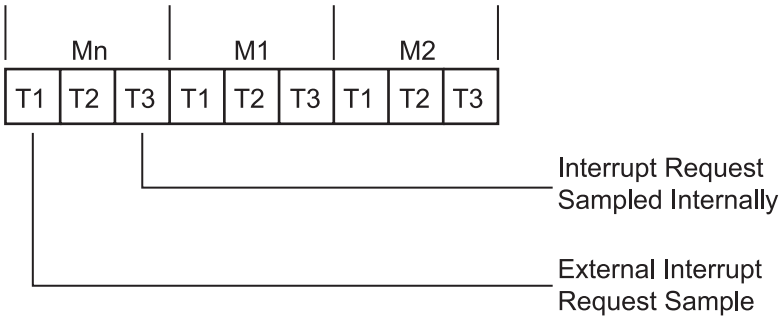


Figure 11. Interrupt Request Timing

At sample time, the interrupt request is transferred to the second flip-flop shown in Figure 10, which drives the interrupt mask and priority logic. When an interrupt cycle occurs, this flip-flop is reset only for the highest priority level that is enabled.

The user has direct access to the second flip-flop by reading and writing to the IRQ. The IRQ is read by specifying it as the source register of an instruction, and the IRQ is written by specifying it as the destination register.

Interrupt Initialization

After RESET, all interrupts are disabled and must be re-initialized before vectored or polled interrupt processing can begin. The Interrupt Priority Register, Interrupt Mask Register, and Interrupt Request Register must be initialized, in that order, to

start the interrupt process. However, the IPR does not have to be initialized for polled processing.

Interrupts must be globally enabled using the EI instruction. Setting bit 7 of the IMR is not sufficient. Subsequent to this EI instruction, interrupts can be enabled either by IMR manipulation or by use of the EI instruction, with equivalent effects.

Additionally, interrupts must be disabled by executing a DI instruction before the IPRs or IMRs can be modified. Interrupts can then be enabled by executing an EI instruction.

IRQ Software Interrupt Generation

IRQ can be used to generate software interrupts by specifying IRQ as the destination of any instruction referencing the Z8 Standard Register File. These Software Interrupts (SWIs) are controlled in the same manner as hardware-generated requests (the IPR and the IMR control the priority and enabling of each SWI level).

To generate a SWI, the request bit in the IRQ is set as follows:

```
OR    IRQ, #NUMBER
```

where the immediate data, *NUMBER*, has a 1 in the bit position corresponding to the appropriate level of the SWI.

For example, for an SWI on IRQ5, *NUMBER* has a 1 in bit 5. With this instruction, if the interrupt system is globally enabled, IRQ5 is enabled, and there are no higher priority pending requests, control is transferred to the service routine pointed to by the IRQ5 vector.

Reset Conditions

A system reset overrides all other operating conditions and puts the Z8 into a known state. The control and status registers are reset to their default conditions after a power-on reset (POR) or a Watch-Dog Timer (WDT) time-out while in RUN mode. The control and status registers are not reset to their default conditions after Stop Mode Recovery (SMR) while in HALT or STOP mode.

General-purpose registers are undefined after the device is powered up. Resetting the Z8 does not affect the contents of the general-purpose registers. The registers keep their most recent value after any reset, as long as the reset occurs in the specified V_{CC} operating range. Registers do not keep their most recent state from a V_{LV} reset, if V_{CC} drops below V_{RAM} (see Table 54 on page 87).

Following a reset (see Table 5), the first routine executed must be one that initializes the control registers to the required system configuration.

Special Functions

Table 7 defines the special functions of Ports 4 and 5.

Table 7. Special Port Pin Functions

Function	Pin	Signal	Configuration Register
Analog Comparator Inputs	P51	CIN1	P456CON
	P52	CIN2	P456CON
Analog Comparator References	P50	CREF1	
	P53	CREF2	
Analog Comparator Outputs	P54	COUT1	
	P55	COUT2	
ADC Channels	P44	ADC0	ADCCTRL
	P45	ADC1	ADCCTRL
	P46	ADC2	ADCCTRL
	P47	ADC3	ADCCTRL
External Interrupts	P52	IRQ_0	IMR and IRQ
	P53	IRQ_1	IMR and IRQ
	P51	IRQ_2	IMR and IRQ
T_{IN} External Clock Input	P52	T_{IN}	TMR and PRE1
Capture Timer Input	P51	Demodulator_Input	CTR1
T1 Timer Output	P56	T1OUT	TMR
T8 Output	P40	P40_Out	CTR0
T16 Output	P41	P41_Out	CTR2
Combined T8/T16 Output Controlled Current Output	P43	P43_Out	CTR1
ZiLOG Test Mode	P41	DSn Enable	P456CON
	P42	ASn Enable	P456CON

Controlled Current Output

P43 is an open-drain output-only pin on the Z86D990/D991, but it can be configured as output or Tristate High Impedance on the Z86L990/L991. To function properly, Bit 3 of P4M must be set to zero to configure the pin as an open-drain output. For the Z86L990/L991 after reset, P43 defaults to Tristate High Impedance while the Z86D990/D991 P43 is always configured as output. The data at Port 4 must be initialized as it is undefined at power-on reset.

The current output is a controlled current source that is controlled by the output of the value of P43 (see Table 9). P43 *cannot* be configured as input, and if P43 is read, P43 always returns the state of the output value (1 for no sink and 0 for sink).

P43 uses internal current reference and will draw current if it outputs a low logic even without external connection. This applies to both Run mode and Stop mode.

Table 9. Current Sink Pad P43 Specifications (Preliminary)

Parameter	Min	Max	Conditions
Rise time		0.4 µ	LED load
Fall time		0.02 µ	LED load
V_{outmin}		0.54 V	@27C
Comparator response		0.2 µ	
Regulated current	80 mA	120 mA	
Internal resistance		80 Ω	

The pad driver can function in two modes:

- controlled current output, when the voltage on the pad is over a minimum value

$$V_{pad} > V_{outmin}$$

- resistive pull down when the driver cannot regulate the current; in this mode, the gate of the NMOS pull down is raised to the power rail.

The I-V characteristics of the pad are presented in Figure 17.

Counter/timer 1 is driven by a timer clock generated by dividing the internal clock by four. The divide-by-four stage, the 6-bit prescaler, and the 8-bit counter/timer form a synchronous 16-bit divide chain. Counter/timer T_1 can also be driven by an external input (T_{IN}) using Port P52. Port $P5_6$ can serve as a timer output (T_{OUT}) through which T_1 or the internal clock can be output. The timer output toggles at the end-of-count. Figure 18 is a block diagram of the counter/timer.

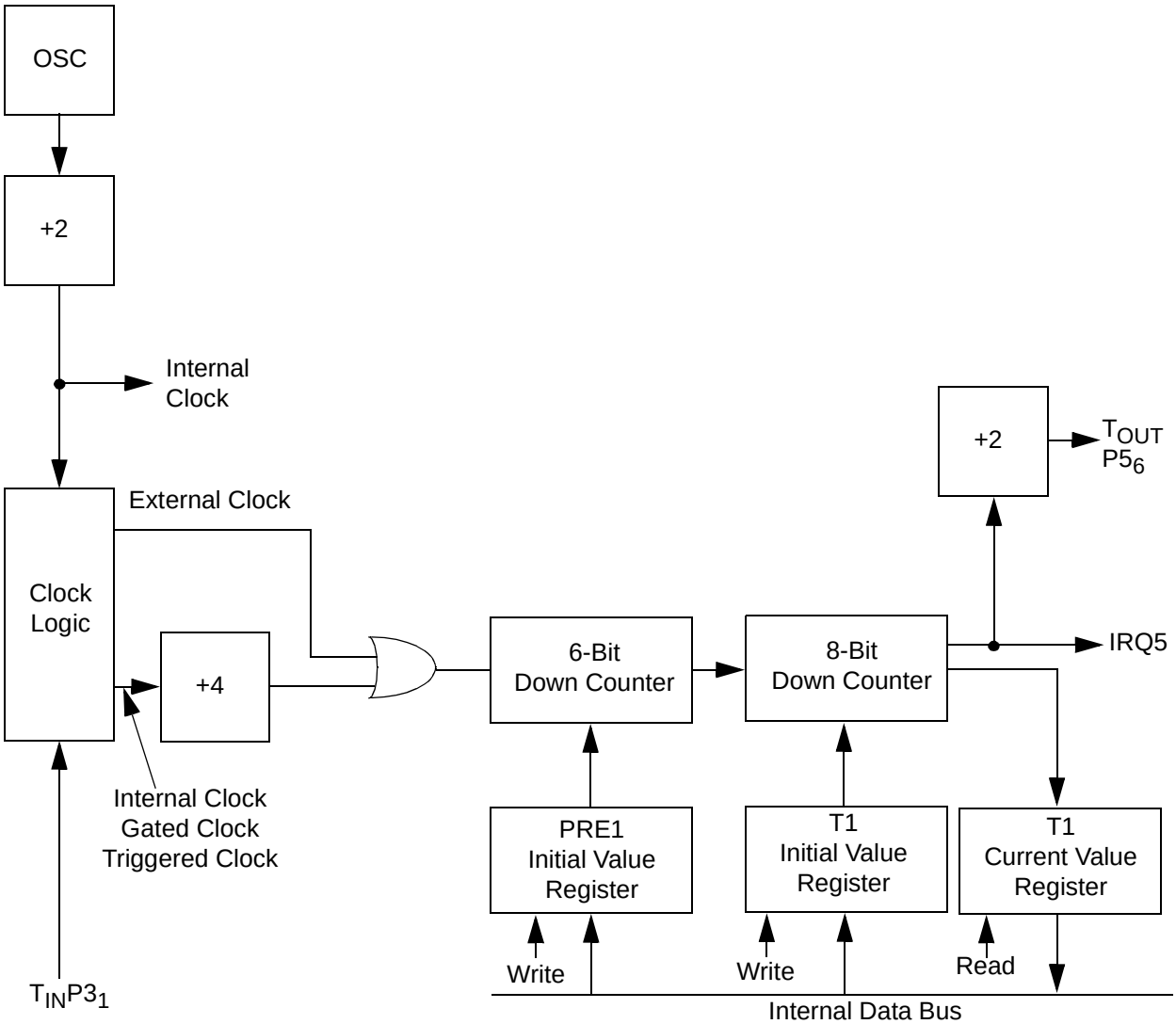


Figure 18. T_1 Counter/Timer Block Diagram

The six most significant bits (D_2–D_7) of PRE_1 hold the prescaler count modulo, a value from 11 to 64 decimal. The prescaler register also contains control bits that specify T_1 counting modes. These bits also indicate whether the clock source for T_1 is internal or external.

The counter/timer T_1 (F2h) consists of an 8-bit down-counter, a write-only register that holds the initial count value, and a read-only register that holds the current count value (see Figure 18 on page 35). The initial value can range from 1 to 256 decimal (01h, 02h, ..., 00h). Figure 21 illustrates the counter/timer register.

R242 T1
Counter/Timer 1 Register
(F2h; Read/Write)

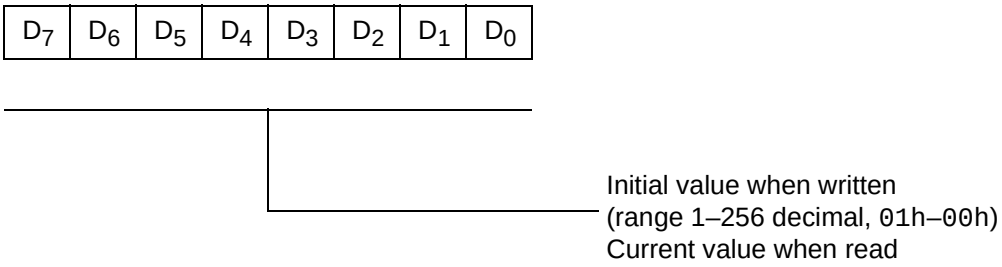


Figure 21. Counter/Timer 1 Register

Counter/Timer Operation

Under software control, T_1 is started and stopped using the Timer Mode register (F1h) bits D_2–D_3: a Load bit and an Enable Count bit. See Figure 22.

R241 TMR
Timer Mode Register
(F1h; Read/Write)

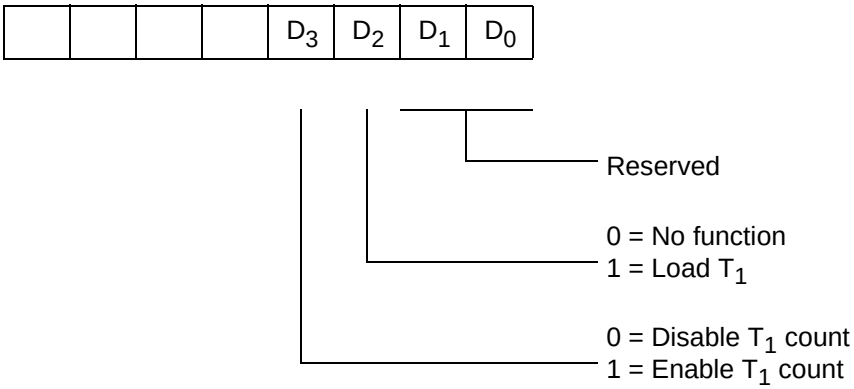


Figure 22. Timer Mode Register

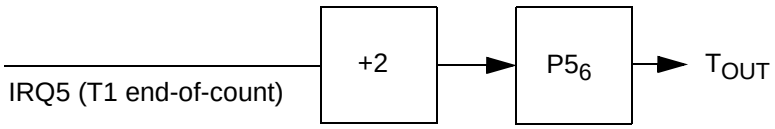


Figure 26. Counter/Timer Output Using T_{OUT}

The internal clock can be selected as output instead of T_1 by setting TMR bits D_7 and D_6 both to 1. The internal clock (XTAL frequency/2) is then directly output on $P5_6$ (Figure 27).

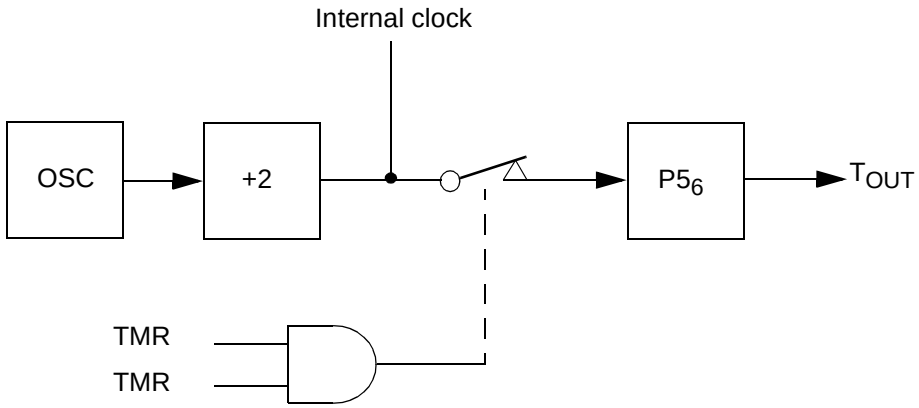


Figure 27. Internal Clock Output Using T_{OUT}

While programmed as T_{OUT}, $P5_6$ cannot be modified by a write to port register P5. However, the Z8 software can examine $P5_6$'s current output by reading the port register.

T_{IN} Modes

The Timer Mode register TMR (F1h) (Figure 28) is used in conjunction with the Prescaler register PRE_1 (F3h) (Figure 29) to configure $P5_2$ as T_{IN}. T_{IN} is used in conjunction with T_1 in one of four modes:

- External clock input
- Gated internal clock
- Triggered internal clock
- Retriggerable internal clock

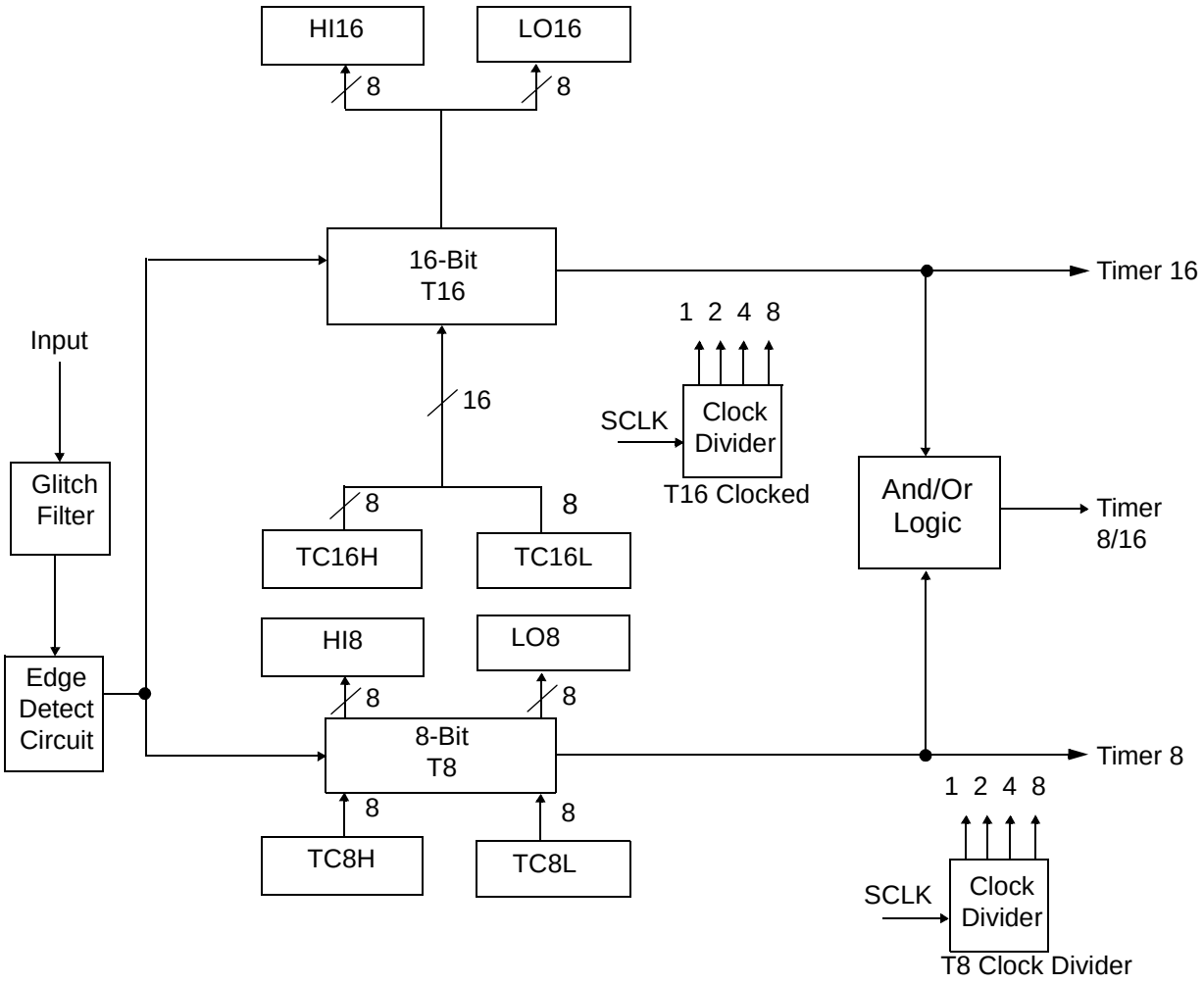


Figure 33. Counter/Timer Architecture

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If CTR1, D1 is 0, T8_OUT is 1. If CTR1, D1 is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In single-pass mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1). In modulo-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if T8_OUT level is 0), TC8L is loaded; if T8_OUT is 1, TC8H is loaded.

Table 15. FLAGS Register [Group/Bank F0h, Register C (R252)] (Continued)

____3___	Decimal Adjust Flag (D)	R/W	1 0	Used for BCD arithmetic—after a subtraction, the flag is set to 1; following an addition, it is cleared to 0
_____2__	Half Carry Flag (H)	R/W	1 0	Set to 1, whenever an addition generates a “carry out” of bit position 3 (overflow) of an accumulator; or subtraction generates a “borrow into” bit 3
______1_	User Flag (F2)	R/W	1 0	User definable
_______0	User Flag (F1)	R/W	1 0	User definable

Register Pointer (RP)

Z8 instructions can access registers directly or indirectly using either a 4-bit or 8-bit address field. The upper nibble of the Register Pointer, as described in Table 16, contains the base address of the active Working Register GROUP. The lower nibble contains the base address of the Expanded Register File BANK. When using 4-bit addressing, the 4-bit address of the working register (r0 to rF) is combined with the upper nibble of the Register Pointer (identifying the WR GROUP), thus forming the 8-bit actual address.

Table 16. RP Register [Group/Bank F0h, Register D (R253)]

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit/Field	**Working Register Group**				**Expanded Register File Bank**			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	**Bit/Field**	**R/W**	**Value**	**Description**
7654_____	Working Register Group Pointer	R/W	X	Identifies 1 of 16 possible WR Groups, each containing 16 Working Registers
_____3210	Expanded Register File Bank Pointer	R/W	X	Identifies 1 of 16 possible ERF Banks; only Banks 0, D, and F are valid for the Z86D99/Z86L99 family

Interrupt Mask Register

The IMR, as described in Table 21, individually or globally enables the six interrupt requests. Bit 7 of the IMR is the master enable and must be set before any of the individual interrupt requests can be recognized. Bit 7 must be set and reset by the enable interrupts and disable interrupts instructions only. The IMR is automatically reset during an interrupt service routine and set following the execution of an Interrupt Return (IRET) instruction.

Table 21. IMR (Group/Bank 0Fh, Register B)

Bit	7	6	5	4	3	2	1	0
Bit/Field	**Master**	**Re-served**	**IRQ5**	**IRQ4**	**IRQ3**	**IRQ2**	**IRQ1**	**IRQ0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	Master	R/W	1 0	Enable Master Interrupt Disable Master Interrupt
_6_____	Reserved	R W	1 X	Always reads 1 No Effect
__5_____	IRQ_5	R/W	1 0	Enable IRQ_5 Disable IRQ_5
___4____	IRQ_4	R/W	1 0	Enable IRQ_4 Disable IRQ_4
____3___	IRQ_3	R/W	1 0	Enable IRQ_3 Disable IRQ_3
_____2__	IRQ_2	R/W	1 0	Enable IRQ_2 Disable IRQ_2
______1_	IRQ_1	R/W	1 0	Enable IRQ_1 Disable IRQ_1
_______0	IRQ_0	R/W	1 0	Enable IRQ_0 Disable IRQ_0

Note: Bit 7 must be reset by the DI instruction before the contents of the Interrupt Mask Register or the Interrupt Priority Register are changed except in the following situations:

- Immediately after a hardware reset
- Immediately after executing an interrupt service routine and before IMR bit 7 has been set by any instruction

T1 Data Register (T1)

The counter/timer register (T1) consists of an 8-bit down counter, a write-only register that holds the initial count value, and a read-only register that holds the current count value. The initial value of T1 can range from 1 to 255 (0 represents 256) (see Table 34.)

Table 34. T1 Register [Group/Bank F0h, Register 2 (R242)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**T1_Value**							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76543210	T_1 Value	R	Data	Current Value
		W	Data	Initial Value (Range 1 to 256 Decimal)

T1 Mode Register (TMR)

Under software control, T1 counter/timer is started and stopped using the T1 Mode Register as shown in Table 35.

Table 35. TMR Register [Group/Bank F0h, Register 1 (R241)]

Bit	7	6	5	4	3	2	1	0
Bit/Field	**TOUT_Mode**		**TIN_Mode**		**T1_ Count**	**T1_ Load**	**Reserved**	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
76_____	T_{OUT} Mode	R/W	11	Internal Clock OUT on P56
			10	T_1OUT on P56
			01	Reserved
			00	Not used (P56 configured as I/O)
__54____	T_{IN} Mode	R/W	11	Trigger Input (Retriggerable)
			10	Trigger Input (Not-retriggerable)
			01	Gate Input
			00	External Clock Input (T_{IN} on P52)
____3___	T_1 Count	R/W	1	Enable T_1 Count
			0	Disable T_1 Count

T8/T16 Control Register A (CTR1)

The T8/T16 Control Register A controls the functions in common with both the T_8 and T_{16} counter/timers. The T_8 and T_{16} counter/timers have two primary modes of operation: Transmit Mode and Demodulation Mode. Transmit Mode is used for generating complex waveforms. The Transmit Mode has two submodes: Normal Mode and Ping-Pong Mode. The settings for CTR1 in Transmit Mode are given in Table 37.

Table 37. CTR1 Register (In Transmit Mode) (Group/Bank 0Dh, Register 1)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Mode	P43 Out	T8/T16_Logic		Transmit_ Submode		Initial_ T8_Out	Initial_ T16_ Out
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read, W = Write, X = Indeterminate

Bit Position	Bit/Field	R/W	Value	Description
7_____	Mode	R/W	1 0	Demodulation Transmit
_6_____	P43_Out	R/W	1 0	P43 configured as T8/T16 Output P43 configured as I/O
__54____	T_8/T_{16} Logic	R/W	11 10 01 00	NAND NOR OR AND
____32__	Transmit_ Submode	R/W	11 10 01 00	T16_Out = 1 T16_Out = 0 Ping-Pong Mode Normal Operation
_____1_	Initial_T8_Out	R/W	1 0	T8_Out set to 1 initially T8_Out set to 0 initially
_____0	Initial_T16_Out	R/W	1 0	T16_Out set to 1 initially T16_Out set to 0 initially

Electrical Characteristics

This section covers the absolute maximum ratings, standard test conditions, DC characteristics, and AC characteristics.

Absolute Maximum Ratings

Table 53 lists the absolute maximum ratings.

Table 53. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C
V_{RAM}	Minimum RAM Voltage	1.0 V**		

Note:
*Voltage on all pins with respect to GND.
†See “Ordering Information” on page 95.
** Estimated value, not tested.

Stresses greater than those listed in the preceding table can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 36).

Analog-to-Digital Converter Characteristics

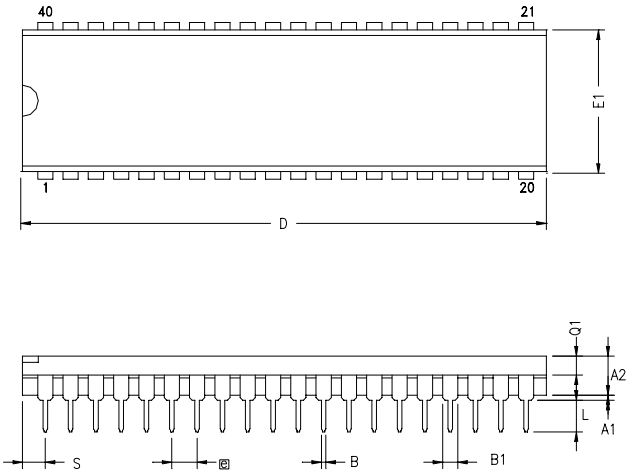
Table 56 lists the analog-to-digital converter characteristics.

Table 56. Analog-to-Digital Converter Characteristics

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		bits
Integral Nonlinearity		0.5	1	LSB
Differential Nonlinearity		0.5	1	LSB
Zero Error at 25 °C			7.8	mV
Supply Voltage Range (OTP)	3.0		5.5	V
Supply Voltage Range (ROM)	2.3		5.5	V
Power Dissipation (No Load)			1.2	mW
Clock Frequency (f ADC)			4	MHz
Input Voltage Range	V_{Ref-}		V_{Ref+}	V
Step Response			2/(0.0021 X f ADC)	s
ADC Input Capacitance	25		40	pF
Vref Input Capacitance	25		40	pF
V_{Ref+} Range	V_{Ref-}+2.0		AV_{DD}	V
V_{Ref-} Range	AGND		V_{Ref+}–2.0	V
$(V_{Ref+})–(V_{Ref-})$	2.0		AV_{DD}	V
Temperature Range	0		70	°C
3-db Frequency		(0.0021 X f ADC)		Hz
Signal to Noise	47			db
ADC Output Code		Dout		
Vref Input Source Impedance			1.0	kOhms
ADC Input Source Impedance			1.0	kOhms

Notes: Dout= $[(Vin–V_{Ref-})/(V_{Ref+}–V_{Ref-})]$ X 256
f ADC = set in ADCCTRL configuration register
Step Response is the time to track the input if a step from V_{Ref-} to V_{Ref+} is applied.

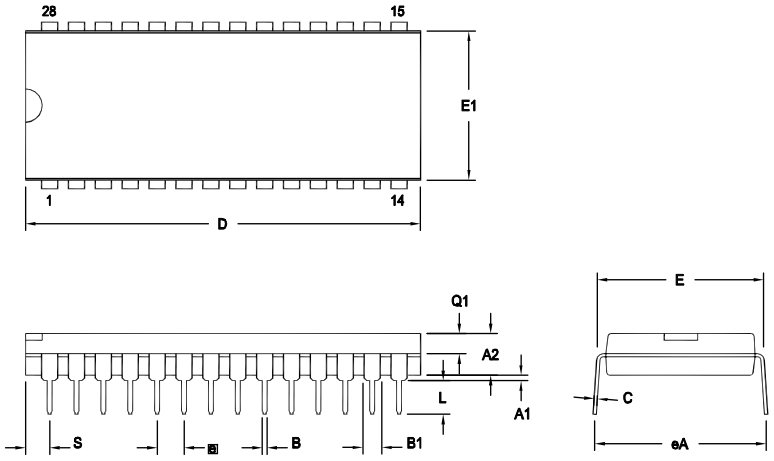
The ADC input is a switching capacitor that charges up to the applied input voltage whenever it is configured as an ADC input. If you switch it from digital mode to



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 38. 40-Pin PDIP



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 39. 28-Pin PDIP

Ordering Information

Part	PSI	Description
Z86D99 (OTP)	Z86D990PZ008SC	40-pin PDIP
	Z86D990HZ008SC	48-pin SSOP
	Z86D991PZ008SC	28-pin PDIP
	Z86D991SZ008SC	28-pin SOIC
Z86L99 (Mask ROM)	Z86L990PZ008SC	40-pin PDIP
	Z86L990HZ008SC	48-pin SSOP
	Z86L991PZ008SC	28-pin PDIP
	Z86L991SZ008SC	28-pin SOIC
	Z86L996PZ008SC	28-pin PDIP
	Z86L996SZ008SC	28-pin SOIC
	Z86L997PZ008SC	28-pin PDIP
	Z86L997SZ008SC	28-pin SOIC
Emulator	Z86L9900100ZEM	Emulator/Programmer
Adapter	Z86D9900100ZDH	48 SSOP Adapter
Evaluation Board	Z86L9900100ZCO	Evaluation Board

For fast results, contact your local ZiLOG sale offices for assistance in ordering part(s). Updated information can be found on the ZiLOG website: HTTP://WWW.ZILOG.COM

Precharacterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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