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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-24lfxi

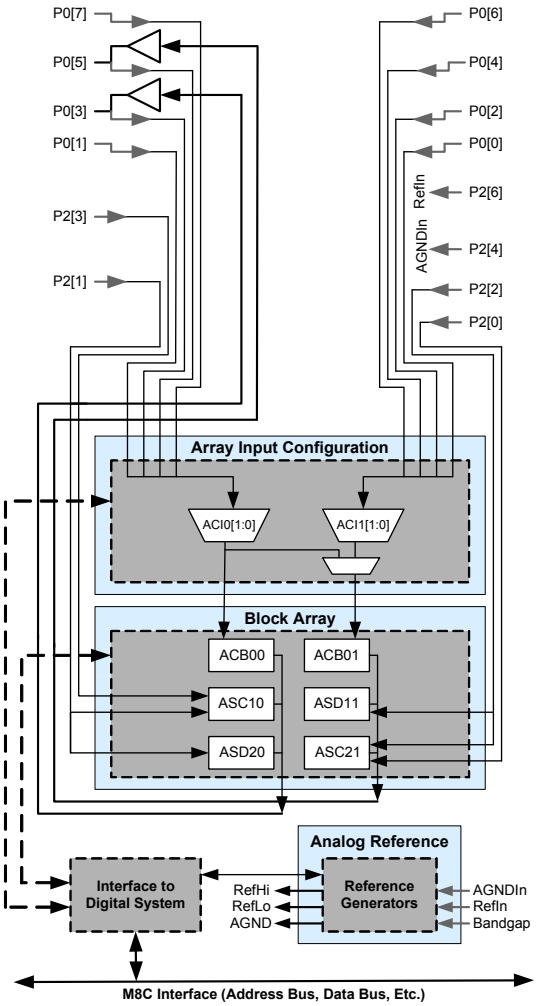
Analog System

The Analog System consists of six configurable blocks, each consisting of an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master are supported.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms Used

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SLIMO	slow IMO
SMP	switch mode pump
SRAM	static random access memory

Units of Measure

A unit of measure table is located in the section Electrical Specifications on page 17. Table 8 on page 14 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

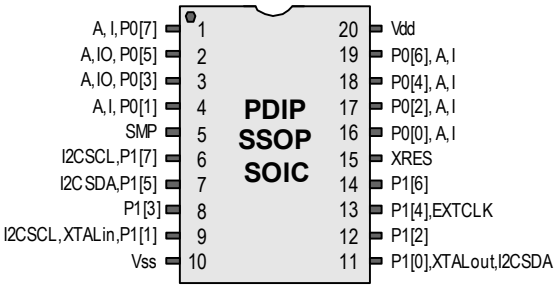
Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

20-Pin Part Pinout

Table 4. Pin Definitions - 20-Pin PDIP, SSOP, and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog Column Mux Input
2	I/O	I/O	P0[5]	Analog Column Mux Input and Column Output
3	I/O	I/O	P0[3]	Analog Column Mux Input and Column Output
4	I/O	I	P0[1]	Analog Column Mux Input
5	Power		SMP	Switch Mode Pump (SMP) Connection to External Components required
6	I/O		P1[7]	I2C Serial Clock (SCL)
7	I/O		P1[5]	I2C Serial Data (SDA)
8	I/O		P1[3]	
9	I/O		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*
10	Power		Vss	Ground Connection.
11	I/O		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*
12	I/O		P1[2]	
13	I/O		P1[4]	Optional External Clock Input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active High External Reset with Internal Pull Down
16	I/O	I	P0[0]	Analog Column Mux Input
17	I/O	I	P0[2]	Analog Column Mux Input
18	I/O	I	P0[4]	Analog Column Mux Input
19	I/O	I	P0[6]	Analog Column Mux Input
20	Power		Vdd	Supply Voltage

Figure 4. CY8C24223A 20-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable Sytem-on-Chip Technical Reference Manual* for details.

28-Pin Part Pinout

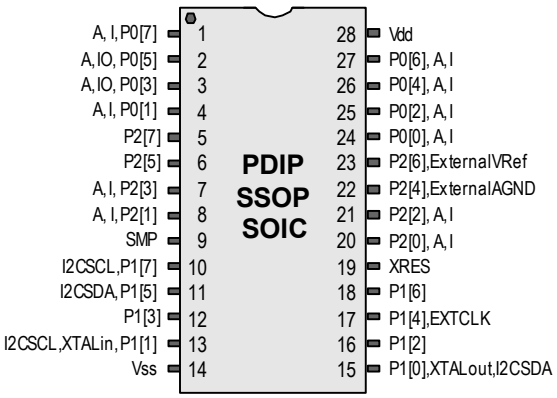
Table 5. Pin Definitions - 28-Pin PDIP, SSOP, and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog Column Mux Input
2	I/O	I/O	P0[5]	Analog Column Mux Input and column output
3	I/O	I/O	P0[3]	Analog Column Mux Input and Column Output
4	I/O	I	P0[1]	Analog Column Mux Input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct Switched Capacitor Block Input
8	I/O	I	P2[1]	Direct Switched Capacitor Block Input
9	Power		SMP	Switch Mode Pump (SMP) Connection to External Components required
10	I/O		P1[7]	I2C Serial Clock (SCL)
11	I/O		P1[5]	I2C Serial Data (SDA)
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*
14	Power		Vss	Ground connection.
15	I/O		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK)
18	I/O		P1[6]	
19	Input		XRES	Active High External Reset with Internal Pull Down
20	I/O	I	P2[0]	Direct Switched Capacitor Block Input
21	I/O	I	P2[2]	Direct Switched Capacitor Block Input
22	I/O		P2[4]	External Analog Ground (AGND)
23	I/O		P2[6]	External Voltage Reference (VRef)
24	I/O	I	P0[0]	Analog Column Mux Input
25	I/O	I	P0[2]	Analog Column Mux Input
26	I/O	I	P0[4]	Analog Column Mux Input
27	I/O	I	P0[6]	Analog Column Mux Input
28	Power		Vdd	Supply Voltage

LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable Sytem-on-Chip Technical Reference Manual* for details.

Figure 5. CY8C24423A 28-Pin PSoC Device



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 13. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 50 on page 50. The user must limit the power consumption to comply with this requirement.

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 17. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = High Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	64	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd

Table 23. 2.7V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 0.2 0.5 x Vdd + 0.2	 – –	 – –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 0.7 0.5 x Vdd - 0.7	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25).

DC Switch Mode Pump Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

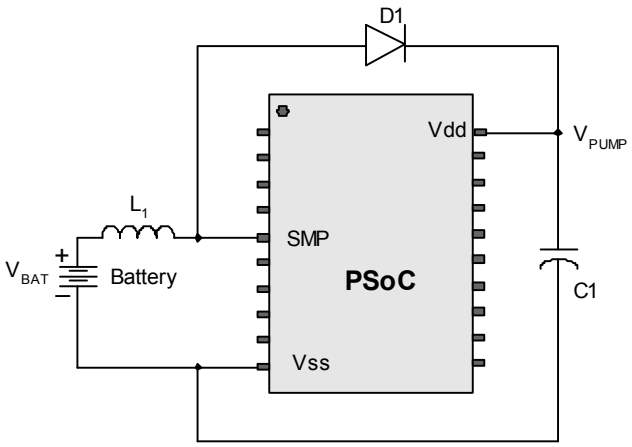
Table 24. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5V Output Voltage from Pump	4.75	5.0	5.25	V	Configuration listed in footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V_{PUMP} 3V	3.3V Output Voltage from Pump	3.00	3.25	3.60	V	Configuration listed in footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
V_{PUMP} 2V	2.6V Output Voltage from Pump	2.45	2.55	2.80	V	Configuration listed in footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 2.55V.
I_{PUMP}	Available Output Current V_{BAT} = 1.8V, V_{PUMP} = 5.0V V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.3V, V_{PUMP} = 2.55V	 5 8 8	 – – –	 – – –	 mA mA mA	Configuration listed in footnote.[a] SMP trip voltage is set to 5.0V. SMP trip voltage is set to 3.25V. SMP trip voltage is set to 2.55V.
V_{BAT}5V	Input Voltage Range from Battery	1.8	–	5.0	V	Configuration listed in footnote.[a] SMP trip voltage is set to 5.0V.
V_{BAT}3V	Input Voltage Range from Battery	1.0	–	3.3	V	Configuration listed in footnote.[a] SMP trip voltage is set to 3.25V.
V_{BAT}2V	Input Voltage Range from Battery	1.0	–	3.0	V	Configuration listed in footnote.[a] SMP trip voltage is set to 2.55V.
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.2	–	–	V	Configuration listed in footnote.[a] 0°C ≤ T_A ≤ 100. 1.25V at T_A = -40°C

Table 24. DC Switch Mode Pump (SMP) Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
ΔV_{PUMP_Line}	Line Regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration listed in footnote.[4] V_O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 29 on page 29.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$	Configuration listed in footnote.[4] V_O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 29 on page 29.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration listed in footnote.[4] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration listed in footnote.[4] Load is 5 mA. SMP trip voltage is set to 3.25V.
E_2	Efficiency					
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

Figure 13. Basic Switch Mode Pump Circuit



Note
4. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 13.

DC Analog Reference Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 25. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2 P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

Table 26. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.33	V
–	AGND = Vdd/2	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			

DC Analog PSoC Block Specifications

Table 29 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 28. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

DC POR, SMP, and LVD Specifications

Table 30 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Programmable Sytem-on-Chip Technical Reference Manual* for more information on the VLT_CR register.

Table 29. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[5]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[6]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	Vdd Value for SMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.50	2.55	2.62[7]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[8]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
5. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
6. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.
7. Always greater than 50 mV above V_{LVD0}.
8. Always greater than 50 mV above V_{LVD3}.

AC General Purpose IO Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 33. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Table 34. 2.7V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%

Figure 19. GPIO Timing Diagram

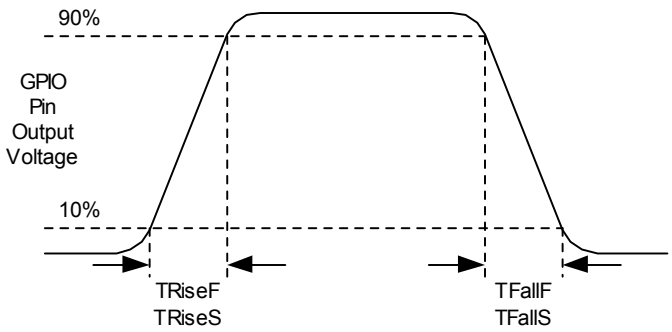


Table 37. 2.7V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 40. 2.7V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			12.7	MHz	2.4V < Vdd < 3.0V
Timer	Capture Pulse Width	100[18]	–	–	ns	
	Maximum Frequency, With or Without Capture	–	–	12.7	MHz	
Counter	Enable Pulse Width	100[18]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	12.7	MHz	
	Maximum Frequency, Enable Input	–	–	12.7	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	100[18]	–	–	ns	
	Disable Mode	100[18]	–	–	ns	
	Maximum Frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
SPIM	Maximum Input Clock Frequency	–	–	6.35	MHz	Maximum data rate at 3.17 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.23	ns	
	Width of SS_ Negated Between Transmissions	100[18]	–	–	ns	
Trans-mitter	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.

Note
18. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Table 43. 2.7V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 4 4	 µs µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3 3	 µs µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.4 0.4	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.4 0.4	 – –	 – –	 V/µs V/µs
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load Power = Low Power = High	 0.6 0.6	 – –	 – –	 MHz MHz
BW_{OB}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100 pF Load Power = Low Power = High	 180 180	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 44. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

Table 45. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[19]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[20]	0.186	–	24.6	MHz
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

Notes
19. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
20. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met

Table 46. 2.7V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[21]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[22]	0.186	–	12.3	MHz
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

AC Programming Specifications

Table 47 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 47. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	20	–	ms	
T_{WRITE}	Flash Block Write Time	–	20	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0

AC I^2C Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 48. AC Characteristics of the I^2C SDA and SCL Pins for Vdd > 3.0V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[23]	–	ns

Notes

21. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
22. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
23. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ Š 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 28. 28-Pin (300-Mil) Molded DIP

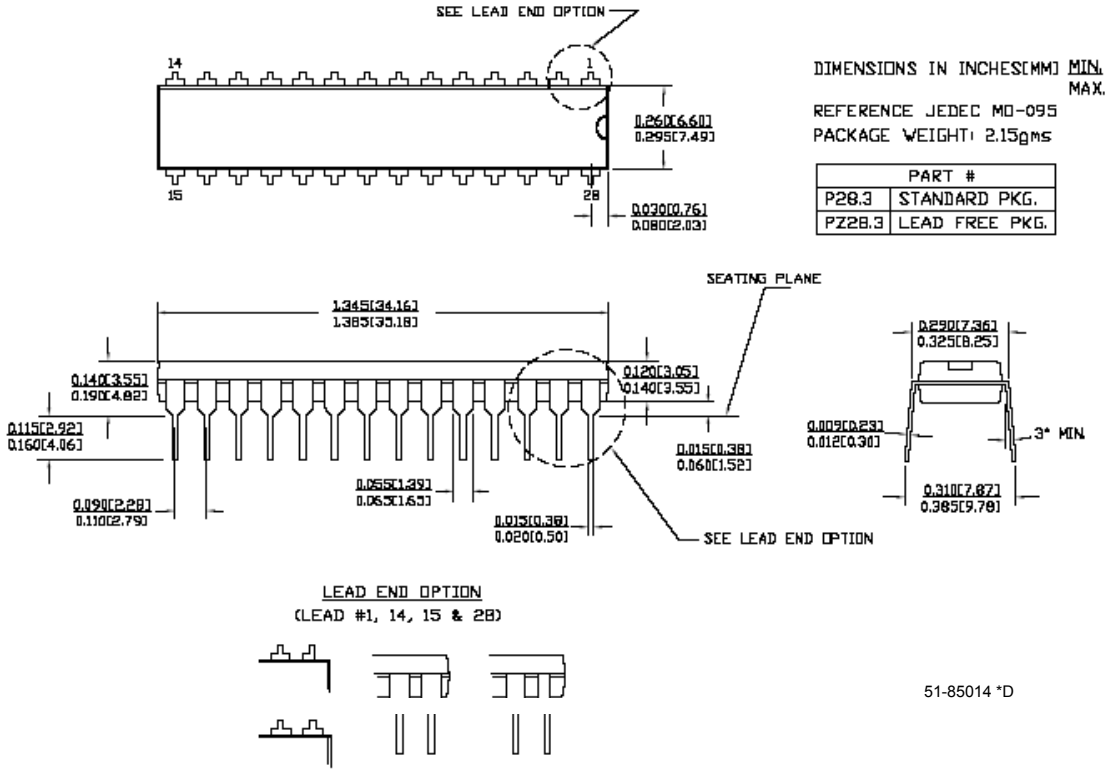


Figure 29. 28-Pin (210-Mil) SSOP

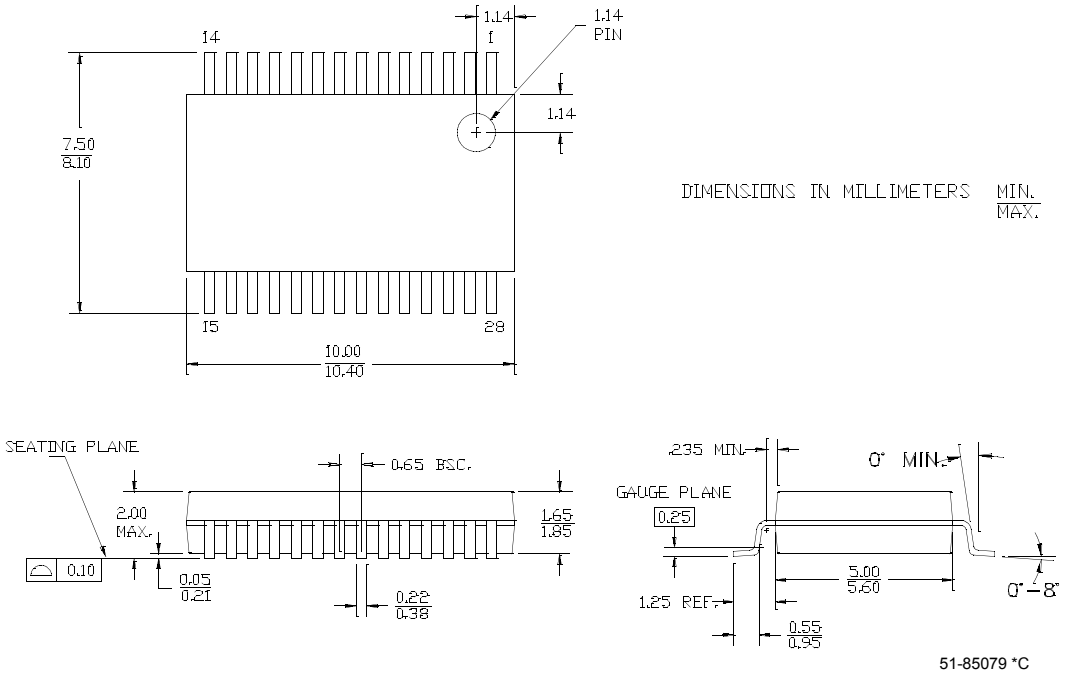
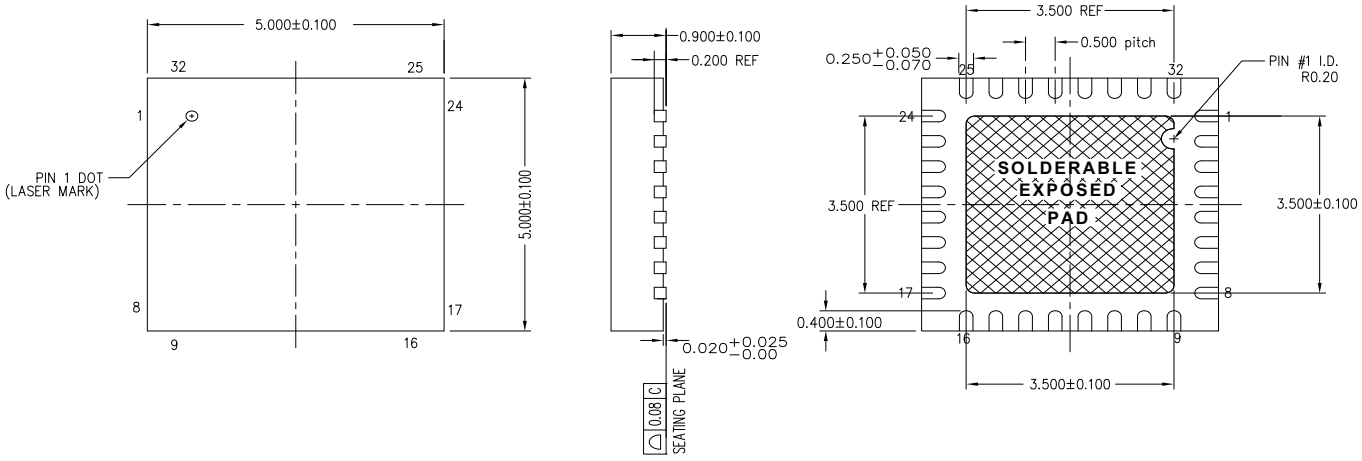


Figure 32. 32-Pin Sawn QFN Package



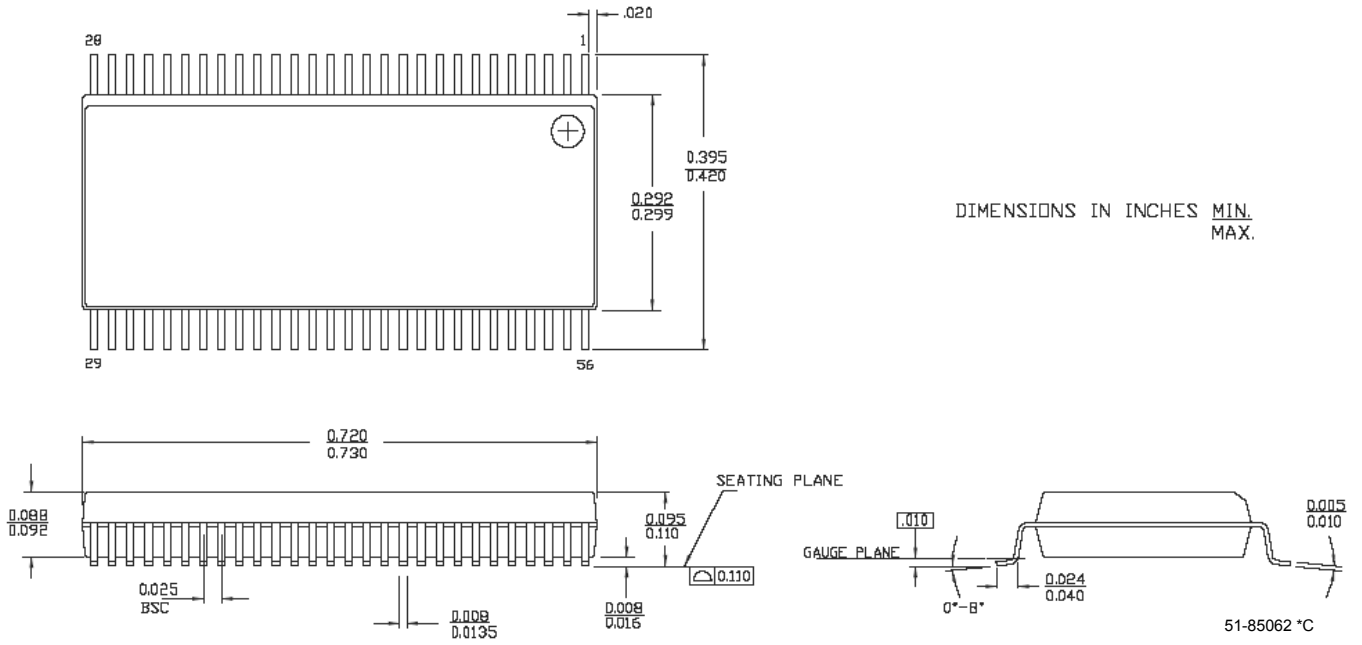
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. PACKAGE WEIGHT: 0.058g
4. DIMENSIONS ARE IN MILLIMETERS

001-30999 *A

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 33. 56-Pin (300-Mil) SSOP



CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 53. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[26]	Foot Kit[27]	Adapter[28]
All non-QFN	All non QFN	CY3250-24X23A	CY3250-8DIP-FK, CY3250-8SOIC-FK, CY3250-20DIP-FK, CY3250-20SOIC-FK, CY3250-20SSOP-FK, CY3250-28DIP-FK, CY3250-28SOIC-FK, CY3250-28SSOP-FK	Adapters can be found at http://www.emulation.com.
CY8C24423A-24LFXI	32 QFN	CY3250-24X23AQFN	CY3250-32QFN-FK	

Third Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see application note AN2323 “Debugging - Build a PSoC Emulator into Your Board”.

Notes
26. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
27. Foot kit includes surface mount feet that can be soldered to the target PCB.
28. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

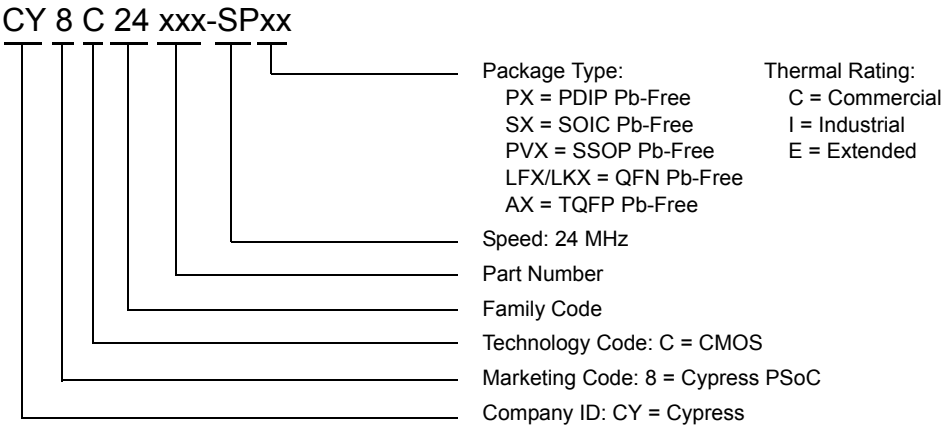
The following table lists the CY8C24x23A PSoC device's key package features and ordering codes.

Table 54. CY8C24x23A PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (300 Mil) DIP	CY8C24123A-24PXI	4K	256	No	-40C to +85C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC	CY8C24123A-24SXI	4K	256	No	-40C to +85C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC (Tape and Reel)	CY8C24123A-24SXIT	4K	256	No	-40C to +85C	4	6	6	4	2	No
20 Pin (300 Mil) DIP	CY8C24223A-24PXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP	CY8C24223A-24PVXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24223A-24PVXIT	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC	CY8C24223A-24SXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24223A-24SXIT	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
28 Pin (300 Mil) DIP	CY8C24423A-24PXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP	CY8C24423A-24PVXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423A-24PVXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC	CY8C24423A-24SXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24423A-24SXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm) QFN	CY8C24423A-24LFXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm 1.00 MAX) SAWN QFN	CY8C24423A-24LTXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm 1.00 MAX) SAWN QFN (Tape and Reel)	CY8C24423A-24LTXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
56 Pin OCD SSOP	CY8C24000A-24PVXI[29]	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Note
29. This part may be used for in-circuit debugging. It is NOT available for production

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

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USB	psoc.cypress.com/usb