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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-24lfxit

PSoC Functional Overview

The PSoC family consists of many Mixed-Signal Array with On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in Figure 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows combining all the device resources into a complete custom system. The PSoC CY8C24x23A family can have up to three IO ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 11 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watchdog Timers (WDT).

Memory encompasses 4 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

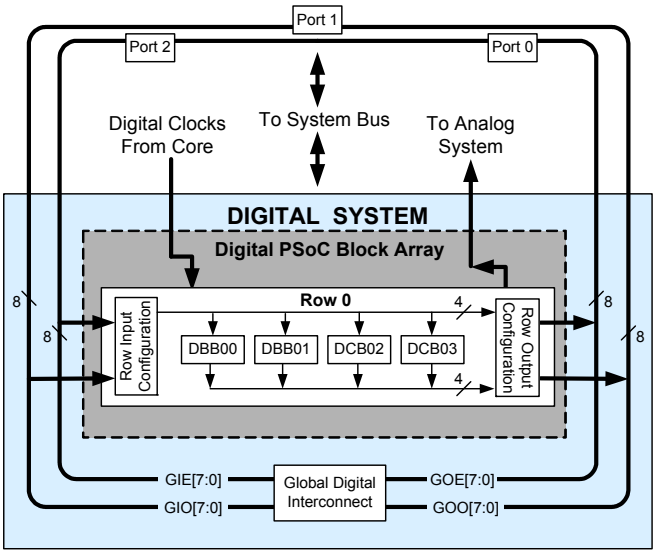
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is required, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin can generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital System consists of 4 digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave and multi-master (one is available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This gives a choice of system resources for your application. Family resources are shown in Table 1 on page 4.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms Used

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SLIMO	slow IMO
SMP	switch mode pump
SRAM	static random access memory

Units of Measure

A unit of measure table is located in the section Electrical Specifications on page 17. Table 8 on page 14 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

56-Pin Part Pinout

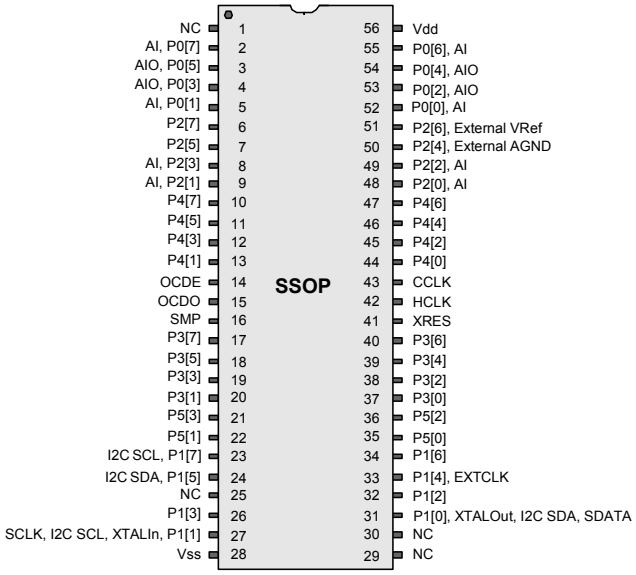
The 56-pin SSOP part is for the CY8C24000A On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. Pin Definitions - 56-Pin SSOP

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No Connection
2	I/O	I	P0[7]	Analog Column Mux Input
3	I/O	I	P0[5]	Analog Column Mux Input and Column Output
4	I/O	I	P0[3]	Analog Column Mux Input and Column Output
5	I/O	I	P0[1]	Analog Column Mux Input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct Switched Capacitor Block Input
9	I/O	I	P2[1]	Direct sWitched Capacitor Block Input
10	I/O		P4[7]	
11	I/O		P4[5]	
12	I/O	I	P4[3]	
13	I/O	I	P4[1]	
14	OCD		OCDE	OCD Even Data IO.
15	OCD		OCDO	OCD Odd Data Output
16	Power		SMP	Switch Mode Pump (SMP) Connection to required External Components
17	I/O		P3[7]	
18	I/O		P3[5]	
19	I/O		P3[3]	
20	I/O		P3[1]	
21	I/O		P5[3]	
22	I/O		P5[1]	
23	I/O		P1[7]	I2C Serial Clock (SCL)
24	I/O		P1[5]	I2C Serial Data (SDA)
25			NC	No Connection
26	I/O		P1[3]	
27	I/O		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*
28	Power		Vdd	Supply Voltage
29			NC	No Connection
30			NC	No Connection
31	I/O		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*
32	I/O		P1[2]	
33	I/O		P1[4]	Optional External Clock Input (EXTCLK)

Figure 10. CY8C24000A 56-Pin PSoC Device



Not for Production

Table 7. Pin Definitions - 56-Pin SSOP (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
34	I/O		P1[6]	
35	I/O		P5[0]	
36	I/O		P5[2]	
37	I/O		P3[0]	
38	I/O		P3[2]	
39	I/O		P3[4]	
40	I/O		P3[6]	
41	Input		XRES	Active high external reset with internal pull down.
42	OCD		HCLK	OCD high-speed clock output.
43	OCD		CCLK	OCD CPU clock output.
44	I/O		P4[0]	
45	I/O		P4[2]	
46	I/O		P4[4]	
47	I/O		P4[6]	
48	I/O	I	P2[0]	Direct switched capacitor block input.
49	I/O	I	P2[2]	Direct switched capacitor block input.
50	I/O		P2[4]	External Analog Ground (AGND).
51	I/O		P2[6]	External Voltage Reference (VRef).
52	I/O	I	P0[0]	Analog column mux input.
53	I/O	I	P0[2]	Analog column mux input and column output.
54	I/O	I	P0[4]	Analog column mux input and column output.
55	I/O	I	P0[6]	Analog column mux input.
56	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable Sytem-on-Chip Technical Reference Manual* for details.

Register Reference

This section lists the registers of the CY8C24x23A PSoC device. For detailed register information, refer the *PSoC Programmable Sytem-on-Chip Reference Manual*.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 8. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 9. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23A PSoC device. For the latest electrical specifications, check if you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Refer to Table 31 on page 31 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 11. Voltage versus CPU Frequency

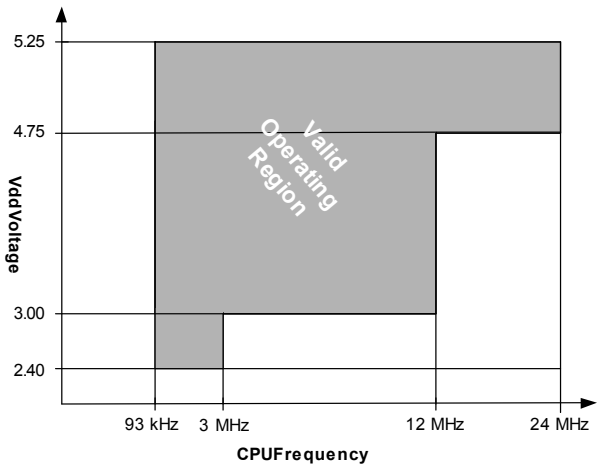
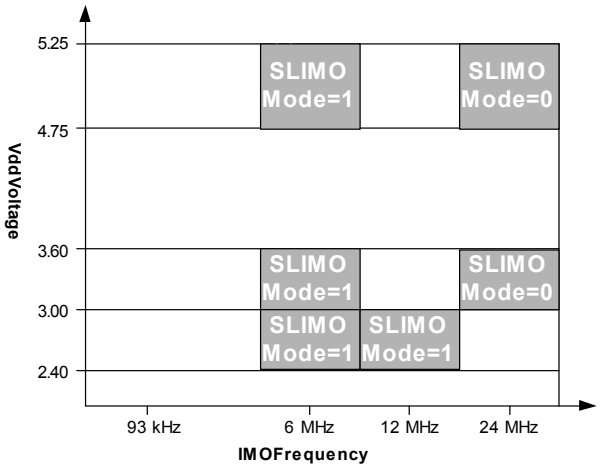


Figure 12. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 11. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

DC Electrical Characteristics

DC Chip-Level Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 14. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	2.4	–	5.25	V	See DC POR and LVD specifications, Table 29 on page 29.
I_{DD}	Supply Current	–	5	8	mA	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{DD3}	Supply Current	–	3.3	6.0	mA	Conditions are Vdd = 3.3V, T_A= 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.
I_{DD27}	Supply Current	–	2	4	mA	Conditions are Vdd = 2.7V, T_A = 25°C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz, analog power = off. SLIMO mode = 1. IMO = 6 MHz.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[3]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40°C ≤ T_A ≤ 55°C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[3]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55°C < T_A ≤ 85°C, analog power = off.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[3]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40°C ≤ T_A ≤ 55°C, analog power = off.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[3]	–	5	26	µA	Conditions are with properly loaded, 1µW max, 32.768 kHz crystal. Vdd = 3.3 V, 55°C < T_A ≤ 85°C, analog power = off.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.33	V	Trimmed for appropriate Vdd. Vdd > 3.0V
V_{REF27}	Reference Voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate Vdd. Vdd = 2.4V to 3.0V

Note
3. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

Table 19. 2.7V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5 Volts Only	 – –	 1.65 1.32	 10 8	 mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High	 60 60 80	–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	64	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd

DC Low Power Comparator Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 20. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Table 21. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 .5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25).

Table 22. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	V_{OUT} > (Vdd - 1.25)

Table 32. 2.7V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	Internal Main Oscillator Frequency for 12 MHz	11.5	12	12.7[14,15,16]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 12 on page 17. SLIMO mode = 1.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[14,15,16]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 12 on page 17. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.93	3	3.15[14,15]	MHz	
F_{BLK27}	Digital PSoC Block Frequency (2.7V Nominal)	0	12	12.7[14,15,16]	MHz	Refer to the AC Digital Block Specifications.
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
Jitter32k	32 kHz Period Jitter	–	150		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC12M	12 MHz Duty Cycle	40	50	60	%	
Jitter12M1P	12 MHz Period Jitter (IMO) Peak-to-Peak	–	340		ps	
Jitter12M1R	12 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.7	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Notes
14. 2.4V < Vdd < 3.0V.
15. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
16. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on maximum frequency for User Modules.

Figure 14. PLL Lock Timing Diagram

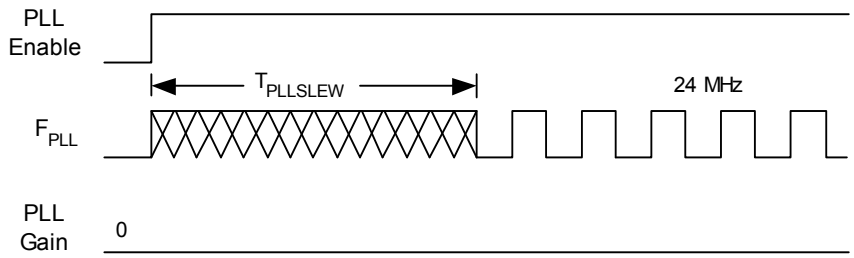


Figure 15. PLL Lock for Low Gain Setting Timing Diagram

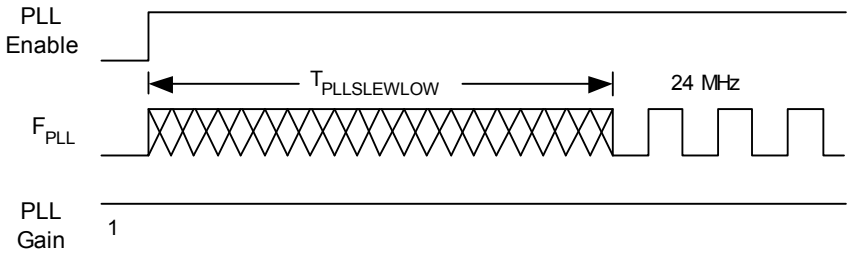


Figure 16. External Crystal Oscillator Startup Timing Diagram

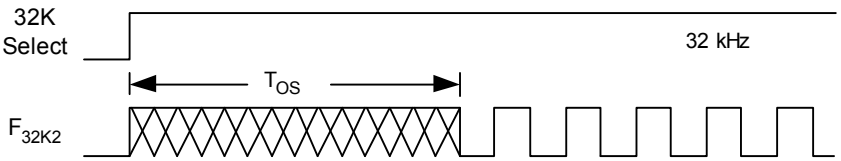


Figure 17. 24 MHz Period Jitter (IMO) Timing Diagram

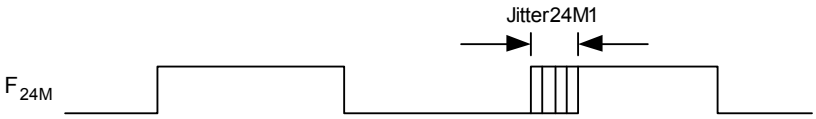
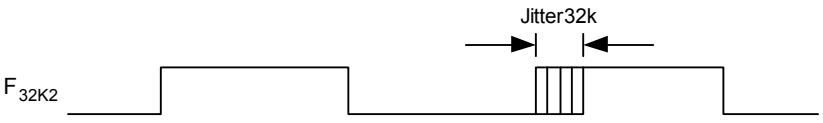


Figure 18. 32 kHz Period Jitter (ECO) Timing Diagram



AC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V and 2.7V.

Table 35. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 36. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Figure 30. 28-Pin (300-Mil) Molded SOIC

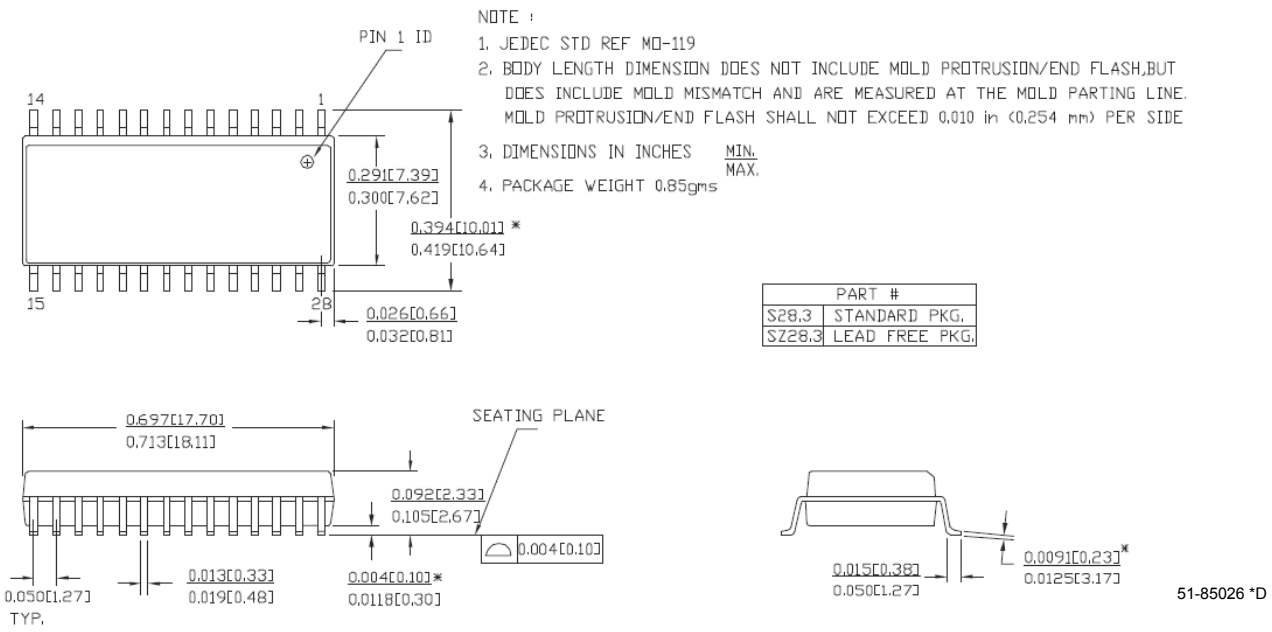
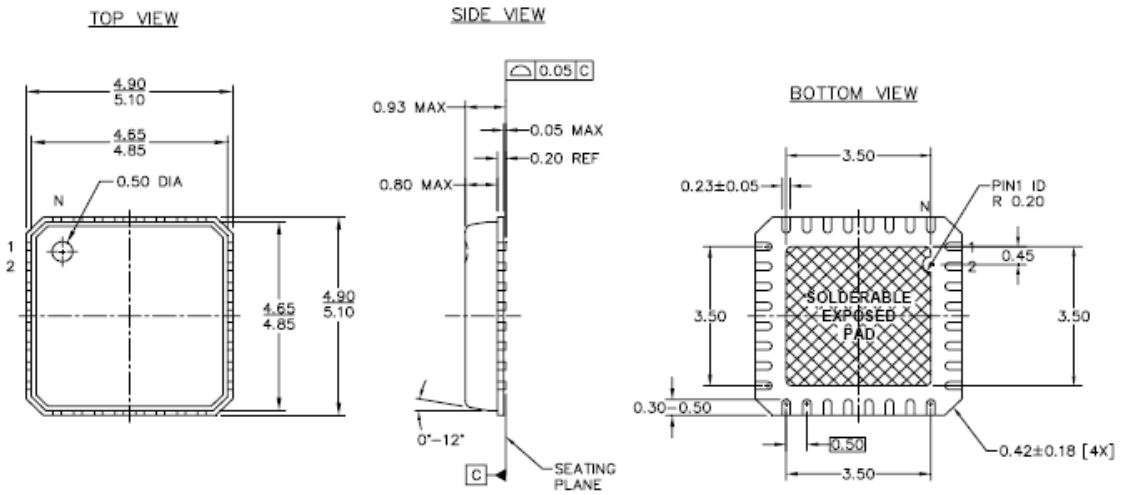


Figure 31. 32-Pin (5x5 mm) QFN

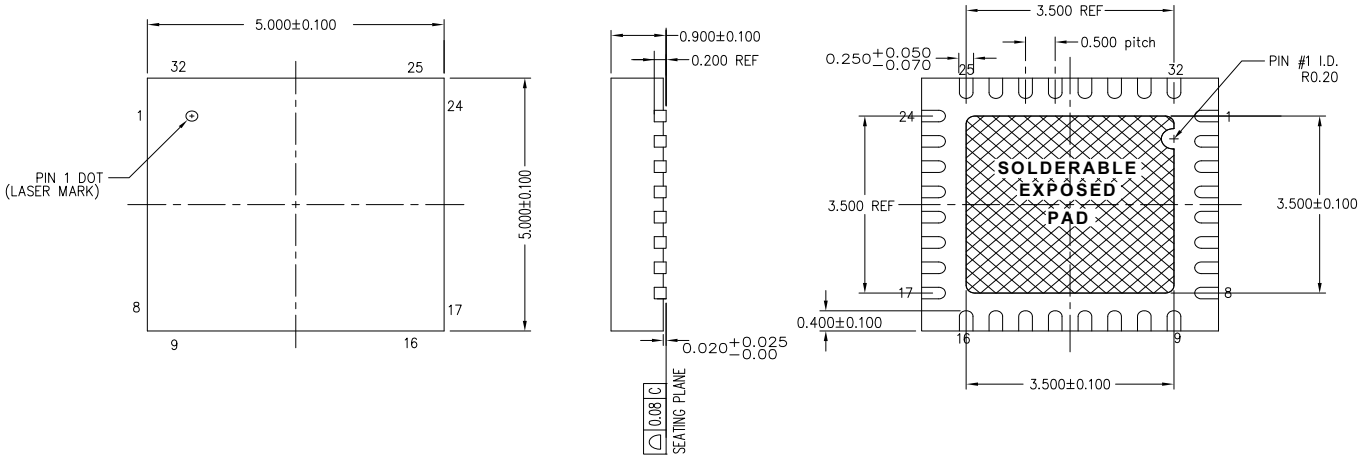


NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.054g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF32	STANDARD
LY32	PB-FREE

51-85188 *C

Figure 32. 32-Pin Sawn QFN Package



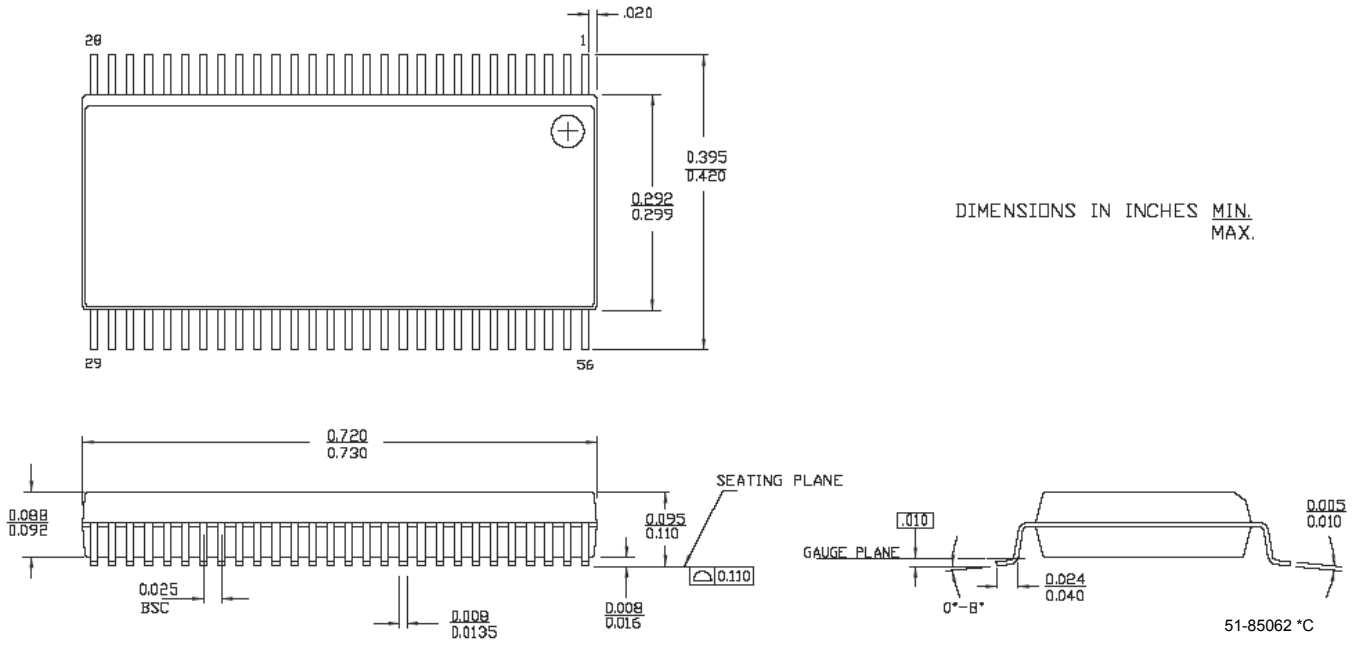
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. PACKAGE WEIGHT: 0.058g
4. DIMENSIONS ARE IN MILLIMETERS

001-30999 *A

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 33. 56-Pin (300-Mil) SSOP



Thermal Impedances

Table 50. Thermal Impedances per Package

Package	Typical θ_{JA} [24]
8 PDIP	123°C/W
8 SOIC	185°C/W
20 PDIP	109°C/W
20 SSOP	117 °C/W
20 SOIC	81°C/W
28 PDIP	69 °C/W
28 SSOP	101°C/W
28 SOIC	74 °C/W
32 QFN	22°C/W

Capacitance on Crystal Pins

Table 51. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8 PDIP	2.8 pF
8 SOIC	2.0 pF
20 PDIP	3.0 pF
20 SSOP	2.6 pF
20 SOIC	2.5 pF
28 PDIP	3.5 pF
28 SSOP	2.8 pF
28 SOIC	2.7 pF
32 QFN	2.0 pF

Solder Reflow Peak Temperature

The following table lists the minimum solder reflow peak temperatures to achieve good solderability.

Table 52. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[25]	Maximum Peak Temperature
8 PDIP	240°C	260°C
8 SOIC	240°C	260°C
20 PDIP	240°C	260°C
20 SSOP	240°C	260°C
20 SOIC	220°C	260°C
28 PDIP	240°C	260°C
28 SSOP	240°C	260°C
28 SOIC	220°C	260°C
32 QFN	240°C	260°C

Notes
24. $T_J = T_A + POWER \times \theta_{JA}$
25. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 53. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[26]	Foot Kit[27]	Adapter[28]
All non-QFN	All non QFN	CY3250-24X23A	CY3250-8DIP-FK, CY3250-8SOIC-FK, CY3250-20DIP-FK, CY3250-20SOIC-FK, CY3250-20SSOP-FK, CY3250-28DIP-FK, CY3250-28SOIC-FK, CY3250-28SSOP-FK	Adapters can be found at http://www.emulation.com.
CY8C24423A-24LFXI	32 QFN	CY3250-24X23AQFN	CY3250-32QFN-FK	

Third Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see application note AN2323 “Debugging - Build a PSoC Emulator into Your Board”.

Notes
26. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
27. Foot kit includes surface mount feet that can be soldered to the target PCB.
28. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

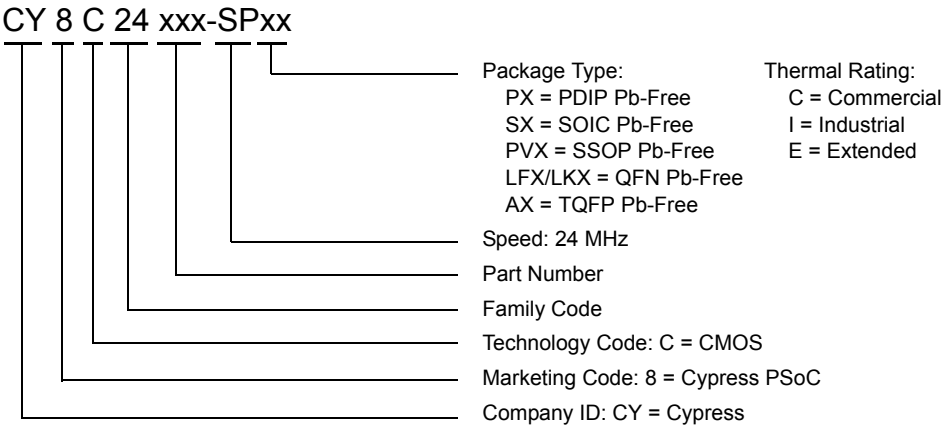
The following table lists the CY8C24x23A PSoC device's key package features and ordering codes.

Table 54. CY8C24x23A PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
8 Pin (300 Mil) DIP	CY8C24123A-24PXI	4K	256	No	-40C to +85C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC	CY8C24123A-24SXI	4K	256	No	-40C to +85C	4	6	6	4	2	No
8 Pin (150 Mil) SOIC (Tape and Reel)	CY8C24123A-24SXIT	4K	256	No	-40C to +85C	4	6	6	4	2	No
20 Pin (300 Mil) DIP	CY8C24223A-24PXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP	CY8C24223A-24PVXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24223A-24PVXIT	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC	CY8C24223A-24SXI	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
20 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24223A-24SXIT	4K	256	Yes	-40C to +85C	4	6	16	8	2	Yes
28 Pin (300 Mil) DIP	CY8C24423A-24PXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP	CY8C24423A-24PVXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423A-24PVXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC	CY8C24423A-24SXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C24423A-24SXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm) QFN	CY8C24423A-24LFXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm 1.00 MAX) SAWN QFN	CY8C24423A-24LTXI	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
32 Pin (5x5 mm 1.00 MAX) SAWN QFN (Tape and Reel)	CY8C24423A-24LTXIT	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes
56 Pin OCD SSOP	CY8C24000A-24PVXI[29]	4K	256	Yes	-40C to +85C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Note
29. This part may be used for in-circuit debugging. It is NOT available for production

Document History Page

Document Title: CY8C24123A, CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip™ Document Number: 38-12028				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	236409	SFV	See ECN	New silicon and new document – Preliminary Data Sheet.
*A	247589	SFV	See ECN	Changed the title to read “Final” data sheet. Updated Electrical Specifications chapter.
*B	261711	HMT	See ECN	Input all SFV memo changes. Updated Electrical Specifications chapter.
*C	279731	HMT	See ECN	Update Electrical Specifications chapter, including 2.7 VIL DC GPIO spec. Add Solder Reflow Peak Temperature table. Clean up pinouts and fine tune wording and format throughout.
*D	352614	HMT	See ECN	Add new color and CY logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications. Re-add ISSP pinout identifier. Delete Electrical Specification sentence re: devices running at greater than 12 MHz. Update Solder Reflow Peak Temperature table. Fix CY.com URLs. Update CY copyright.
*E	424036	HMT	See ECN	Fix SMP 8-pin SOIC error in Feature and Order table. Update 32-pin QFN E-Pad dimensions and rev. *A. Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Add OCD non-production pinout and package diagram. Update CY branding and QFN convention. Update package diagram revisions.
*F	521439	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table.
*G	2256806	UVS/PYRS	See ECN	Added Sawn pin information.
*H	2425586	DSO/AESA	See ECN	Corrected Ordering Information to include CY8C24423A-24LTXI and CY8C24423A-24LTXIT
*I	2619935	OGNE/AESA	12/11/2008	Changed title to “CY8C24123A, CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip™” Updated package diagram 001-30999 to *A. Added note on digital signaling in DC Analog Reference Specifications on page 27. Added Die Sales information note to Ordering Information on page 53.
*J	2692871	DPT/PYRS	04/16/2009	Updated Max package thickness for 32-pin QFN package Formatted Notes Updated “Getting Started” on page 4 Updated “Development Tools” on page 5 and “Designing with PSoC Designer” on page 6

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