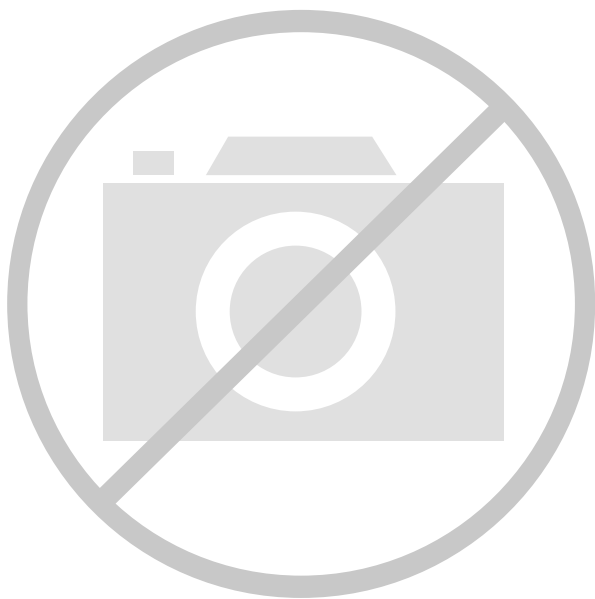




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

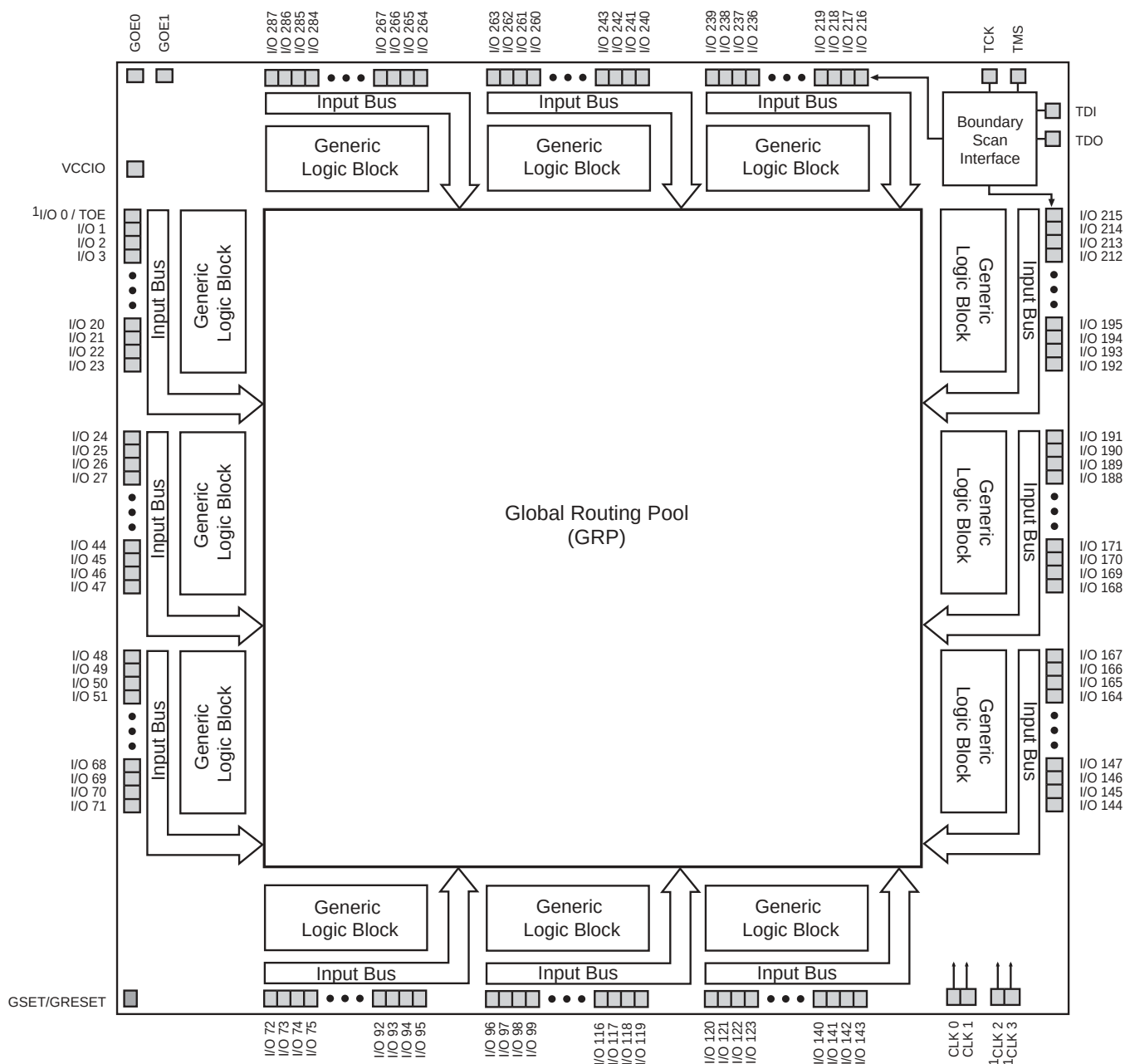
Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	12
Number of Macrocells	384
Number of Gates	18000
Number of I/O	288
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-5384va-100lb388

Functional Block Diagram

Figure 1. ispLSI 5384VA Functional Block Diagram (388 BGA Option)



1. CLK2, CLK3 and TOE signals are multiplexed with I/O signals. Which I/O is multiplexed is determined by the package type used – see table below.

Package Type	Multiplexed Signals		
208 PQFP	I/O 89 / CLK2	I/O 98 / CLK3	I/O 0 / TOE
208 fpBGA	I/O 89 / CLK2	I/O 98 / CLK3	I/O 0 / TOE
272 BGA	I/O 119 / CLK2	I/O 131 / CLK3	I/O 0 / TOE
388 BGA	I/O 179 / CLK2	I/O 197 / CLK3	I/O 0 / TOE

ispLSI 5000V Description (Continued)

five extra product terms are used for shared GLB controls, set, reset, clock, clock enable and output enable.

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, which can be fed back through the Global Routing Pool. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of this feature to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flip flop.

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one line from each macrocell output and one line from each I/O pin.

The input buffer threshold has programmable TTL/3.3V/2.5V compatible levels. The output driver can source 4mA and sink 8mA in 3.3V mode. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows the output drivers to drive either 3.3V or 2.5V output levels while the device logic and the output current drive is always powered from 3.3V. The output drivers also

provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device.

The ispLSI 5000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 5000V Family Members

The ispLSI 5000V Family ranges from 256 macrocells to 512 macrocells and operates from a 3.3V power supply. All family members will be available with multiple package options. The ispLSI 5000VA Family device matrix showing the various bondout options is shown in the table below.

The interconnect structure (GRP) is very similar to Lattice's existing ispLSI 1000, 2000 and 3000 families, but with an enhanced interconnect structure for optimal pin locking and logic routing. This eliminates the need for registered I/O cells or an Output Routing Pool.

Table 1. ispLSI 5000VA Family

Device	GLBs	Macrocells	Package Type			
			208 fpBGA	208 PQFP	272 BGA	388 BGA
ispLSI 5256VA	8	256	144 I/O	144 I/O	192 I/O	—
ispLSI 5384VA	12	384	144 I/O	144 I/O	192 I/O	288 I/O
ispLSI 5512VA	16	512	—	144 I/O	192 I/O	288 I/O

Figure 3. ispLSI 5000V Generic Logic Block (GLB)

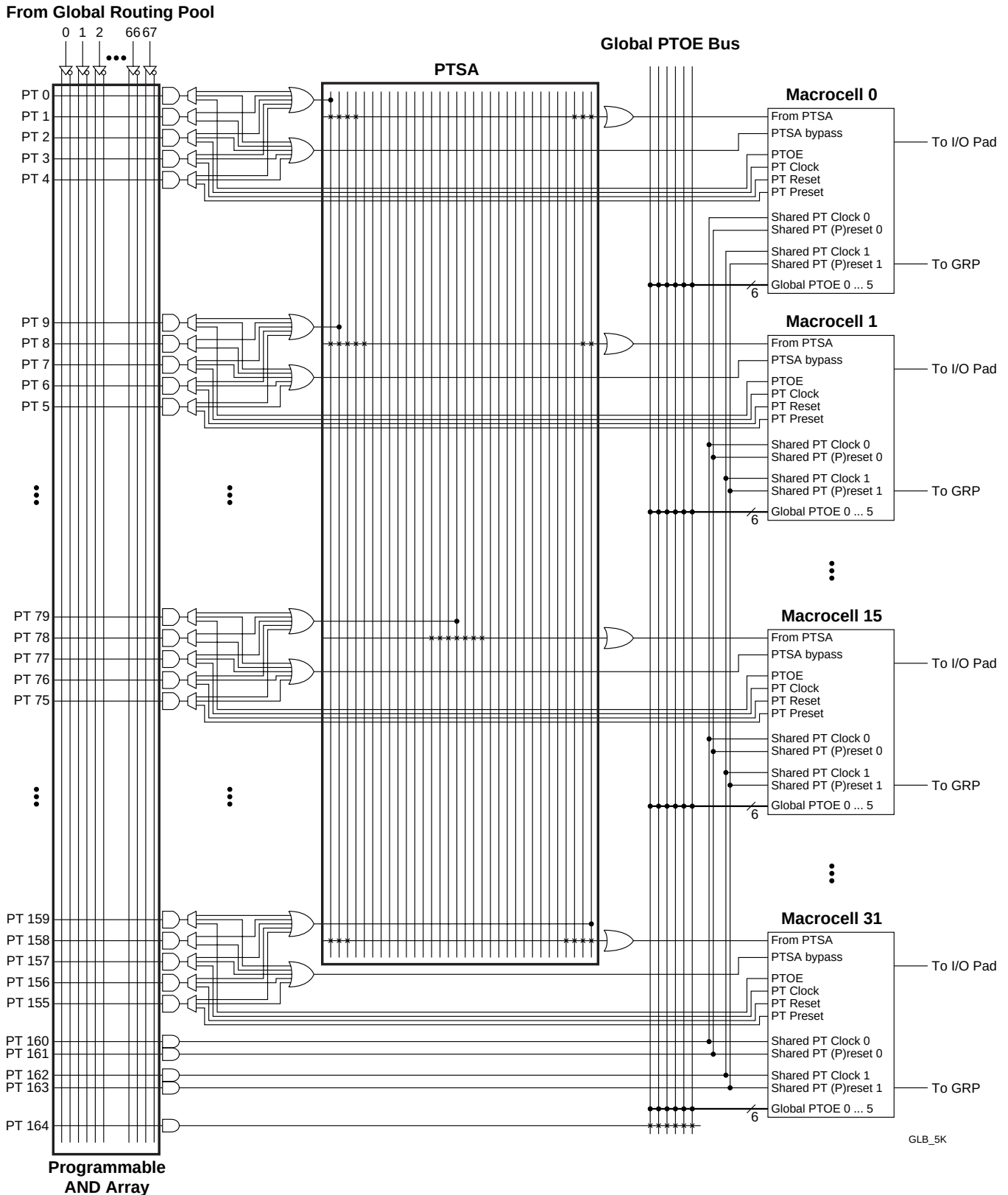
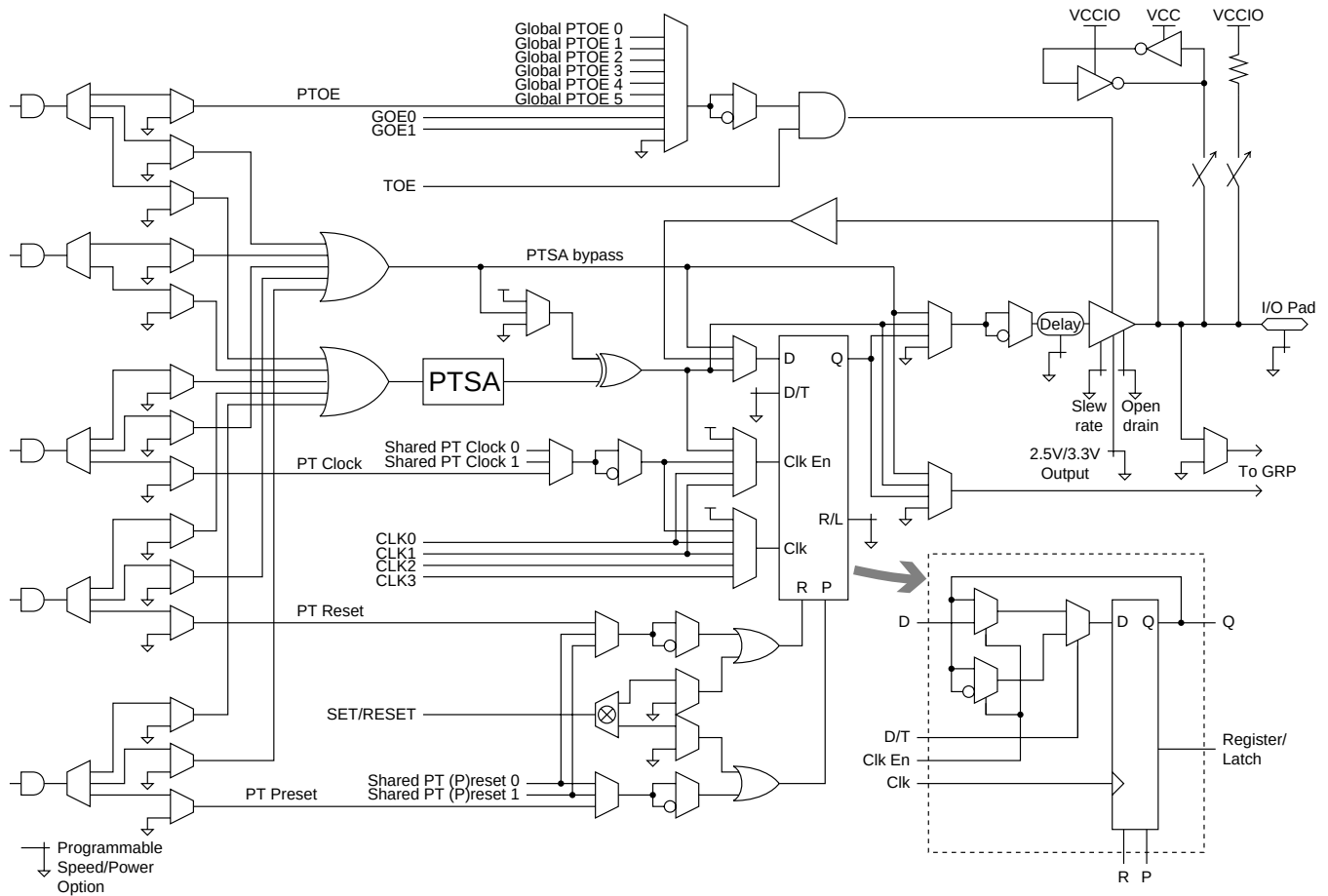


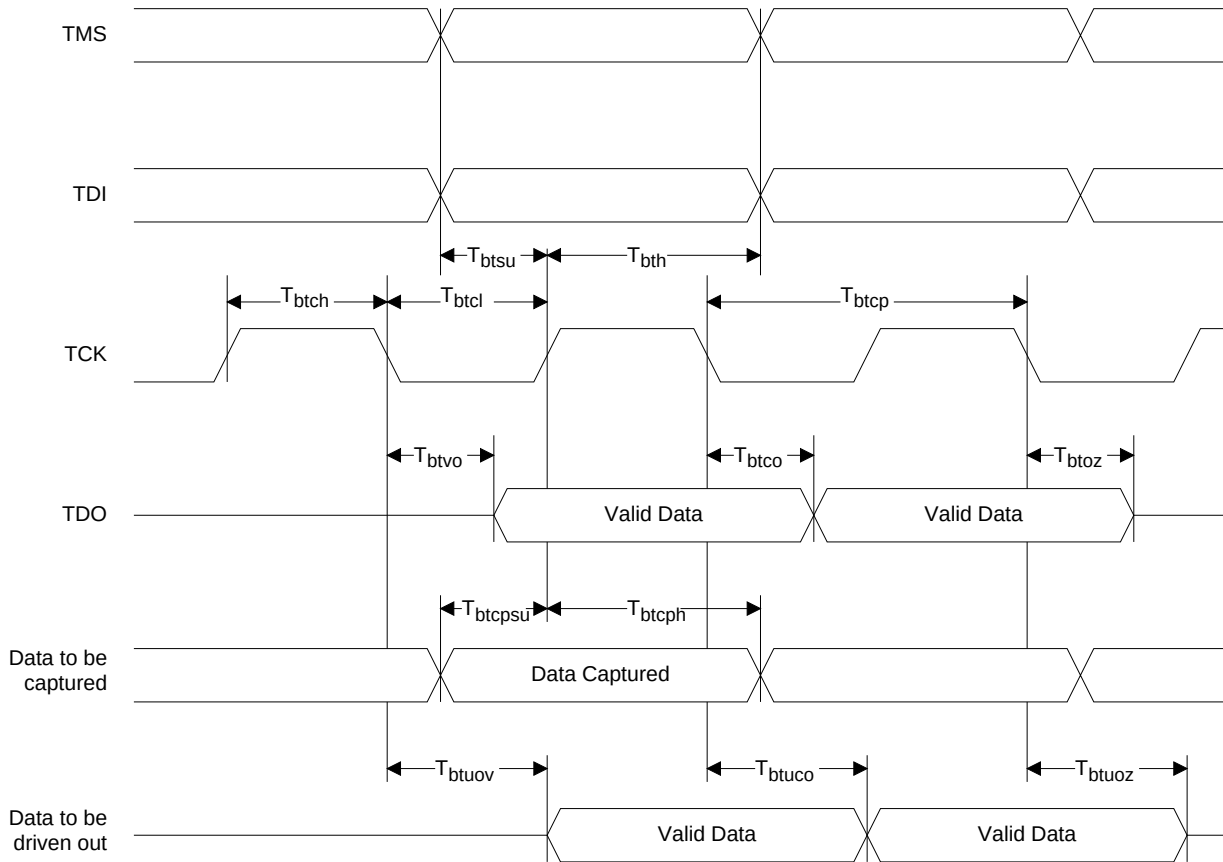
Figure 4. ispLSI 5000V Macrocell



The diagram illustrates the internal logic of the BSCAN block. It features three BSCAN Registers and three BSCAN Latches. The SCANIN signal (from the previous cell) is connected to the D input of the first register. The EXTEST signal is connected to the OE input of the first and second multiplexers. The TOE signal is connected to the output of the first multiplexer. The HIGHZ signal is connected to the output of the first multiplexer. The PROG_MODE signal is connected to the output of the second multiplexer. The output of the second multiplexer is connected to the I/O Pin. The output of the third multiplexer is connected to the SCANOUT signal (to the next cell). The control signals Shift DR, Clock DR, Update DR, and Reset are connected to the registers and latches.

The diagram shows a D flip-flop with four inputs and one output. The inputs are: 'Input Pin' (a trapezoidal symbol), 'SCANIN (from previous cell)' (a symbol with a triangle on the left), 'Shift DR' (a straight line), and 'Clock DR' (a straight line with a triangle on the left). The 'Input Pin' and 'SCANIN' inputs are connected to a 2-to-1 multiplexer. The output of the multiplexer is connected to the 'D' input of the flip-flop. The 'Shift DR' input is connected to the 'Q' input of the flip-flop. The 'Clock DR' input is connected to the clock input of the flip-flop. The output of the flip-flop is labeled 'SCANOUT (to next cell)'.

Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{btcp}	TCK [BSCAN test] clock pulse width	125	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	62.5	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	62.5	–	ns
t_{btsu}	TCK [BSCAN test] setup time	25	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsh}	BSCAN test Capture register setup time	25	–	ns
t_{btcpsh}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoZ}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

DC Electrical Characteristics for 2.5V Range¹

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCIO}	I/O Reference Voltage		2.3	–	2.7	V
V _{IL}	Input Low Voltage	$V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	-0.3	–	0.7	V
V _{IH}	Input High Voltage	$V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	1.7	–	5.25	V
V _{OL}	Output Low Voltage	V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OL} = 100μA	–	–	0.2	V
		V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OL} = 2mA	–	–	0.7	V
V _{OH}	Output High Voltage	V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OH} = -100μA	2.1	–	–	V
		V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OH} = -2mA	1.7	–	–	V

1. I/O voltage configuration must be set to V_{CCIO}.

2.5V/5384VA

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
I _{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL(Max)}$	–	–	-10	μA
I _{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2)V \leq V_{IN} \leq V_{CCIO}$	–	–	10	μA
		$V_{CCIO} \leq V_{IN} \leq 5.25V$	–	–	50	μA
I _{PU} ¹	I/O Active Pullup Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
I _{BHL}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL(max)}$	40	–	–	μA
I _{BHH}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH(min)}$	-40	–	–	μA
I _{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	550	μA
I _{BHLH}	Bus Hold High Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	-550	μA
I _{BHT}	Bus Hold Trip Points		V _{IL}	–	V _{IH}	V
I _{VCCIO}	Current Needed for V _{CCIO} Pin	All I/Os Pulled-up, (Total I/Os * I _{PUmax})	–	–	45	mA

1. Pullup is capable of pulling to a minimum voltage of V_{OH} under no-load conditions.

DC Char_5384VA

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST ³ COND.	#	DESCRIPTION ^{4,5}	-125		-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1⁶	A	1	Data Prop. Delay, 5PT Bypass	—	7.5	—	10	—	15	ns
tpd2⁶	A	2	Data Propagation Delay	—	9.5	—	13	—	19	ns
fmax	A	3	Clock Frequency with Internal Feedback ¹	125	—	100	—	70	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback, 1/(tsu2 + tco1)	91	—	69	—	45	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle ²	167	—	125	—	83	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clk, 5PT bypass	6	—	8	—	12	—	ns
tco1⁶	A	7	GLB Reg. Clock to Output Delay	—	4	—	5.5	—	8	ns
th1	—	8	GLB Reg. Hold Time after Clock, 5PT bypass	0	—	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	7	—	9	—	14	—	ns
th2	—	10	GLB Reg. Hold Time after Clock	0	—	0	—	0	—	ns
tsu3 (CLK0/1)	—	11	GLB Reg. Setup Time before Clock, Input Reg. Path (CLK0/1)	4.5	—	6	—	9	—	ns
tsu3 (CLK2/3)	—	12	GLB Reg. Setup Time before Clock, Input Reg. Path (CLK2/3)	3.5	—	5	—	7	—	ns
th3 (CLK0/1)	—	13	GLB Reg. Hold Time after Clock, Input Reg. Path (CLK0/1)	0	—	0	—	0	—	ns
th3 (CLK2/3)	—	14	GLB Reg. Hold Time after Clock, Input Reg. Path (CLK2/3)	0	—	0	—	0	—	ns
tr1	A	15	Ext. Reset Pin to Output Delay	—	15	—	20	—	30	ns
trw1	—	16	Ext. Reset Pulse Duration	7	—	9	—	14	—	ns
tp toe/dis	B/C	17	Local Product Term Output Enable/Disable	—	9	—	12	—	18	ns
tg toe/dis	B/C	18	Global Product Term Output Enable/Disable	—	18	—	24	—	30	ns
tgoe/dis	B/C	19	Global OE Input to Output Enable/Disable	—	6	—	8	—	12	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	3	—	4	—	6	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	3	—	4	—	6	—	ns

1. Standard 32-bit counter using GRP feedback.
2. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
3. Reference Switching Test Conditions section.
4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, and CLK0.
5. Timing parameters measured using normal active output driver.
6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

Timing Ext.5384VA/4.0.eps

Internal Timing Parameters¹

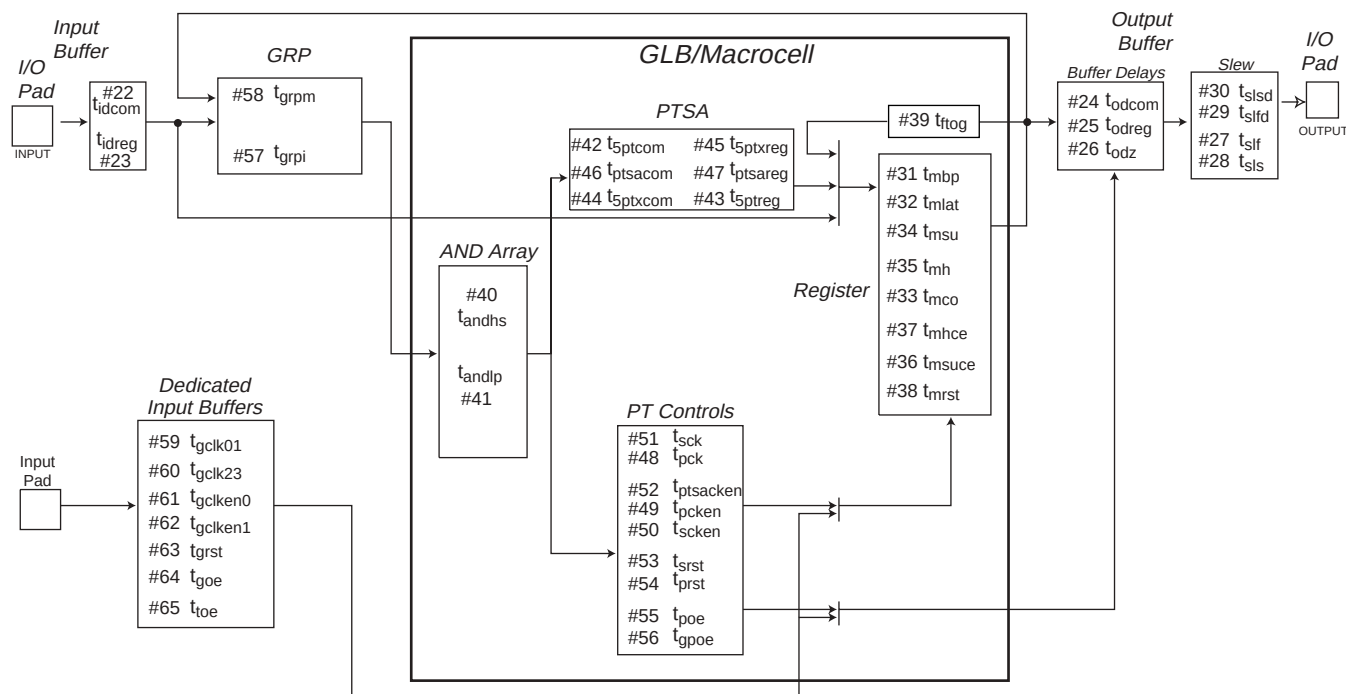
Over Recommended Operating Conditions

PARAM	#	DESCRIPTION	-125		-100		-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
GRP									
tgrpi	57	GRP Delay from I/O Pad	–	1.5	–	2	–	3	ns
tgrpm	58	GRP Delay from Macrocell	–	1.0	–	1.2	–	1.2	ns
Global Control Delays									
tgclk01	59	Global Clock 0 or 1 Delay	–	1.2	–	1.7	–	2.4	ns
tgclk23	60	Global Clock 2 or 3 Delay	–	2.2	–	2.7	–	4.4	ns
tgclken0	61	Global CLKEN 0 Delay	–	1.7	–	2.4	–	3.4	ns
tgclken1	62	Global CLKEN 1 Delay	–	2.7	–	3.4	–	5.4	ns
tgrst	63	Global Set/Reset Delay	–	12.2	–	15.8	–	23.4	ns
tgoe	64	Global OE Delay	–	4.7	–	6.3	–	9.4	ns
ttoe	65	Test OE Delay	–	4.7	–	6.2	–	9.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
Refer to Timing Model in this data sheet for further details.

Timing Rev 4.0

ispLSI 5384VA Timing Model



208-Ball fpBGA Signal Locations

Signal	Ball
GOE0, GOE1	P9, P10
TOE / I/O0	K1
GSET/GRST	H14
TCK	K2
TDI	K3
TDO	G14
TMS	J1
CLK0, CLK1	A7, B8
CLK2 / I/O89	B13
CLK3 / I/O98	A11
VCCIO	H15
GND	D10, D12, D13, D5, D7, D8, E4, F13, G4, G8, G9, H10, H13, H7, J10, J13, J4, J7, K8, K9, L13, L4, M13, N10, N12, N4, N5, N7, N8
VCC	D11, D4, D6, D9, E13, F4, G10, G13, G7, H4, H8, H9, J8, J9, K10, K13, K4, K7, M4, N11, N13, N6, N9
NC ¹	E15, C14

1. NCs are not to be connected to any active signals, VCC or GND.

208-Ball fpBGA I/O Locations (Sorted by I/O)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	K1	24	T4	48	R12	72	G16	96	C11	120	C3
1	L2	25	T5	49	P14	73	F14	97	B11	121	C2
2	L1	26	R7	50	P13	74	G15	98*	A11	122	B3
3	L3	27	P6	51	R13	75	F16	99	B10	123	B2
4	M1	28	T6	52	R15	76	E14	100	A10	124	A1
5	M2	29	T7	53	P15	77	F15	101	C10	125	D2
6	M3	30	R8	54	R16	78	E16	102	B9	126	B1
7	N1	31	P8	55	P16	79	D16	103	C9	127	D3
8	N3	32	P7	56	N15	80	C16	104	A9	128	E2
9	N2	33	T8	57	N14	81	B16	105	A8	129	C1
10	P2	34	T9	58	M14	82	D15	106	C8	130	E3
11	P1	35	R9	59	N16	83	D14	107	C7	131	D1
12	R1	36	R10	60	M15	84	A16	108	B7	132	F2
13	R2	37	T10	61	M16	85	C15	109	A6	133	E1
14	R3	38	T11	62	L14	86	B15	110	A5	134	F1
15	P3	39	T12	63	L15	87	A15	111	C6	135	G2
16	T1	40	T13	64	L16	88	B14	112	B6	136	F3
17	P4	41	T14	65	K14	89*	B13	113	A4	137	H2
18	R4	42	P11	66	K15	90	C13	114	A3	138	H3
19	R5	43	P12	67	K16	91	A14	115	A2	139	G3
20	P5	44	R11	68	J14	92	C12	116	C5	140	G1
21	T2	45	T15	69	J15	93	B12	117	B5	141	H1
22	R6	46	T16	70	J16	94	A13	118	B4	142	J2
23	T3	47	R14	71	H16	95	A12	119	C4	143	J3

* I/O 89 is multiplexed with CLK2, I/O 98 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

208-Ball fpBGA I/O Locations (Sorted by Ball)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
124	A01	97	B11	83	D14	143	J03	56	N15	35	R09
115	A02	93	B12	82	D15	68	J14	59	N16	36	R10
114	A03	89*	B13	79	D16	69	J15	11	P01	44	R11
113	A04	88	B14	133	E01	70	J16	10	P02	48	R12
110	A05	86	B15	128	E02	0*	K01	15	P03	51	R13
109	A06	81	B16	130	E03	65	K14	17	P04	47	R14
105	A08	129	C01	76	E14	66	K15	20	P05	52	R15
104	A09	121	C02	78	E16	67	K16	27	P06	54	R16
100	A10	120	C03	134	F01	2	L01	32	P07	16	T01
98*	A11	119	C04	132	F02	1	L02	31	P08	21	T02
95	A12	116	C05	136	F03	3	L03	42	P11	23	T03
94	A13	111	C06	73	F14	62	L14	43	P12	24	T04
91	A14	107	C07	77	F15	63	L15	50	P13	25	T05
87	A15	106	C08	75	F16	64	L16	49	P14	28	T06
84	A16	103	C09	140	G01	4	M01	53	P15	29	T07
126	B01	101	C10	135	G02	5	M02	55	P16	33	T08
123	B02	96	C11	139	G03	6	M03	12	R01	34	T09
122	B03	92	C12	74	G15	58	M14	13	R02	37	T10
118	B04	90	C13	72	G16	60	M15	14	R03	38	T11
117	B05	85	C15	141	H01	61	M16	18	R04	39	T12
112	B06	80	C16	137	H02	7	N01	19	R05	40	T13
108	B07	131	D01	138	H03	9	N02	22	R06	41	T14
102	B09	125	D02	71	H16	8	N03	26	R07	45	T15
99	B10	127	D03	142	J02	57	N14	30	R08	46	T16

* I/O 89 is multiplexed with CLK2, I/O 98 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

272-Ball BGA Signal Locations

Signal	Ball
GOE0, GOE1	V11, U11
TOE / I/O 0	M2
GSET/GRST	J18
TCK	L4
TDI	M1
TDO	J20
TMS	L3
CLK0, CLK1	C10, D10
CLK2 / I/O 119	A18
CLK3 / I/O 131	B13
VCCIO	J19
GND	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17
VCC	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15
NC ¹	U1, W1, E2, U2, W2, Y2, B3, C3, D3, U3, C5, W4, T4, Y12, A17, T17, W17, B18, C18, B19, C19, D19, W19, B20, T20, W20, Y20, P19, R3

1. NCs are not to be connected to any active signals, VCC or GND.

272-Ball BGA I/O Locations (Sorted by I/O)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	M2	32	W7	64	U16	96	J17	128	B14	160	A3
1	M3	33	Y7	65	V17	97	H20	129	A14	161	D5
2	M4	34	V8	66	W18	98	H19	130	C13	162	C4
3	N1	35	W8	67	Y19	99	H18	131*	B13	163	B2
4	N2	36	Y8	68	V18	100	G20	132	A13	164	A2
5	N3	37	U9	69	V19	101	G19	133	D12	165	B1
6	P1	38	V9	70	U19	102	F20	134	C12	166	C2
7	P2	39	W9	71	U18	103	G18	135	B12	167	D2
8	R1	40	Y9	72	V20	104	F19	136	A12	168	E4
9	P3	41	W10	73	U20	105	E20	137	B11	169	C1
10	R2	42	V10	74	T18	106	G17	138	C11	170	D1
11	T1	43	Y10	75	T19	107	F18	139	A11	171	E3
12	P4	44	Y11	76	R18	108	E19	140	A10	172	E1
13	T2	45	W11	77	P17	109	D20	141	B10	173	F3
14	T3	46	W12	78	R19	110	E18	142	A9	174	G4
15	V1	47	V12	79	R20	111	C20	143	B9	175	F2
16	V2	48	U12	80	P18	112	E17	144	C9	176	F1
17	V3	49	Y13	81	P20	113	D18	145	D9	177	G3
18	Y1	50	W13	82	N18	114	A20	146	A8	178	G2
19	W3	51	V13	83	N19	115	A19	147	B8	179	G1
20	V4	52	Y14	84	N20	116	B17	148	C8	180	H3
21	U5	53	W14	85	M17	117	C17	149	A7	181	H2
22	Y3	54	Y15	86	M18	118	D16	150	B7	182	H1
23	Y4	55	V14	87	M19	119*	A18	151	A6	183	J4
24	V5	56	W15	88	M20	120	C16	152	C7	184	J3
25	W5	57	Y16	89	L19	121	B16	153	B6	185	J2
26	Y5	58	U14	90	L18	122	A16	154	A5	186	J1
27	V6	59	V15	91	L20	123	C15	155	D7	187	K2
28	U7	60	W16	92	K20	124	D14	156	C6	188	K3
29	W6	61	Y17	93	K19	125	B15	157	B5	189	K1
30	Y6	62	V16	94	K18	126	A15	158	A4	190	L1
31	V7	63	Y18	95	K17	127	C14	159	B4	191	L2

* I/O 119 is multiplexed with CLK2, I/O 131 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

272-Ball BGA I/O Locations (Sorted by Ball)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
164	A02	121	B16	108	E19	93	K19	11	T01	72	V20
160	A03	116	B17	105	E20	92	K20	13	T02	19	W03
158	A04	169	C01	176	F01	190	L01	14	T03	25	W05
154	A05	166	C02	175	F02	191	L02	74	T18	29	W06
151	A06	162	C04	173	F03	90	L18	75	T19	32	W07
149	A07	156	C06	107	F18	89	L19	21	U05	35	W08
146	A08	152	C07	104	F19	91	L20	28	U07	39	W09
142	A09	148	C08	102	F20	0*	M02	37	U09	41	W10
140	A10	144	C09	179	G01	1	M03	48	U12	45	W11
139	A11	138	C11	178	G02	2	M04	58	U14	46	W12
136	A12	134	C12	177	G03	85	M17	64	U16	50	W13
132	A13	130	C13	174	G04	86	M18	71	U18	53	W14
129	A14	127	C14	106	G17	87	M19	70	U19	56	W15
126	A15	123	C15	103	G18	88	M20	73	U20	60	W16
122	A16	120	C16	101	G19	3	N01	15	V01	66	W18
119*	A18	117	C17	100	G20	4	N02	16	V02	18	Y01
115	A19	111	C20	182	H01	5	N03	17	V03	22	Y03
114	A20	170	D01	181	H02	82	N18	20	V04	23	Y04
165	B01	167	D02	180	H03	83	N19	24	V05	26	Y05
163	B02	161	D05	99	H18	84	N20	27	V06	30	Y06
159	B04	155	D07	98	H19	6	P01	31	V07	33	Y07
157	B05	145	D09	97	H20	7	P02	34	V08	36	Y08
153	B06	133	D12	186	J01	9	P03	38	V09	40	Y09
150	B07	124	D14	185	J02	12	P04	42	V10	43	Y10
147	B08	118	D16	184	J03	77	P17	47	V12	44	Y11
143	B09	113	D18	183	J04	80	P18	51	V13	49	Y13
141	B10	109	D20	96	J17	81	P20	55	V14	52	Y14
137	B11	172	E01	189	K01	8	R01	59	V15	54	Y15
135	B12	171	E03	187	K02	10	R02	62	V16	57	Y16
131*	B13	168	E04	188	K03	76	R18	65	V17	61	Y17
128	B14	112	E17	95	K17	78	R19	68	V18	63	Y18
125	B15	110	E18	94	K18	79	R20	69	V19	67	Y19

* I/O 119 is multiplexed with CLK2, I/O 131 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

388-Ball BGA I/O Locations (Sorted by I/O)

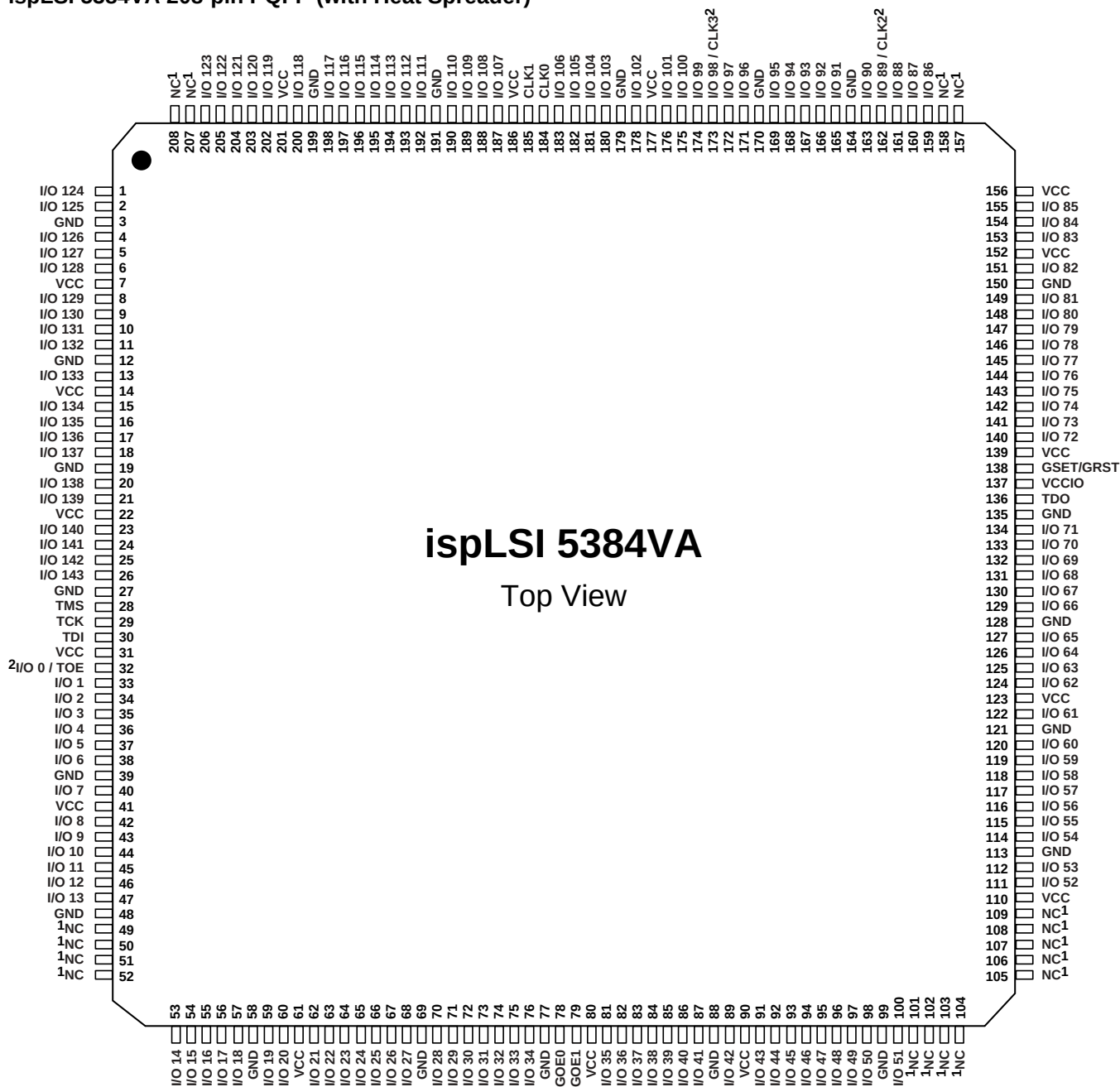
I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	T1	48	AC9	96	AE23	144	M24	192	D18	240	B4
1	R4	49	AF8	97	AC22	145	L26	193	A19	241	D5
2	U2	50	AD8	98	AF23	146	M23	194	C19	242	A4
3	T3	51	AE9	99	AD22	147	K25	195	B18	243	C5
4	U1	52	AF9	100	AE24	148	L24	196	A18	244	B3
5	U4	53	AE10	101	AD23	149	K26	197*	B17	245	C4
6	V2	54	AD9	102	AF24	150	K23	198	C18	246	A3
7	U3	55	AF10	103	AE26	151	J25	199	A17	247	B1
8	V1	56	AC10	104	AD25	152	K24	200	D17	248	C2
9	W2	57	AE11	105	AD26	153	J26	201	B16	249	C1
10	W1	58	AD10	106	AC24	154	H25	202	C17	250	D3
11	V3	59	AF11	107	AC26	155	H26	203	A16	251	D1
12	Y2	60	AE12	108	AB25	156	J24	204	B15	252	E2
13	W4	61	AF12	109	AB23	157	G25	205	A15	253	E4
14	Y1	62	AD11	110	AB24	158	H23	206	C16	254	E3
15	W3	63	AE13	111	AB26	159	G26	207	B14	255	E1
16	AA2	64	AC12	112	AA25	160	H24	208	D15	256	F2
17	Y4	65	AF13	113	Y23	161	F25	209	A14	257	G4
18	AA1	66	AD12	114	AA24	162	G23	210	C15	258	F3
19	Y3	67	AE14	115	AA26	163	F26	211	B13	259	F1
20	AB2	68	AC14	116	Y25	164	G24	212	D13	260	G2
21	AB1	69	AE15	117	Y26	165	E25	213	B12	261	G1
22	AA3	70	AD14	118	Y24	166	E26	214	C13	262	G3
23	AC2	71	AF15	119	W25	167	F24	215	A12	263	H2
24	AB4	72	AE16	120	V23	168	D25	216	B11	264	J4
25	AC1	73	AD15	121	W26	169	E23	217	C12	265	H1
26	AB3	74	AF16	122	W24	170	D26	218	A11	266	H3
27	AD2	75	AC15	123	V25	171	C25	219	D12	267	J2
28	AC3	76	AE17	124	V26	172	D24	220	B10	268	J1
29	AD1	77	AD16	125	U25	173	C26	221	C11	269	K2
30	AF2	78	AF17	126	V24	174	A25	222	A10	270	J3
31	AE3	79	AC17	127	U26	175	B24	223	D10	271	K1
32	AF3	80	AE18	128	U23	176	A24	224	B9	272	K4
33	AE4	81	AD17	129	T25	177	B23	225	C10	273	L2
34	AD4	82	AF18	130	U24	178	C23	226	A9	274	K3
35	AF4	83	AE19	131	T26	179*	A23	227	B8	275	M2
36	AE5	84	AD18	132	R25	180	B22	228	A8	276	M1
37	AC5	85	AE20	133	R26	181	D22	229	B7	277	L3
38	AD5	86	AC19	134	T24	182	C22	230	D8	278	N2
39	AF5	87	AF20	135	P25	183	A22	231	A7	279	M4
40	AE6	88	AD19	136	R23	184	B21	232	C8	280	N1
41	AC7	89	AE21	137	P26	185	D20	233	B6	281	M3
42	AD6	90	AC20	138	R24	186	C21	234	D7	282	P2
43	AF6	91	AF21	139	N25	187	A21	235	A6	283	P4
44	AE7	92	AD20	140	N23	188	B20	236	C7	284	P1
45	AF7	93	AE22	141	N26	189	A20	237	B5	285	N3
46	AD7	94	AF22	142	P24	190	C20	238	A5	286	R2
47	AE8	95	AD21	143	M25	191	B19	239	C6	287	P3

* I/O 179 is multiplexed with CLK2, I/O 197 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

388-Ball BGA I/O Locations (Sorted by Ball)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
246	A03	243	C05	261	G01	282	P02	16	AA02	99	AD22
242	A04	239	C06	260	G02	287	P03	22	AA03	101	AD23
238	A05	236	C07	262	G03	283	P04	114	AA24	104	AD25
235	A06	232	C08	257	G04	142	P24	112	AA25	105	AD26
231	A07	225	C10	162	G23	135	P25	115	AA26	31	AE03
228	A08	221	C11	164	G24	137	P26	21	AB01	33	AE04
226	A09	217	C12	157	G25	286	R02	20	AB02	36	AE05
222	A10	214	C13	159	G26	1	R04	26	AB03	40	AE06
218	A11	210	C15	265	H01	136	R23	24	AB04	44	AE07
215	A12	206	C16	263	H02	138	R24	109	AB23	47	AE08
209	A14	202	C17	266	H03	132	R25	110	AB24	51	AE09
205	A15	198	C18	158	H23	133	R26	108	AB25	53	AE10
203	A16	194	C19	160	H24	0*	T01	111	AB26	57	AE11
199	A17	190	C20	154	H25	3	T03	25	AC01	60	AE12
196	A18	186	C21	155	H26	134	T24	23	AC02	63	AE13
193	A19	182	C22	268	J01	129	T25	28	AC03	67	AE14
189	A20	178	C23	267	J02	131	T26	37	AC05	69	AE15
187	A21	171	C25	270	J03	4	U01	41	AC07	72	AE16
183	A22	173	C26	264	J04	2	U02	48	AC09	76	AE17
179*	A23	251	D01	156	J24	7	U03	56	AC10	80	AE18
176	A24	250	D03	151	J25	5	U04	64	AC12	83	AE19
174	A25	241	D05	153	J26	128	U23	68	AC14	85	AE20
247	B01	234	D07	271	K01	130	U24	75	AC15	89	AE21
244	B03	230	D08	269	K02	125	U25	79	AC17	93	AE22
240	B04	223	D10	274	K03	127	U26	86	AC19	96	AE23
237	B05	219	D12	272	K04	8	V01	90	AC20	100	AE24
233	B06	212	D13	150	K23	6	V02	97	AC22	103	AE26
229	B07	208	D15	152	K24	11	V03	106	AC24	30	AF02
227	B08	200	D17	147	K25	120	V23	107	AC26	32	AF03
224	B09	192	D18	149	K26	126	V24	29	AD01	35	AF04
220	B10	185	D20	273	L02	123	V25	27	AD02	39	AF05
216	B11	181	D22	277	L03	124	V26	34	AD04	43	AF06
213	B12	172	D24	148	L24	10	W01	38	AD05	45	AF07
211	B13	168	D25	145	L26	9	W02	42	AD06	49	AF08
207	B14	170	D26	276	M01	15	W03	46	AD07	52	AF09
204	B15	255	E01	275	M02	13	W04	50	AD08	55	AF10
201	B16	252	E02	281	M03	122	W24	54	AD09	59	AF11
197*	B17	254	E03	279	M04	119	W25	58	AD10	61	AF12
195	B18	253	E04	146	M23	121	W26	62	AD11	65	AF13
191	B19	169	E23	144	M24	14	Y01	66	AD12	71	AF15
188	B20	165	E25	143	M25	12	Y02	70	AD14	74	AF16
184	B21	166	E26	280	N01	19	Y03	73	AD15	78	AF17
180	B22	259	F01	278	N02	17	Y04	77	AD16	82	AF18
177	B23	256	F02	285	N03	113	Y23	81	AD17	87	AF20
175	B24	258	F03	140	N23	118	Y24	84	AD18	91	AF21
249	C01	167	F24	139	N25	116	Y25	88	AD19	94	AF22
248	C02	161	F25	141	N26	117	Y26	92	AD20	98	AF23
245	C04	163	F26	284	P01	18	AA01	95	AD21	102	AF24

* I/O 179 is multiplexed with CLK2, I/O 197 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

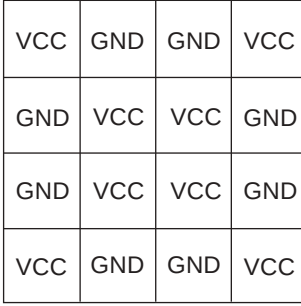
ispLSI 5384VA 208-pin PQFP (with Heat Spreader)

208-POFP/5384V

1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Signal Configuration

ispLSI 5384VA 208-ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O 84	I/O 87	I/O 91	I/O 94	I/O 95	CLK3/ I/O98	I/O 100	I/O 104	I/O 105	CLK 0	I/O 109	I/O 110	I/O 113	I/O 114	I/O 115	I/O 124	A
B	I/O 81	I/O 86	I/O 88	CLK2/ I/O89	I/O 93	I/O 97	I/O 99	I/O 102	CLK 1	I/O 108	I/O 112	I/O 117	I/O 118	I/O 122	I/O 123	I/O 126	B
C	I/O 80	I/O 85	NC ¹	I/O 90	I/O 92	I/O 96	I/O 101	I/O 103	I/O 106	I/O 107	I/O 111	I/O 116	I/O 119	I/O 120	I/O 121	I/O 129	C
D	I/O 79	I/O 82	I/O 83	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O 127	I/O 125	I/O 131	D
E	I/O 78	NC ¹	I/O 76	VCC	 ispLSI 5384VA Bottom View								GND	I/O 130	I/O 128	I/O 133	E
F	I/O 75	I/O 77	I/O 73	GND									VCC	I/O 136	I/O 132	I/O 134	F
G	I/O 72	I/O 74	TDO	VCC									GND	I/O 139	I/O 135	I/O 140	G
H	I/O 71	VCCIO	GSET/ GRST	GND									VCC	I/O 138	I/O 137	I/O 141	H
J	I/O 70	I/O 69	I/O 68	GND									GND	I/O 143	I/O 142	TMS	J
K	I/O 67	I/O 66	I/O 65	VCC									VCC	TDI	TCK	TOE/ I/O0	K
L	I/O 64	I/O 63	I/O 62	GND									GND	I/O 3	I/O 1	I/O 2	L
M	I/O 61	I/O 60	I/O 58	GND									VCC	I/O 6	I/O 5	I/O 4	M
N	I/O 59	I/O 56	I/O 57	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	I/O 8	I/O 9	I/O 7	N
P	I/O 55	I/O 53	I/O 49	I/O 50	I/O 43	I/O 42	GOE1	GOE0	I/O 31	I/O 32	I/O 27	I/O 20	I/O 17	I/O 15	I/O 10	I/O 11	P
R	I/O 54	I/O 52	I/O 47	I/O 51	I/O 48	I/O 44	I/O 36	I/O 35	I/O 30	I/O 26	I/O 22	I/O 19	I/O 18	I/O 14	I/O 13	I/O 12	R
T	I/O 46	I/O 45	I/O 41	I/O 40	I/O 39	I/O 38	I/O 37	I/O 34	I/O 33	I/O 29	I/O 28	I/O 25	I/O 24	I/O 23	I/O 21	I/O 16	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

208 fpBGA/5384VA

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispLSI 5384VA 272-ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O 114	I/O 115	CLK2/ I/O 119	NC ¹	I/O 122	I/O 126	I/O 129	I/O 132	I/O 136	I/O 139	I/O 140	I/O 142	I/O 146	I/O 149	I/O 151	I/O 154	I/O 158	I/O 160	I/O 164	GND	A
B	NC ¹	NC ¹	NC ¹	I/O 116	I/O 121	I/O 125	I/O 128	CLK3/ I/O 131	I/O 135	I/O 137	I/O 141	I/O 143	I/O 147	I/O 150	I/O 153	I/O 157	I/O 159	NC ¹	I/O 163	I/O 165	B
C	I/O 111	NC ¹	NC ¹	I/O 117	I/O 120	I/O 123	I/O 127	I/O 130	I/O 134	I/O 138	CLK0	I/O 144	I/O 148	I/O 152	I/O 156	NC ¹	I/O 162	NC ¹	I/O 166	I/O 169	C
D	I/O 109	NC ¹	I/O 113	GND	I/O 118	VCC	I/O 124	GND	I/O 133	VCC	CLK1	I/O 145	GND	I/O 155	VCC	I/O 161	GND	NC ¹	I/O 167	I/O 170	D
E	I/O 105	I/O 108	I/O 110	I/O 112	ispLSI 5384VA Bottom View GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND												I/O 168	I/O 171	NC ¹	I/O 172	E
F	I/O 102	I/O 104	I/O 107	VCC													VCC	I/O 173	I/O 175	I/O 176	F
G	I/O 100	I/O 101	I/O 103	I/O 106													I/O 174	I/O 177	I/O 178	I/O 179	G
H	I/O 97	I/O 98	I/O 99	GND													GND	I/O 180	I/O 181	I/O 182	H
J	TDO	VCCIO	SET/ RST	I/O 96													I/O 183	I/O 184	I/O 185	I/O 186	J
K	I/O 92	I/O 93	I/O 94	I/O 95													VCC	I/O 188	I/O 187	I/O 189	K
L	I/O 91	I/O 89	I/O 90	VCC													TCK	TMS	I/O 191	I/O 190	L
M	I/O 88	I/O 87	I/O 86	I/O 85													I/O 2	I/O 1	TOE I/O 0	TDI	M
N	I/O 84	I/O 83	I/O 82	GND													GND	I/O 5	I/O 4	I/O 3	N
P	I/O 81	NC ¹	I/O 80	I/O 77													I/O 12	I/O 9	I/O 7	I/O 6	P
R	I/O 79	I/O 78	I/O 76	VCC	VCC	NC ¹	I/O 10	I/O 8	R												
T	NC ¹	I/O 75	I/O 74	NC ¹	NC ¹	I/O 14	I/O 13	I/O 11	T												
U	I/O 73	I/O 70	I/O 71	GND	I/O 64	VCC	I/O 58	GND	I/O 48	GOE1	VCC	I/O 37	GND	I/O 28	VCC	I/O 21	GND	NC ¹	NC ¹	NC ¹	U
V	I/O 72	I/O 69	I/O 68	I/O 65	I/O 62	I/O 59	I/O 55	I/O 51	I/O 47	GOE0	I/O 42	I/O 38	I/O 34	I/O 31	I/O 27	I/O 24	I/O 20	I/O 17	I/O 16	I/O 15	V
W	NC ¹	NC ¹	I/O 66	NC ¹	I/O 60	I/O 56	I/O 53	I/O 50	I/O 46	I/O 45	I/O 41	I/O 39	I/O 35	I/O 32	I/O 29	I/O 25	NC ¹	I/O 19	NC ¹	NC ¹	W
Y	NC ¹	I/O 67	I/O 63	I/O 61	I/O 57	I/O 54	I/O 52	I/O 49	NC ¹	I/O 44	I/O 43	I/O 40	I/O 36	I/O 33	I/O 30	I/O 26	I/O 23	I/O 22	NC ¹	I/O 18	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

1. NCs are not to be connected to any active signals, Vcc or GND.

272 BGA/5384VA

Note: Ball A1 indicator dot on top side of package.

Pin Configuration

ispLSI 5384VA 388-ball BGA

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O 174	I/O 176	I/O 179/ CLK2	I/O 183	I/O 187	I/O 189	I/O 193	I/O 196	I/O 199	I/O 203	I/O 205	I/O 209	CLK0	I/O 215	I/O 218	I/O 222	I/O 226	I/O 228	I/O 231	I/O 235	I/O 238	I/O 242	I/O 246	GND	GND	A
B	GND	GND	I/O 175	I/O 177	I/O 180	I/O 184	I/O 188	I/O 191	I/O 195	I/O 197/ CLK3	I/O 201	I/O 204	I/O 207	I/O 211	I/O 213	I/O 216	I/O 220	I/O 224	I/O 227	I/O 229	I/O 233	I/O 237	I/O 240	I/O 244	GND	I/O 247	B
C	I/O 173	I/O 171	GND	I/O 178	I/O 182	I/O 186	I/O 190	I/O 194	I/O 198	I/O 202	I/O 206	I/O 210	CLK1	I/O 214	I/O 217	I/O 221	I/O 225	NC ¹	I/O 232	I/O 236	I/O 239	I/O 243	I/O 245	GND	I/O 248	I/O 249	C
D	I/O 170	I/O 168	I/O 172	GND	I/O 181	VCC	I/O 185	GND	I/O 192	I/O 200	VCC	I/O 208	GND	I/O 212	I/O 219	VCC	I/O 223	GND	I/O 230	I/O 234	VCC	I/O 241	GND	I/O 250	NC ¹	I/O 251	D
E	I/O 166	I/O 165	NC ¹	I/O 169																			I/O 253	I/O 254	I/O 252	I/O 255	E
F	I/O 163	I/O 161	I/O 167	VCC																			VCC	I/O 258	I/O 256	I/O 259	F
G	I/O 159	I/O 157	I/O 164	I/O 162																			I/O 257	I/O 262	I/O 260	I/O 261	G
H	I/O 155	I/O 154	I/O 160	I/O 158																			GND	I/O 266	I/O 263	I/O 265	H
J	I/O 153	I/O 151	I/O 156	GND																			I/O 264	I/O 270	I/O 267	I/O 268	J
K	I/O 149	I/O 147	I/O 152	I/O 150																			I/O 272	I/O 274	I/O 269	I/O 271	K
L	I/O 145	SET/ RST	I/O 148	VCC																			VCC	I/O 277	I/O 273	NC ¹	L
M	VCCIO	I/O 143	I/O 144	I/O 146																			I/O 279	I/O 281	I/O 275	I/O 276	M
N	I/O 141	I/O 139	TDO	I/O 140																			GND	I/O 285	I/O 278	I/O 280	N
P	I/O 137	I/O 135	I/O 142	GND																			I/O 283	I/O 287	I/O 282	I/O 284	P
R	I/O 133	I/O 132	I/O 138	I/O 136																			I/O 1	TDI	I/O 286	TMS	R
T	I/O 131	I/O 129	I/O 134	VCC																			VCC	I/O 3	TCK	I/O 0/ TOE	T
U	I/O 127	I/O 125	I/O 130	I/O 128																			I/O 5	I/O 7	I/O 2	I/O 4	U
V	I/O 124	I/O 123	I/O 126	I/O 120																			GND	I/O 11	I/O 6	I/O 8	V
W	I/O 121	I/O 119	I/O 122	GND																			I/O 13	I/O 15	I/O 9	I/O 10	W
Y	I/O 117	I/O 116	I/O 118	I/O 113																			I/O 17	I/O 19	I/O 12	I/O 14	Y
AA	I/O 115	I/O 112	I/O 114	VCC																			VCC	I/O 22	I/O 16	I/O 18	AA
AB	I/O 111	I/O 108	I/O 110	I/O 109																			I/O 24	I/O 26	I/O 20	I/O 21	AB
AC	I/O 107	NC ¹	I/O 106	GND	I/O 97	VCC	I/O 90	I/O 86	GND	I/O 79	VCC	I/O 75	I/O 68	GND	I/O 64	VCC	I/O 56	I/O 48	GND	I/O 41	VCC	I/O 37	GND	I/O 28	I/O 23	I/O 25	AC
AD	I/O 105	I/O 104	GND	I/O 101	I/O 99	I/O 95	I/O 92	I/O 88	I/O 84	I/O 81	I/O 77	I/O 73	I/O 70	GOE1	I/O 66	I/O 62	I/O 58	I/O 54	I/O 50	I/O 46	I/O 42	I/O 38	I/O 34	GND	I/O 27	I/O 29	AD
AE	I/O 103	GND	I/O 100	I/O 96	I/O 93	I/O 89	I/O 85	I/O 83	I/O 80	I/O 76	I/O 72	I/O 69	I/O 67	I/O 63	I/O 60	I/O 57	I/O 53	I/O 51	I/O 47	I/O 44	I/O 40	I/O 36	I/O 33	I/O 31	GND	GND	AE
AF	GND	GND	I/O 102	I/O 98	I/O 94	I/O 91	I/O 87	NC ¹	I/O 82	I/O 78	I/O 74	I/O 71	GOE0	I/O 65	I/O 61	I/O 59	I/O 55	I/O 52	I/O 49	I/O 45	I/O 43	I/O 39	I/O 35	I/O 32	I/O 30	GND	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispLSI 5384VA
Bottom View

1. NC pins are not to be connected to any active signals, VCC or GND.

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Note: Ball A1 indicator dot on top side of package.