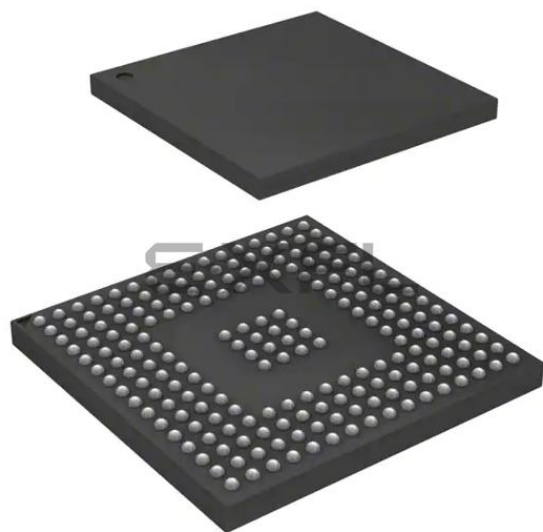




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

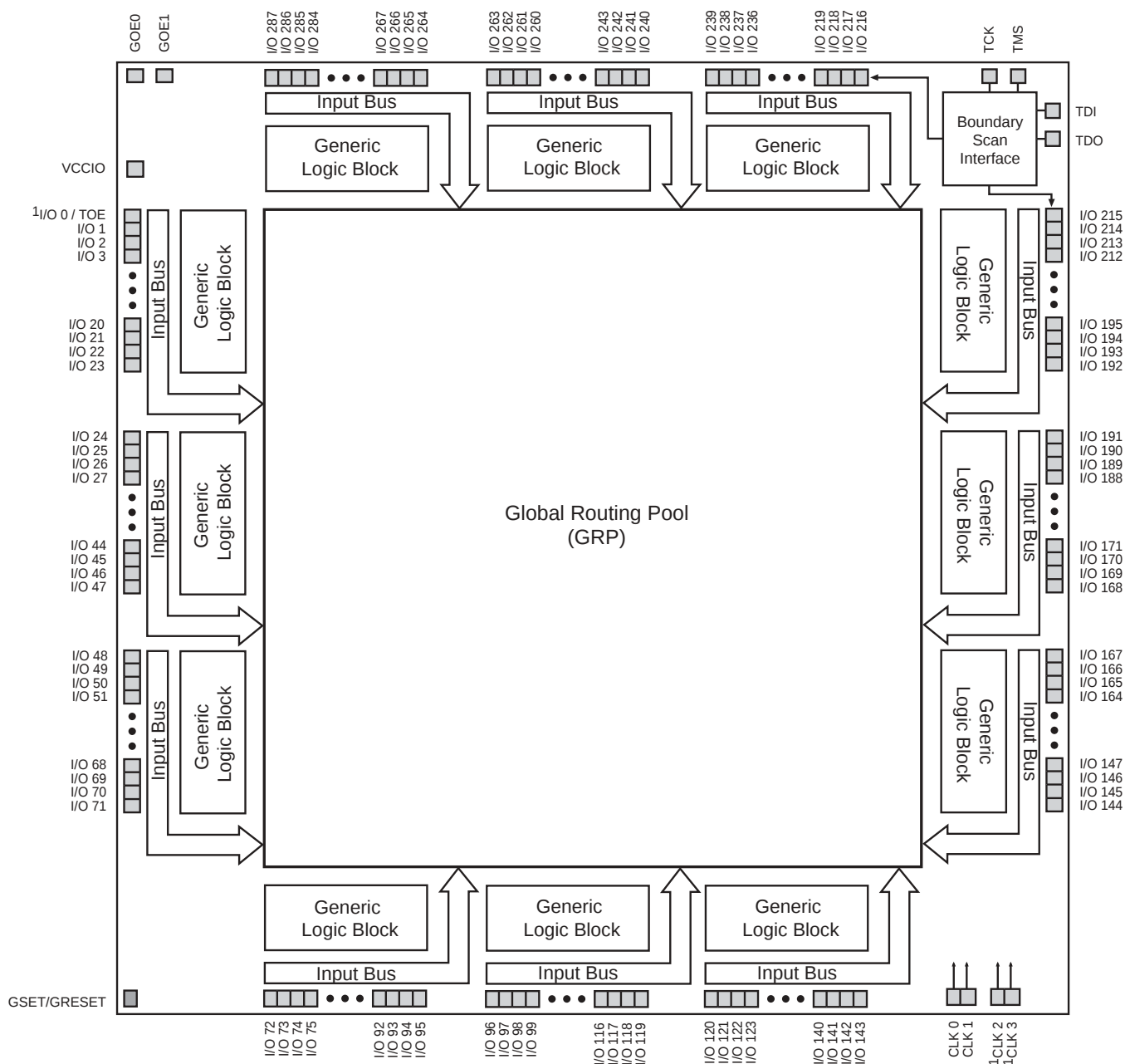
Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	12
Number of Macrocells	384
Number of Gates	18000
Number of I/O	144
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-5384va-125lb208

Functional Block Diagram

Figure 1. ispLSI 5384VA Functional Block Diagram (388 BGA Option)



1. CLK2, CLK3 and TOE signals are multiplexed with I/O signals. Which I/O is multiplexed is determined by the package type used – see table below.

Package Type	Multiplexed Signals		
208 PQFP	I/O 89 / CLK2	I/O 98 / CLK3	I/O 0 / TOE
208 fpBGA	I/O 89 / CLK2	I/O 98 / CLK3	I/O 0 / TOE
272 BGA	I/O 119 / CLK2	I/O 131 / CLK3	I/O 0 / TOE
388 BGA	I/O 179 / CLK2	I/O 197 / CLK3	I/O 0 / TOE

ispLSI 5000V Description (Continued)

five extra product terms are used for shared GLB controls, set, reset, clock, clock enable and output enable.

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, which can be fed back through the Global Routing Pool. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of this feature to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flip flop.

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one line from each macrocell output and one line from each I/O pin.

The input buffer threshold has programmable TTL/3.3V/2.5V compatible levels. The output driver can source 4mA and sink 8mA in 3.3V mode. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows the output drivers to drive either 3.3V or 2.5V output levels while the device logic and the output current drive is always powered from 3.3V. The output drivers also

provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device.

The ispLSI 5000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 5000V Family Members

The ispLSI 5000V Family ranges from 256 macrocells to 512 macrocells and operates from a 3.3V power supply. All family members will be available with multiple package options. The ispLSI 5000VA Family device matrix showing the various bondout options is shown in the table below.

The interconnect structure (GRP) is very similar to Lattice's existing ispLSI 1000, 2000 and 3000 families, but with an enhanced interconnect structure for optimal pin locking and logic routing. This eliminates the need for registered I/O cells or an Output Routing Pool.

Table 1. ispLSI 5000VA Family

Device	GLBs	Macrocells	Package Type			
			208 fpBGA	208 PQFP	272 BGA	388 BGA
ispLSI 5256VA	8	256	144 I/O	144 I/O	192 I/O	—
ispLSI 5384VA	12	384	144 I/O	144 I/O	192 I/O	288 I/O
ispLSI 5512VA	16	512	—	144 I/O	192 I/O	288 I/O

Figure 3. ispLSI 5000V Generic Logic Block (GLB)

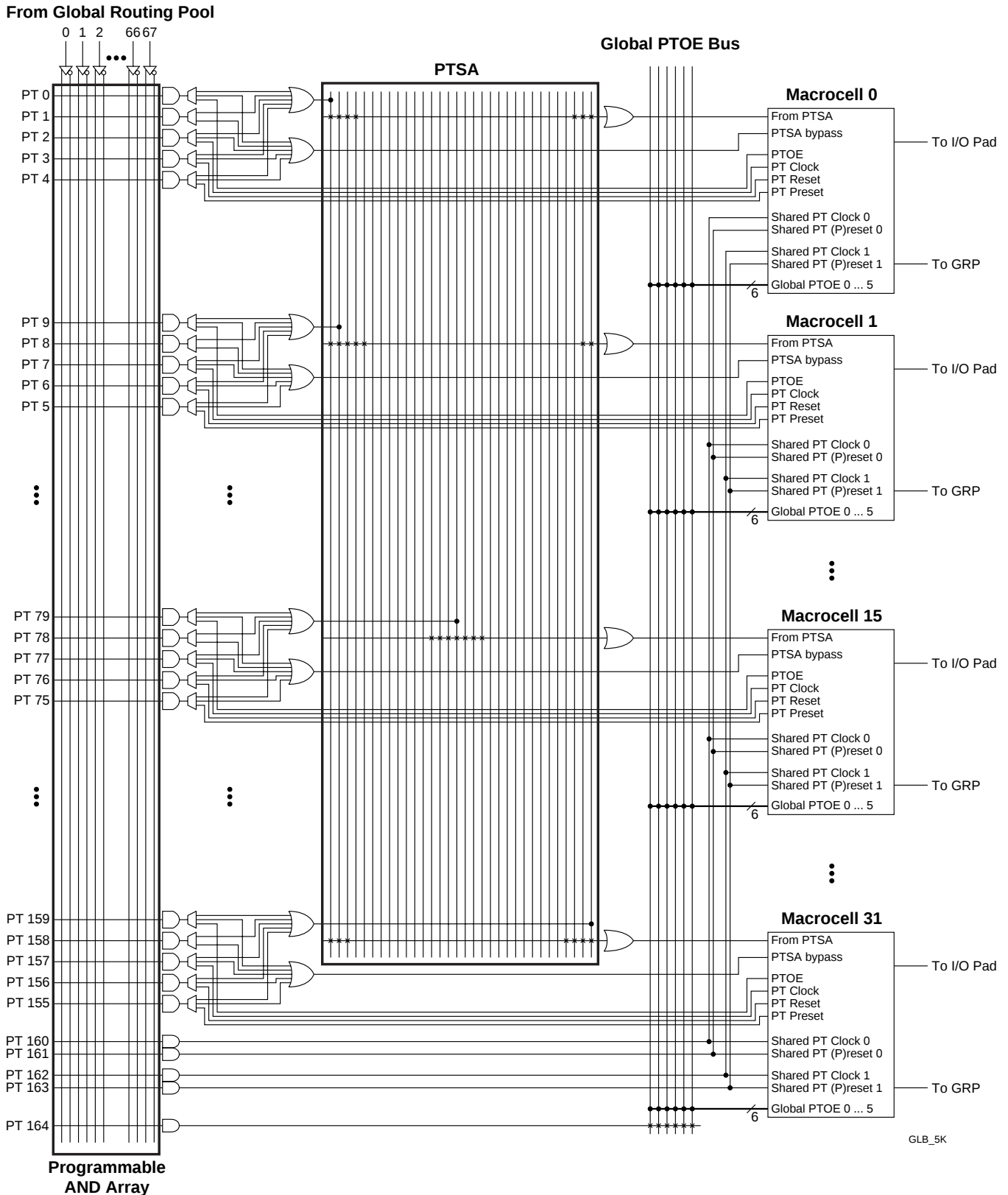
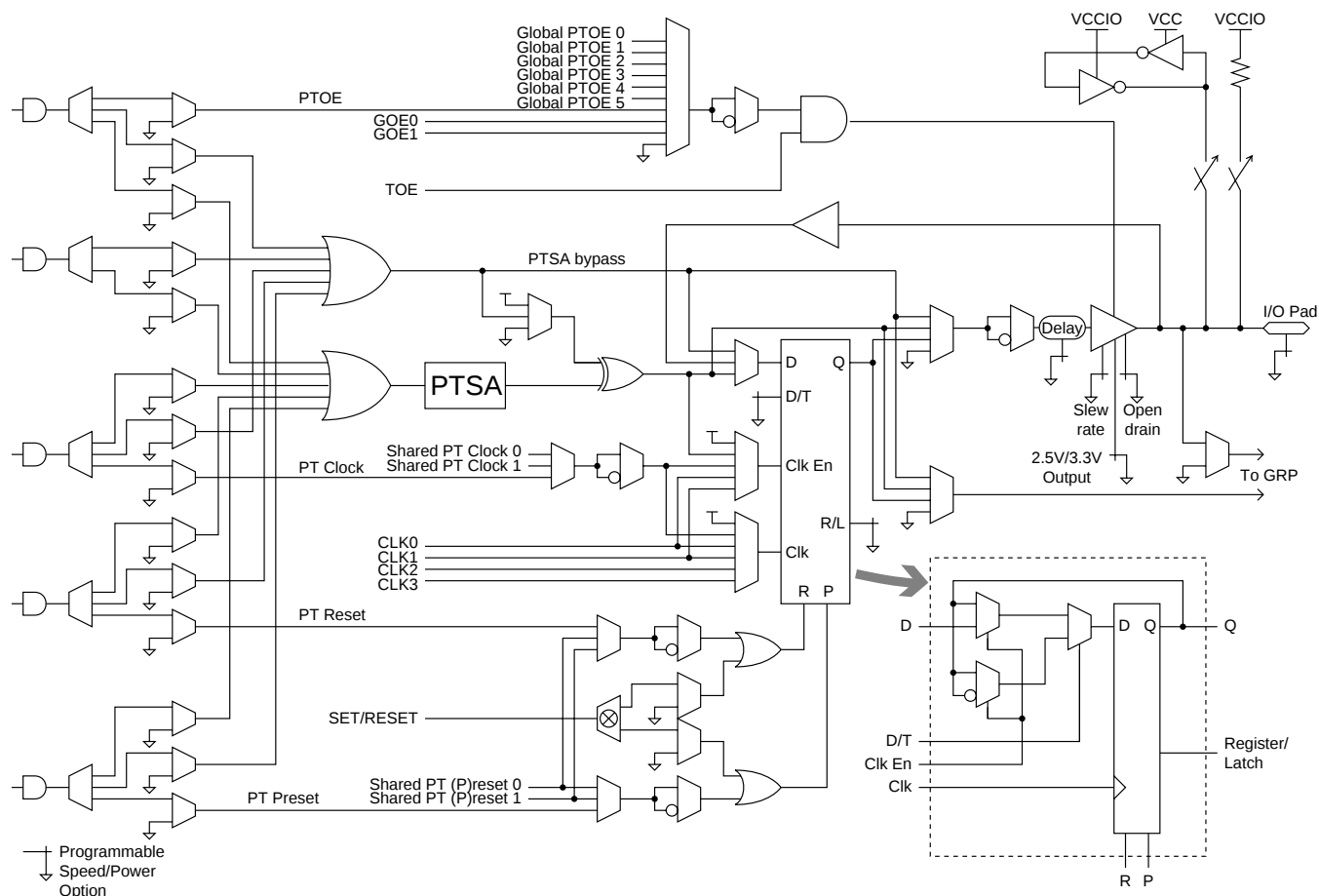


Figure 4. ispLSI 5000V Macrocell

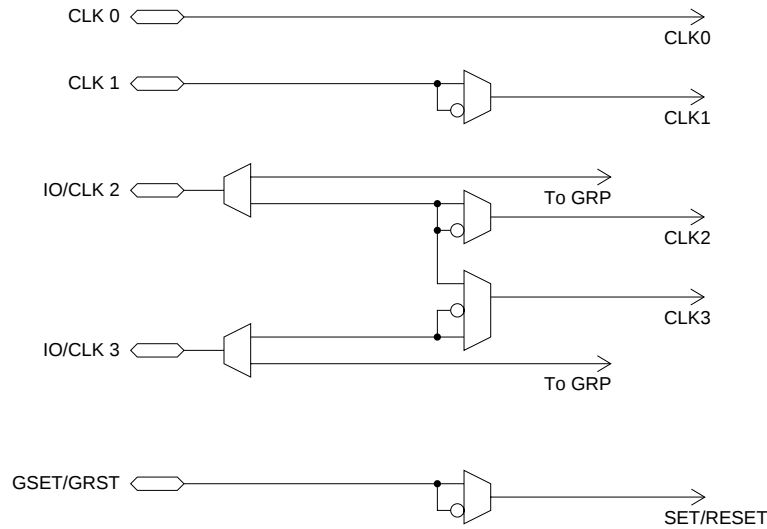


Global Clock Distribution

The ispLSI 5000V Family has four dedicated clock input pins: CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock

speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but also is available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

Figure 5. ispLSI 5000V Global Clock Structure

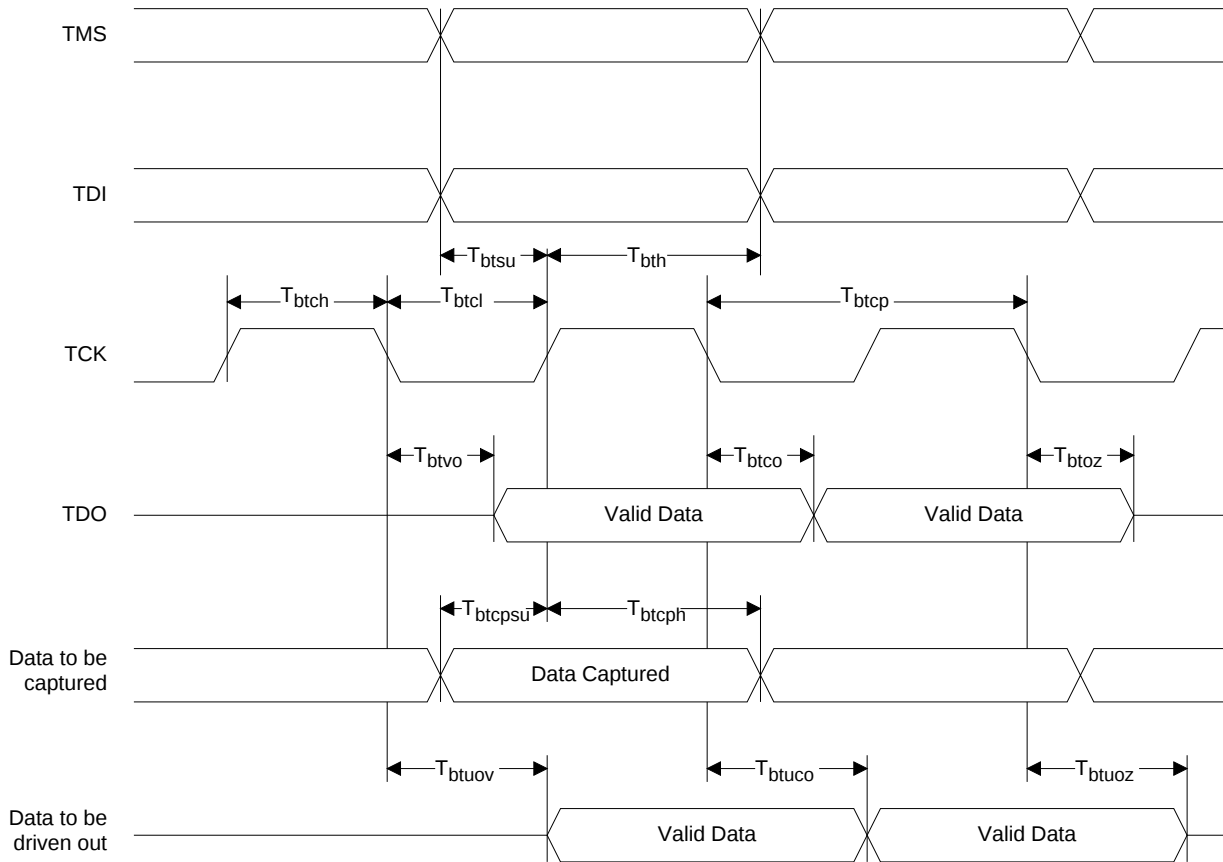


```

graph LR
    IP[Input Pin] --> MUX
    SCANIN[SCANIN  
(from previous cell)] --> MUX
    ShiftDR[Shift DR] --> MUX
    MUX --> D
    ClockDR[Clock DR] --> CK
    subgraph FF [D Flip-Flop]
        D --> Q
        CK --> FF
    end
    Q --> SCANOUT[SCANOUT  
(to next cell)]

```

Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{btcp}	TCK [BSCAN test] clock pulse width	125	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	62.5	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	62.5	–	ns
t_{btsu}	TCK [BSCAN test] setup time	25	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsh}	BSCAN test Capture register setup time	25	–	ns
t_{btcpsh}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoz}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Absolute Maximum Ratings ^{1, 2}

Supply Voltage V_{CC} -0.5 to +5.4V
 Input Voltage Applied -0.5 to +5.6V
 Tri-Stated Output Voltage Applied -0.5 to +5.6V
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Condition

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V _{CC}	Supply Voltage	Commercial T _A = 0°C to +70°C	3.00	3.60	V
		Industrial T _A = -40°C to +85°C	3.00	3.60	V
V _{CCIO}	I/O Reference Voltage		2.3	3.60	V

Table 2 - 0005/5384

Capacitance ($T_A=25^\circ\text{C}, f=1.0\text{ MHz}$)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	$V_{CC} = 3.3\text{V}$, $V_{I/O} = 2.0\text{V}$
C_2	Clock Capacitance	10	pf	$V_{CC} = 3.3\text{V}$, $V_{CK} = 2.0\text{V}$
C_3	Global Input Capacitance	10	pf	$V_{CC} = 3.3\text{V}$, $V_G = 2.0\text{V}$

Table 2 - 0006/5384

Erase Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
ispLSI Erase/Reprogram Cycles	10000	—	Cycles

Table 2-0008/3320

DC Electrical Characteristics for 2.5V Range¹

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V _{CCIO}	I/O Reference Voltage		2.3	–	2.7	V
V _{IL}	Input Low Voltage	$V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	-0.3	–	0.7	V
V _{IH}	Input High Voltage	$V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	1.7	–	5.25	V
V _{OL}	Output Low Voltage	V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OL} = 100μA	–	–	0.2	V
		V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OL} = 2mA	–	–	0.7	V
V _{OH}	Output High Voltage	V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OH} = -100μA	2.1	–	–	V
		V _{CCIO} =min, V _{IN} =V _{IH} or V _{IL} , I _{OH} = -2mA	1.7	–	–	V

1. I/O voltage configuration must be set to V_{CCIO}.

2.5V/5384VA

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
I _{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL(Max)}$	–	–	-10	μA
I _{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2)V \leq V_{IN} \leq V_{CCIO}$	–	–	10	μA
		$V_{CCIO} \leq V_{IN} \leq 5.25V$	–	–	50	μA
I _{PU} ¹	I/O Active Pullup Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
I _{BHL}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL(max)}$	40	–	–	μA
I _{BHH}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH(min)}$	-40	–	–	μA
I _{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	550	μA
I _{BHLH}	Bus Hold High Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	-550	μA
I _{BHT}	Bus Hold Trip Points		V _{IL}	–	V _{IH}	V
I _{VCCIO}	Current Needed for V _{CCIO} Pin	All I/Os Pulled-up, (Total I/Os * I _{PUmax})	–	–	45	mA

1. Pullup is capable of pulling to a minimum voltage of V_{OH} under no-load conditions.

DC Char_5384VA

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST ³ COND.	#	DESCRIPTION ^{4,5}	-125		-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1 ⁶	A	1	Data Prop. Delay, 5PT Bypass	—	7.5	—	10	—	15	ns
tpd2 ⁶	A	2	Data Propagation Delay	—	9.5	—	13	—	19	ns
fmax	A	3	Clock Frequency with Internal Feedback ¹	125	—	100	—	70	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback, 1/(tsu2 + tco1)	91	—	69	—	45	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle ²	167	—	125	—	83	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clk, 5PT bypass	6	—	8	—	12	—	ns
tco1 ⁶	A	7	GLB Reg. Clock to Output Delay	—	4	—	5.5	—	8	ns
th1	—	8	GLB Reg. Hold Time after Clock, 5PT bypass	0	—	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	7	—	9	—	14	—	ns
th2	—	10	GLB Reg. Hold Time after Clock	0	—	0	—	0	—	ns
tsu3 (CLK0/1)	—	11	GLB Reg. Setup Time before Clock, Input Reg. Path (CLK0/1)	4.5	—	6	—	9	—	ns
tsu3 (CLK2/3)	—	12	GLB Reg. Setup Time before Clock, Input Reg. Path (CLK2/3)	3.5	—	5	—	7	—	ns
th3 (CLK0/1)	—	13	GLB Reg. Hold Time after Clock, Input Reg. Path (CLK0/1)	0	—	0	—	0	—	ns
th3 (CLK2/3)	—	14	GLB Reg. Hold Time after Clock, Input Reg. Path (CLK2/3)	0	—	0	—	0	—	ns
tr1	A	15	Ext. Reset Pin to Output Delay	—	15	—	20	—	30	ns
trw1	—	16	Ext. Reset Pulse Duration	7	—	9	—	14	—	ns
tp toe/dis	B/C	17	Local Product Term Output Enable/Disable	—	9	—	12	—	18	ns
tg toe/dis	B/C	18	Global Product Term Output Enable/Disable	—	18	—	24	—	30	ns
tgoe/dis	B/C	19	Global OE Input to Output Enable/Disable	—	6	—	8	—	12	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	3	—	4	—	6	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	3	—	4	—	6	—	ns

1. Standard 32-bit counter using GRP feedback.
2. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
3. Reference Switching Test Conditions section.
4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, and CLK0.
5. Timing parameters measured using normal active output driver.
6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

Timing Ext.5384VA/4.0.eps

Internal Timing Parameters¹

Over Recommended Operating Conditions

PARAM	#	DESCRIPTION	-125		-100		-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I/O Buffer									
tidcom	22	Input Pad and Buffer, Combinatorial Input	–	0.7	–	0.9	–	1.4	ns
tidreg	23	Input Pad and Buffer, Registered Input	–	4.7	–	6.6	–	9.7	ns
todcom	24	Output Pad and Buffer, Combinatorial Output	–	1.3	–	1.7	–	2.6	ns
todreg	25	Output Pad and Buffer, Registered Output	–	1.8	–	2.8	–	4.6	ns
todz	26	Output Buffer Enable/Disable	–	1.3	–	1.7	–	2.6	ns
tslf	27	Slew Rate Adder, Fast Slew	–	0	–	0	–	0	ns
tsls	28	Slew Rate Adder, Slow Slew	–	7.5	–	10	–	15	ns
tslfd	29	Programmable Delay Adder, Fast Slew	–	0.5	–	0.7	–	1	ns
tslsd	30	Programmable Delay Adder, Slow Slew	–	8	–	10.7	–	16	ns
GLB/Macrocell Delay Register									
tmbp	31	Macrocell Register/Latch Bypass	–	0	–	0	–	0	ns
tmlat	32	Macrocell Latch Delay	–	1	–	1.4	–	2	ns
tmco	33	Macrocell Register/Latch Clock to Output	–	1	–	1	–	1	ns
tmsu	34	Macrocell Register/Latch Setup Time	1	–	1.1	–	1.7	–	ns
tmh	35	Macrocell Register/Latch Hold Time	2.5	–	3.9	–	5.3	–	ns
tmsuce	36	Macrocell Register/Latch CLKEN Setup Time	1	–	1.4	–	2	–	ns
tmhce	37	Macrocell Register/Latch CLKEN Hold Time	1	–	1.4	–	2	–	ns
tmrst	38	Macrocell Register/Latch Set/Reset Time	–	1	–	1.4	–	2	ns
ttfog	39	Toggle Flip-Flop Feedback	–	1	–	1.3	–	2	ns
AND Array									
tandhs	40	AND Array, High Speed Mode	–	3	–	4	–	6	ns
tandlp	41	AND Array, Low Power Mode	–	5	–	6.6	–	10	ns
PTSA									
t5ptcom	42	5 Product Term Bypass, Combinatorial	–	1	–	1.4	–	2	ns
t5ptreg	43	5 Product Term Bypass, Registered	–	1	–	1.7	–	2.3	ns
t5ptxcom	44	5 Product Term XOR, Combinatorial	–	2.5	–	3.6	–	5	ns
t5ptxreg	45	5 Product Term XOR, Registered	–	1.5	–	2.2	–	3.3	ns
tptsacom	46	Product Term Sharing Array, Combinatorial	–	3	–	4.1	–	6	ns
tptsareg	47	Product Term Sharing Array, Registered	–	2.0	–	2.7	–	4.3	ns
PTSA Controls									
tpck	48	Product Term Clock Delay	–	0.5	–	0.7	–	1	ns
tpcken	49	Product Term CLKEN Delay	–	1	–	1.4	–	2	ns
tscken	50	Shared Product Term CLKEN Delay	–	1	–	1.4	–	2	ns
tsck	51	Shared Product Term Clock Delay	–	0.5	–	0.7	–	1	ns
tptsacken	52	Product Term Sharing Array CLKEN Delay	–	2.0	–	2.4	–	4	ns
tsrst	53	Shared Product Term Set/Reset Delay	–	2.5	–	3.4	–	5	ns
tprst	54	Product Term Set/Reset Delay	–	1.5	–	2	–	3	ns
tpoe	55	Product Term Output Enable/Disable	–	2.5	–	3.4	–	5	ns
tgpo	56	Global PT Output Enable/Disable	–	11.5	–	15.4	–	17	ns

1. Internal Timing Parameters are not tested and are for reference only.
Refer to Timing Model in this data sheet for further details.

Timing Rev 4.0

Internal Timing Parameters¹

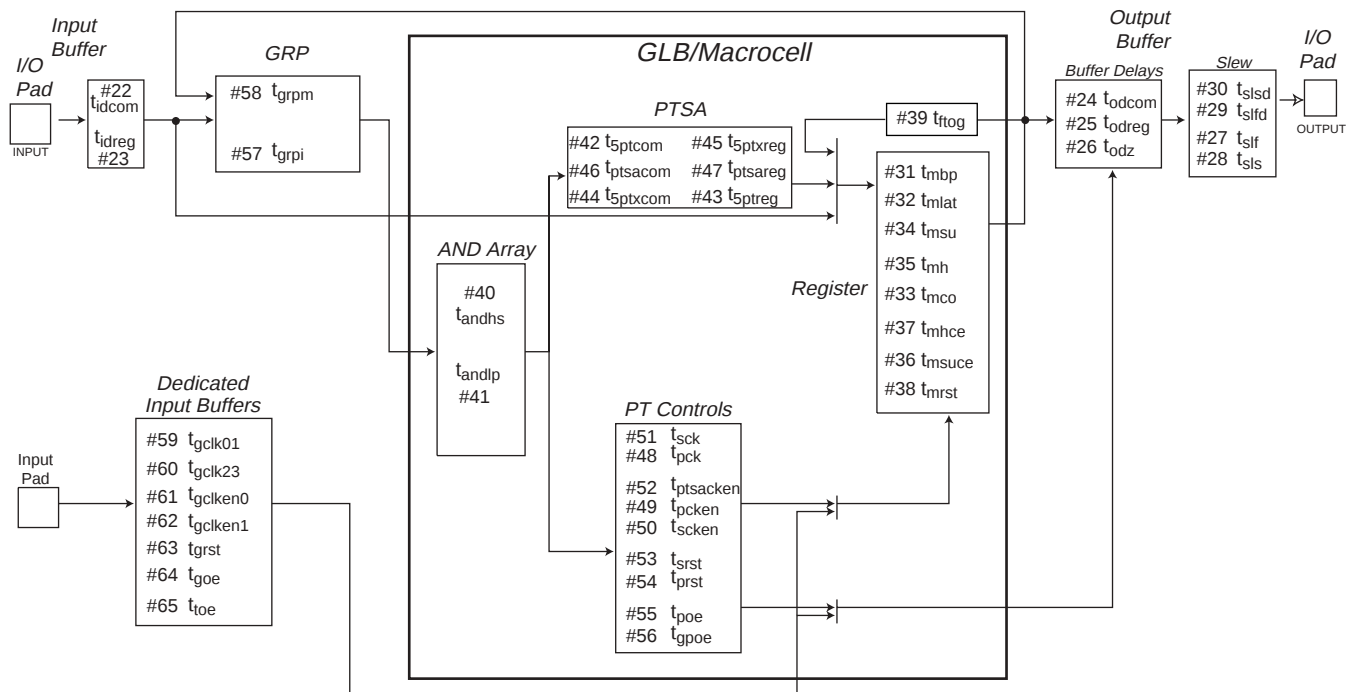
Over Recommended Operating Conditions

PARAM	#	DESCRIPTION	-125		-100		-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
GRP									
tgrpi	57	GRP Delay from I/O Pad	–	1.5	–	2	–	3	ns
tgrpm	58	GRP Delay from Macrocell	–	1.0	–	1.2	–	1.2	ns
Global Control Delays									
tgclk01	59	Global Clock 0 or 1 Delay	–	1.2	–	1.7	–	2.4	ns
tgclk23	60	Global Clock 2 or 3 Delay	–	2.2	–	2.7	–	4.4	ns
tgclken0	61	Global CLKEN 0 Delay	–	1.7	–	2.4	–	3.4	ns
tgclken1	62	Global CLKEN 1 Delay	–	2.7	–	3.4	–	5.4	ns
tgrst	63	Global Set/Reset Delay	–	12.2	–	15.8	–	23.4	ns
tgoe	64	Global OE Delay	–	4.7	–	6.3	–	9.4	ns
ttoe	65	Test OE Delay	–	4.7	–	6.2	–	9.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
Refer to Timing Model in this data sheet for further details.

Timing Rev 4.0

ispLSI 5384VA Timing Model

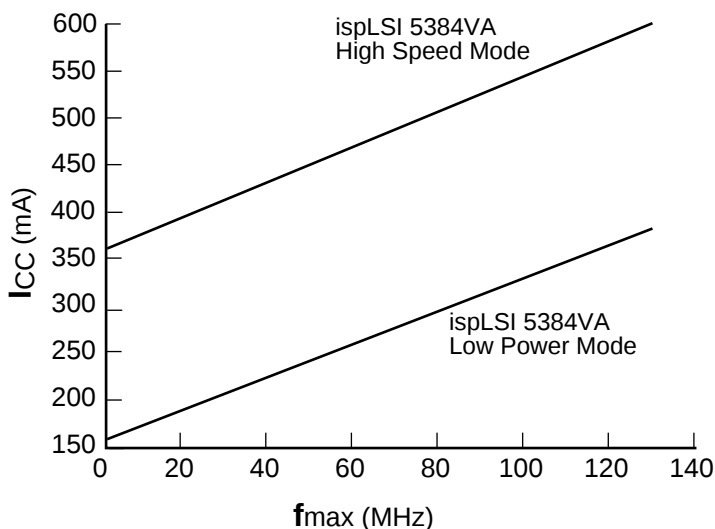


Power Consumption

Power consumption in the ispLSI 5384VA device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts

on the complete group of four. The fast “high-speed” setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower “low-power” setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 24 16-bit Counters
Typical Current at 3.3V, 25° C

ICC can be estimated for the ispLSI 5384VA using the following equation:

High Speed Mode: $ICC = 40 + (\# \text{ of PTs} * 0.432) + (\# \text{ of nets} * \text{Max. freq} * 0.0045)$

Low Power Mode: $ICC = 40 + (\# \text{ of PTs} * 0.161) + (\# \text{ of nets} * \text{Max. freq} * 0.0045)$

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 3.3V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127/5384

Signal Descriptions

Signal Name	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the JTAG state machine.
TCK	Input - This pin is the Test Clock input pin used to clock through the JTAG state machine.
TDI	Input - This pin is the JTAG Test Data In pin used to load data.
TDO	Output - This pin is the JTAG Test Data Out pin used to shift data out.
TOE / I/O0	Input/Output - This pin functions as either the Test Output Enable pin or an I/O pin based upon customer's design. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
GSET/GRST	Dedicated Set/Reset Input - This pin is available to all registers in the device and can independently be configured as preset, reset or no effect on each register. The global polarity (active high or low input) for this pin is also selectable.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
GND	Ground
NC ¹	No connect.
VCC	Vcc
CLK0, CLK1	Dedicated clock inputs for all registers. Both clocks are muxed before being used as the clock input to all registers in the device.
CLK2 / I/O, CLK3 / I/O	Input/Output - These pins function as either dedicated clock inputs for all registers or an I/O pin based upon customer's design. Both clocks are muxed before being used as the clock input to all registers in the device.
VCCIO	Input - This pin is used if an optional 2.5V output is to be used. Every IO can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the Vcc supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.

1. NC pins are not to be connected to any active signals, VCC or GND.

208-Pin PQFP Signal Locations

Signal	Pin
GOE0, GOE1	78, 79
TOE / I/O0	32
GSET/GRST	138
TCK	29
TDI	30
TDO	136
TMS	28
CLK0, CLK1	184,185
CLK2 / I/O89	162
CLK3 / I/O98	173
VCCIO	137
GND	3, 12, 19, 27, 39, 48, 58, 69, 77, 88, 99, 113, 121, 128, 135, 150, 164, 170, 179, 191, 199
VCC	7, 14, 22, 31, 41, 61, 80, 90, 110, 123, 139, 152, 156, 177, 186, 201
NC	49, 50, 51, 52, 101, 102, 103, 104, 105, 106, 107, 108, 109, 157, 158, 207, 208

1. NCs are not to be connected to any active signals, VCC or GND.

208-Pin PQFP I/O Locations

I/O #	Pin	I/O #	Pin	I/O #	Pin	I/O #	Pin	I/O #	Pin	I/O #	Pin
0*	32	24	65	48	96	72	140	96	171	120	203
1	33	25	66	49	97	73	141	97	172	121	204
2	34	26	67	50	98	74	142	98*	173	122	205
3	35	27	68	51	100	75	143	99	174	123	206
4	36	28	70	52	111	76	144	100	175	124	1
5	37	29	71	53	112	77	145	101	176	125	2
6	38	30	72	54	114	78	146	102	178	126	4
7	40	31	73	55	115	79	147	103	180	127	5
8	42	32	74	56	116	80	148	104	181	128	6
9	43	33	75	57	117	81	149	105	182	129	8
10	44	34	76	58	118	82	151	106	183	130	9
11	45	35	81	59	119	83	153	107	187	131	10
12	46	36	82	60	120	84	154	108	188	132	11
13	47	37	83	61	122	85	155	109	189	133	13
14	53	38	84	62	124	86	159	110	190	134	15
15	54	39	85	63	125	87	160	111	192	135	16
16	55	40	86	64	126	88	161	112	193	136	17
17	56	41	87	65	127	89*	162	113	194	137	18
18	57	42	89	66	129	90	163	114	195	138	20
19	59	43	91	67	130	91	165	115	196	139	21
20	60	44	92	68	131	92	166	116	197	140	23
21	62	45	93	69	132	93	167	117	198	141	24
22	63	46	94	70	133	94	168	118	200	142	25
23	64	47	95	71	134	95	169	119	202	143	26

* I/O 89 is multiplexed with CLK2, I/O 98 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

272-Ball BGA Signal Locations

Signal	Ball
GOE0, GOE1	V11, U11
TOE / I/O 0	M2
GSET/GRST	J18
TCK	L4
TDI	M1
TDO	J20
TMS	L3
CLK0, CLK1	C10, D10
CLK2 / I/O 119	A18
CLK3 / I/O 131	B13
VCCIO	J19
GND	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17
VCC	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15
NC ¹	U1, W1, E2, U2, W2, Y2, B3, C3, D3, U3, C5, W4, T4, Y12, A17, T17, W17, B18, C18, B19, C19, D19, W19, B20, T20, W20, Y20, P19, R3

1. NCs are not to be connected to any active signals, VCC or GND.

388-Ball BGA Signal Locations

Signal	Ball
GOE0, GOE1	AF14, AD13
TOE / I/O0	T1
GSET/GRST	L25
TCK	T2
TDI	R3
TDO	N24
TMS	R1
CLK0, CLK1	A13, C14
CLK2 / I/O179	A23
CLK3 / I/O197	B17
VCCIO	M26
GND	A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D19, D23, H4, J23, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N4, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, P23, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V4, W23, AC4, AC8, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26
VCC	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21
NC ¹	C9, D2, E24, L1, AC25, AF19

1. NCs are not to be connected to any active signals, VCC or GND.

388-Ball BGA I/O Locations (Sorted by I/O)

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	T1	48	AC9	96	AE23	144	M24	192	D18	240	B4
1	R4	49	AF8	97	AC22	145	L26	193	A19	241	D5
2	U2	50	AD8	98	AF23	146	M23	194	C19	242	A4
3	T3	51	AE9	99	AD22	147	K25	195	B18	243	C5
4	U1	52	AF9	100	AE24	148	L24	196	A18	244	B3
5	U4	53	AE10	101	AD23	149	K26	197*	B17	245	C4
6	V2	54	AD9	102	AF24	150	K23	198	C18	246	A3
7	U3	55	AF10	103	AE26	151	J25	199	A17	247	B1
8	V1	56	AC10	104	AD25	152	K24	200	D17	248	C2
9	W2	57	AE11	105	AD26	153	J26	201	B16	249	C1
10	W1	58	AD10	106	AC24	154	H25	202	C17	250	D3
11	V3	59	AF11	107	AC26	155	H26	203	A16	251	D1
12	Y2	60	AE12	108	AB25	156	J24	204	B15	252	E2
13	W4	61	AF12	109	AB23	157	G25	205	A15	253	E4
14	Y1	62	AD11	110	AB24	158	H23	206	C16	254	E3
15	W3	63	AE13	111	AB26	159	G26	207	B14	255	E1
16	AA2	64	AC12	112	AA25	160	H24	208	D15	256	F2
17	Y4	65	AF13	113	Y23	161	F25	209	A14	257	G4
18	AA1	66	AD12	114	AA24	162	G23	210	C15	258	F3
19	Y3	67	AE14	115	AA26	163	F26	211	B13	259	F1
20	AB2	68	AC14	116	Y25	164	G24	212	D13	260	G2
21	AB1	69	AE15	117	Y26	165	E25	213	B12	261	G1
22	AA3	70	AD14	118	Y24	166	E26	214	C13	262	G3
23	AC2	71	AF15	119	W25	167	F24	215	A12	263	H2
24	AB4	72	AE16	120	V23	168	D25	216	B11	264	J4
25	AC1	73	AD15	121	W26	169	E23	217	C12	265	H1
26	AB3	74	AF16	122	W24	170	D26	218	A11	266	H3
27	AD2	75	AC15	123	V25	171	C25	219	D12	267	J2
28	AC3	76	AE17	124	V26	172	D24	220	B10	268	J1
29	AD1	77	AD16	125	U25	173	C26	221	C11	269	K2
30	AF2	78	AF17	126	V24	174	A25	222	A10	270	J3
31	AE3	79	AC17	127	U26	175	B24	223	D10	271	K1
32	AF3	80	AE18	128	U23	176	A24	224	B9	272	K4
33	AE4	81	AD17	129	T25	177	B23	225	C10	273	L2
34	AD4	82	AF18	130	U24	178	C23	226	A9	274	K3
35	AF4	83	AE19	131	T26	179*	A23	227	B8	275	M2
36	AE5	84	AD18	132	R25	180	B22	228	A8	276	M1
37	AC5	85	AE20	133	R26	181	D22	229	B7	277	L3
38	AD5	86	AC19	134	T24	182	C22	230	D8	278	N2
39	AF5	87	AF20	135	P25	183	A22	231	A7	279	M4
40	AE6	88	AD19	136	R23	184	B21	232	C8	280	N1
41	AC7	89	AE21	137	P26	185	D20	233	B6	281	M3
42	AD6	90	AC20	138	R24	186	C21	234	D7	282	P2
43	AF6	91	AF21	139	N25	187	A21	235	A6	283	P4
44	AE7	92	AD20	140	N23	188	B20	236	C7	284	P1
45	AF7	93	AE22	141	N26	189	A20	237	B5	285	N3
46	AD7	94	AF22	142	P24	190	C20	238	A5	286	R2
47	AE8	95	AD21	143	M25	191	B19	239	C6	287	P3

* I/O 179 is multiplexed with CLK2, I/O 197 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

Signal Configuration

ispLSI 5384VA 208-ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O 84	I/O 87	I/O 91	I/O 94	I/O 95	CLK3/ I/O98	I/O 100	I/O 104	I/O 105	CLK 0	I/O 109	I/O 110	I/O 113	I/O 114	I/O 115	I/O 124	A
B	I/O 81	I/O 86	I/O 88	CLK2/ I/O89	I/O 93	I/O 97	I/O 99	I/O 102	CLK 1	I/O 108	I/O 112	I/O 117	I/O 118	I/O 122	I/O 123	I/O 126	B
C	I/O 80	I/O 85	NC ¹	I/O 90	I/O 92	I/O 96	I/O 101	I/O 103	I/O 106	I/O 107	I/O 111	I/O 116	I/O 119	I/O 120	I/O 121	I/O 129	C
D	I/O 79	I/O 82	I/O 83	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O 127	I/O 125	I/O 131	D
E	I/O 78	NC ¹	I/O 76	VCC	ispLSI 5384VA Bottom View								GND	I/O 130	I/O 128	I/O 133	E
F	I/O 75	I/O 77	I/O 73	GND									VCC	I/O 136	I/O 132	I/O 134	F
G	I/O 72	I/O 74	TDO	VCC									GND	I/O 139	I/O 135	I/O 140	G
H	I/O 71	VCCIO	GSET/ GRST	GND									VCC	I/O 138	I/O 137	I/O 141	H
J	I/O 70	I/O 69	I/O 68	GND	ispLSI 5384VA Bottom View								GND	I/O 143	I/O 142	TMS	J
K	I/O 67	I/O 66	I/O 65	VCC									VCC	TDI	TCK	TOE/ I/O0	K
L	I/O 64	I/O 63	I/O 62	GND									GND	I/O 3	I/O 1	I/O 2	L
M	I/O 61	I/O 60	I/O 58	GND									VCC	I/O 6	I/O 5	I/O 4	M
N	I/O 59	I/O 56	I/O 57	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	I/O 8	I/O 9	I/O 7	N
P	I/O 55	I/O 53	I/O 49	I/O 50	I/O 43	I/O 42	GOE1	GOE0	I/O 31	I/O 32	I/O 27	I/O 20	I/O 17	I/O 15	I/O 10	I/O 11	P
R	I/O 54	I/O 52	I/O 47	I/O 51	I/O 48	I/O 44	I/O 36	I/O 35	I/O 30	I/O 26	I/O 22	I/O 19	I/O 18	I/O 14	I/O 13	I/O 12	R
T	I/O 46	I/O 45	I/O 41	I/O 40	I/O 39	I/O 38	I/O 37	I/O 34	I/O 33	I/O 29	I/O 28	I/O 25	I/O 24	I/O 23	I/O 21	I/O 16	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

208 fpBGA/5384VA

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Pin Configuration

ispLSI 5384VA 388-ball BGA

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O 174	I/O 176	I/O 179/ CLK2	I/O 183	I/O 187	I/O 189	I/O 193	I/O 196	I/O 199	I/O 203	I/O 205	I/O 209	CLK0	I/O 215	I/O 218	I/O 222	I/O 226	I/O 228	I/O 231	I/O 235	I/O 238	I/O 242	I/O 246	GND	GND	A
B	GND	GND	I/O 175	I/O 177	I/O 180	I/O 184	I/O 188	I/O 191	I/O 195	I/O 197/ CLK3	I/O 201	I/O 204	I/O 207	I/O 211	I/O 213	I/O 216	I/O 220	I/O 224	I/O 227	I/O 229	I/O 233	I/O 237	I/O 240	I/O 244	GND	I/O 247	B
C	I/O 173	I/O 171	GND	I/O 178	I/O 182	I/O 186	I/O 190	I/O 194	I/O 198	I/O 202	I/O 206	I/O 210	CLK1	I/O 214	I/O 217	I/O 221	I/O 225	NC ¹	I/O 232	I/O 236	I/O 239	I/O 243	I/O 245	GND	I/O 248	I/O 249	C
D	I/O 170	I/O 168	I/O 172	GND	I/O 181	VCC	I/O 185	GND	I/O 192	I/O 200	VCC	I/O 208	GND	I/O 212	I/O 219	VCC	I/O 223	GND	I/O 230	I/O 234	VCC	I/O 241	GND	I/O 250	NC ¹	I/O 251	D
E	I/O 166	I/O 165	NC ¹	I/O 169																			I/O 253	I/O 254	I/O 252	I/O 255	E
F	I/O 163	I/O 161	I/O 167	VCC																			VCC	I/O 258	I/O 256	I/O 259	F
G	I/O 159	I/O 157	I/O 164	I/O 162																			I/O 257	I/O 262	I/O 260	I/O 261	G
H	I/O 155	I/O 154	I/O 160	I/O 158																			GND	I/O 266	I/O 263	I/O 265	H
J	I/O 153	I/O 151	I/O 156	GND																			I/O 264	I/O 270	I/O 267	I/O 268	J
K	I/O 149	I/O 147	I/O 152	I/O 150																			I/O 272	I/O 274	I/O 269	I/O 271	K
L	I/O 145	SET/ RST	I/O 148	VCC																			VCC	I/O 277	I/O 273	NC ¹	L
M	VCCIO	I/O 143	I/O 144	I/O 146																			I/O 279	I/O 281	I/O 275	I/O 276	M
N	I/O 141	I/O 139	TDO	I/O 140																			GND	I/O 285	I/O 278	I/O 280	N
P	I/O 137	I/O 135	I/O 142	GND																			I/O 283	I/O 287	I/O 282	I/O 284	P
R	I/O 133	I/O 132	I/O 138	I/O 136																			I/O 1	TDI	I/O 286	TMS	R
T	I/O 131	I/O 129	I/O 134	VCC																			VCC	I/O 3	TCK	I/O 0/ TOE	T
U	I/O 127	I/O 125	I/O 130	I/O 128																			I/O 5	I/O 7	I/O 2	I/O 4	U
V	I/O 124	I/O 123	I/O 126	I/O 120																			GND	I/O 11	I/O 6	I/O 8	V
W	I/O 121	I/O 119	I/O 122	GND																			I/O 13	I/O 15	I/O 9	I/O 10	W
Y	I/O 117	I/O 116	I/O 118	I/O 113																			I/O 17	I/O 19	I/O 12	I/O 14	Y
AA	I/O 115	I/O 112	I/O 114	VCC																			VCC	I/O 22	I/O 16	I/O 18	AA
AB	I/O 111	I/O 108	I/O 110	I/O 109																			I/O 24	I/O 26	I/O 20	I/O 21	AB
AC	I/O 107	NC ¹	I/O 106	GND	I/O 97	VCC	I/O 90	I/O 86	GND	I/O 79	VCC	I/O 75	I/O 68	GND	I/O 64	VCC	I/O 56	I/O 48	GND	I/O 41	VCC	I/O 37	GND	I/O 28	I/O 23	I/O 25	AC
AD	I/O 105	I/O 104	GND	I/O 101	I/O 99	I/O 95	I/O 92	I/O 88	I/O 84	I/O 81	I/O 77	I/O 73	I/O 70	GOE1	I/O 66	I/O 62	I/O 58	I/O 54	I/O 50	I/O 46	I/O 42	I/O 38	I/O 34	GND	I/O 27	I/O 29	AD
AE	I/O 103	GND	I/O 100	I/O 96	I/O 93	I/O 89	I/O 85	I/O 83	I/O 80	I/O 76	I/O 72	I/O 69	I/O 67	I/O 63	I/O 60	I/O 57	I/O 53	I/O 51	I/O 47	I/O 44	I/O 40	I/O 36	I/O 33	I/O 31	GND	GND	AE
AF	GND	GND	I/O 102	I/O 98	I/O 94	I/O 91	I/O 87	NC ¹	I/O 82	I/O 78	I/O 74	I/O 71	GOE0	I/O 65	I/O 61	I/O 59	I/O 55	I/O 52	I/O 49	I/O 45	I/O 43	I/O 39	I/O 35	I/O 32	I/O 30	GND	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispLSI 5384VA
Bottom View

1. NC pins are not to be connected to any active signals, VCC or GND.

388 BGA/5384VA

Note: Ball A1 indicator dot on top side of package.