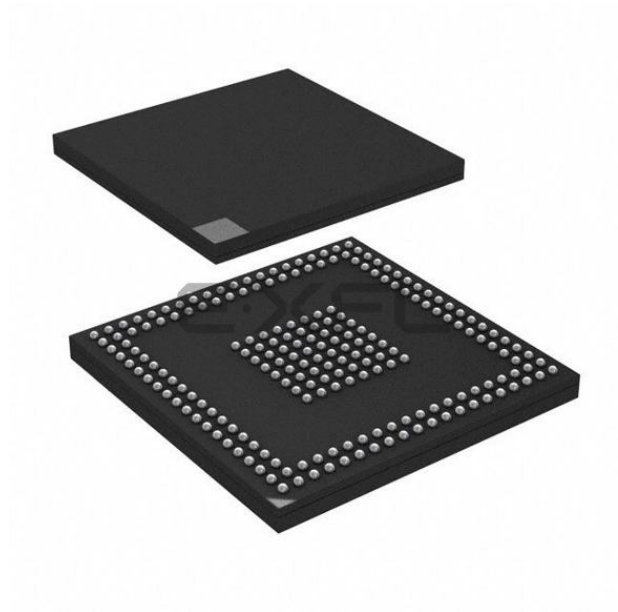

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	DMA, I²C, PPI, SPI, SPORT, UART, USB
Clock Rate	400MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf525wbbcz402

GENERAL DESCRIPTION

The ADSP-BF52x processors are members of the Blackfin family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin® processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF52x processors are completely code compatible with other Blackfin processors. The ADSP-BF523/ADSP-BF525/ADSP-BF527 processors offer performance up to 600 MHz. The ADSP-BF522/ADSP-BF524/ADSP-BF526 processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

Table 1. Processor Comparison

Feature		ADSP-BF522	ADSP-BF524	ADSP-BF526	ADSP-BF523	ADSP-BF525	ADSP-BF527
Host DMA		1	1	1	1	1	1
USB		–	1	1	–	1	1
Ethernet MAC		–	–	1	–	–	1
Internal Voltage Regulator		–	–	–	1	1	1
TWI		1	1	1	1	1	1
SPORTs		2	2	2	2	2	2
UARTs		2	2	2	2	2	2
SPI		1	1	1	1	1	1
GP Timers		8	8	8	8	8	8
GP Counter		1	1	1	1	1	1
Watchdog Timers		1	1	1	1	1	1
RTC		1	1	1	1	1	1
Parallel Peripheral Interface		1	1	1	1	1	1
GPIOs		48	48	48	48	48	48
Memory (bytes)	L1 Instruction SRAM	48K	48K	48K	48K	48K	48K
	L1 Instruction SRAM/Cache	16K	16K	16K	16K	16K	16K
	L1 Data SRAM	32K	32K	32K	32K	32K	32K
	L1 Data SRAM/Cache	32K	32K	32K	32K	32K	32K
	L1 Scratchpad	4K	4K	4K	4K	4K	4K
	L3 Boot ROM	32K	32K	32K	32K	32K	32K
Maximum Instruction Rate[1]		400 MHz			600 MHz		
Maximum System Clock Speed		100 MHz			133 MHz		
Package Options		289-Ball CSP_BGA					
		208-Ball CSP_BGA					

[1] Maximum instruction rate is not available with every possible SCLK selection.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF52x processors are highly integrated system-on-a-chip solutions for the next generation of embedded network connected applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include an IEEE-compliant 802.3 10/100 Ethernet MAC, a USB 2.0 high speed OTG controller, a TWI controller, a NAND flash controller, two UART ports, an SPI port, two serial ports (SPORTs), eight general purpose 32-bit timers with PWM capability, a core timer, a real-time clock, a watchdog timer, a Host DMA (HOSTDP) interface, and a parallel peripheral interface (PPI).

PROCESSOR PERIPHERALS

The ADSP-BF52x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1).

These Blackfin processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, TWI, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF523/ADSP-BF525/ADSP-BF527 processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage

length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The Blackfin processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency on-chip memory as cache or SRAM, and larger, lower-cost and performance off-chip memory systems. See Figure 3.

The on-chip L1 memory system is the highest-performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high-bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

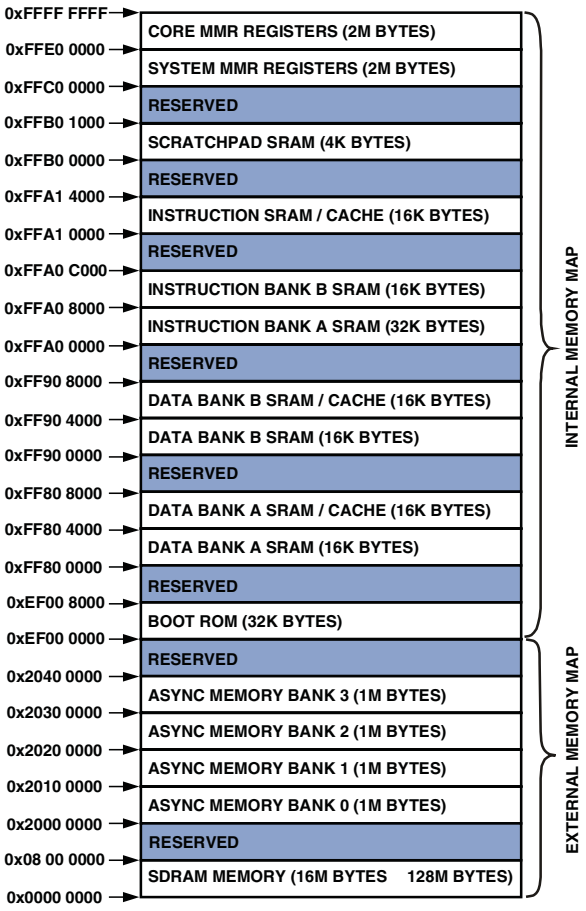


Figure 3. Internal/External Memory Map

Internal (On-Chip) Memory

The processor has three blocks of on-chip memory providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 64K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM), as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. A separate row can be open for each SDRAM internal bank and the SDRAM controller supports up to 4 internal SDRAM banks, improving overall performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing requirements for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

NAND Flash Controller (NFC)

The ADSP-BF52x processors provide a NAND flash controller (NFC). NAND flash devices provide high-density, low-cost memory. However, NAND flash devices also have long random access times, invalid blocks, and lower reliability over device lifetimes. Because of this, NAND flash is often used for read-only code storage. In this case, all DSP code can be stored in NAND flash and then transferred to a faster memory (such as SDRAM or SRAM) before execution. Another common use of NAND flash is for storage of multimedia files or other large data segments. In this case, a software file system may be used to manage reading and writing of the NAND flash device. The file system selects memory segments for storage with the goal of avoiding bad blocks and equally distributing memory accesses across all address locations. Hardware features of the NFC include:

- Support for page program, page read, and block erase of NAND flash devices, with accesses aligned to page boundaries.
- Error checking and correction (ECC) hardware that facilitates error detection and correction.
- A single 8-bit external bus interface for commands, addresses, and data.
- Support for SLC (single level cell) NAND flash devices unlimited in size, with page sizes of 256 and 512 bytes. Larger page sizes can be supported in software.
- Capability of releasing external bus interface pins during long accesses.
- Support for internal bus requests of 16 bits.
- DMA engine to transfer data between internal memory and NAND flash device.

One-Time Programmable Memory

The processor has 64K bits of one-time programmable non-volatile memory that can be programmed by the developer only one time. It includes the array and logic to support read access and programming. Additionally, its pages can be write protected.

OTP enables developers to store both public and private data on-chip. In addition to storing public and private key data for applications requiring security, it also allows developers to store completely user-definable data such as customer ID, product ID, MAC address, etc. Hence, generic parts can be shipped, which are then programmed and protected by the developer within this non-volatile memory.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The processor contains a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the processor is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 18.

Event Handling

The event controller on the processor handles all asynchronous and synchronous events to the processor. The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The controller provides support for five different types of events:

- Emulation — An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- $\overline{\text{RESET}}$ — This event resets the processor.
- Nonmaskable Interrupt (NMI) — The NMI event can be generated by the software watchdog timer or by the $\overline{\text{NMI}}$ input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions — Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts — Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The processor event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt

controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	$\overline{\text{RESET}}$	RST
2	Nonmaskable Interrupt	$\overline{\text{NMI}}$
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	General Purpose Interrupt (at $\overline{\text{RESET}}$)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Registers	
PLL Wakeup Interrupt	IVG7	0	0	IAR0	IMASK0, ISR0, IWR0
DMA Error 0 (generic)	IVG7	1	0	IAR0	IMASK0, ISR0, IWR0
DMAR0 Block Interrupt	IVG7	2	0	IAR0	IMASK0, ISR0, IWR0
DMAR1 Block Interrupt	IVG7	3	0	IAR0	IMASK0, ISR0, IWR0
DMAR0 Overflow Error	IVG7	4	0	IAR0	IMASK0, ISR0, IWR0
DMAR1 Overflow Error	IVG7	5	0	IAR0	IMASK0, ISR0, IWR0
PPI Error	IVG7	6	0	IAR0	IMASK0, ISR0, IWR0
MAC Status	IVG7	7	0	IAR0	IMASK0, ISR0, IWR0
SPORT0 Status	IVG7	8	0	IAR1	IMASK0, ISR0, IWR0
SPORT1 Status	IVG7	9	0	IAR1	IMASK0, ISR0, IWR0
Reserved	IVG7	10	0	IAR1	IMASK0, ISR0, IWR0
Reserved	IVG7	11	0	IAR1	IMASK0, ISR0, IWR0
UART0 Status	IVG7	12	0	IAR1	IMASK0, ISR0, IWR0
UART1 Status	IVG7	13	0	IAR1	IMASK0, ISR0, IWR0
RTC	IVG8	14	1	IAR1	IMASK0, ISR0, IWR0
DMA Channel 0 (PPI/NFC)	IVG8	15	1	IAR1	IMASK0, ISR0, IWR0
DMA Channel 3 (SPORT0 RX)	IVG9	16	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 4 (SPORT0 TX)	IVG9	17	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 5 (SPORT1 RX)	IVG9	18	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 6 (SPORT1 TX)	IVG9	19	2	IAR2	IMASK0, ISR0, IWR0
TWI	IVG10	20	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 7 (SPI)	IVG10	21	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 8 (UART0 RX)	IVG10	22	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 9 (UART0 TX)	IVG10	23	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 10 (UART1 RX)	IVG10	24	3	IAR3	IMASK0, ISR0, IWR0
DMA Channel 11 (UART1 TX)	IVG10	25	3	IAR3	IMASK0, ISR0, IWR0

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF52x processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF52x Blackfin Processor Hardware Reference* (volumes 1 and 2)
- *Blackfin Processor Programming Reference*
- *ADSP-BF522/ADSP-BF524/ADSP-BF526 Blackfin Processor Anomaly List*
- *ADSP-BF523/ADSP-BF525/ADSP-BF527 Blackfin Processor Anomaly List*

SIGNAL DESCRIPTIONS

Signal definitions for the ADSP-BF52x processors are listed in Table 10. In order to maintain maximum function and reduce package size and ball count, some balls have dual, multiplexed functions. In cases where ball function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 10.

All I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs, as noted in Table 10.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements. If no IBIS simulation is performed, it is strongly recommended to add series resistor terminations for all Driver Types A, C and D.

The termination resistors should be placed near the processor to reduce transients and improve signal integrity. The resistance value, typically 33 Ω or 47 Ω, should be chosen to match the average board trace impedance.

Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 10. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
EBIU			
ADDR19–1	O	Address Bus	A
DATA15–0	I/O	Data Bus	A
$\overline{\text{ABE1–0}}$/*SDQM1–0*	O	Byte Enables/*Data Mask*	A
$\overline{\text{AMS3–0}}$	O	Asynchronous Memory Bank Selects (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control	
$\overline{\text{AOE}}$	O	Asynchronous Output Enable	A
$\overline{\text{ARE}}$	O	Asynchronous Read Enable	A
$\overline{\text{AWE}}$	O	Asynchronous Write Enable	A
$\overline{\text{SRAS}}$	O	SDRAM Row Address Strobe	A
$\overline{\text{SCAS}}$	O	SDRAM Column Address Strobe	A
$\overline{\text{SWE}}$	O	SDRAM Write Enable	A
SCKE	O	SDRAM Clock Enable (Requires a pull-down if hibernate with SDRAM self-refresh is used.)	A
CLKOUT	O	SDRAM Clock Output	B
SA10	O	SDRAM A10 Signal	A
$\overline{\text{SMS}}$	O	SDRAM Bank Select	A

Table 20. Electrical Characteristics for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDDEEPSLEEP}$[1]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		10		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.0 V, f_{SCLK} = 25 MHz, T_J = 25°C		20		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.0 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 0.44		53		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.0 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		94		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.15 V, f_{CCLK} = 533 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		144		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 600 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		170		mA
$I_{DDHIBERNATE}$[1, 2]	Hibernate State Current	V_{DDEXT}=V_{DDMEM}=V_{DDRTC}= V_{DDUSB} = 3.30 V, V_{DDOTP}=V_{PPOTP}=2.5 V, T_J = 25°C, CLKIN = 0 MHz with voltage regulator off (V_{DDINT} = 0 V)		40		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20		µA
$I_{DDUSB-FS}$	V_{DDUSB} Current in Full/Low Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, Full Speed USB Transmit		9		mA
$I_{DDUSB-HS}$	V_{DDUSB} Current in High Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, High Speed USB Transmit		25		mA
$I_{DDSLEEP}$[1, 3]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			Table 24 + (0.61 × V_{DDINT} × f_{SCLK})[4]	mA[4]
$I_{DDDEEPSLEEP}$[1, 3]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 24	mA
I_{DDINT}[3, 5]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 24 + (Table 25 × ASF) + (0.61 × V_{DDINT} × f_{SCLK})	mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		1		mA
I_{DDOTP}	V_{DDOTP} Current	V_{DDOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		25		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Read		0		mA
I_{PPOTP}	V_{PPOTP} Current	V_{PPOTP} = 2.5 V, T_J = 25°C, OTP Memory Write		0		mA

[1] See the *ADSP-BF52x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[2] Includes current on V_{DDEXT}, V_{DDUSB}, V_{DDMEM}, V_{DDOTP}, and V_{PPOTP} supplies. Clock inputs are tied high or low.
[3] Guaranteed maximum specifications.
[4] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz. Example: 1.2 V, 75 MHz would be 0.61 × 1.2 × 75 = 54.9 mA adder.
[5] See Table 21 for the list of I_{DDINT} power vectors covered.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 32 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 22 or Table 24), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 23 or Table 25).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 21).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 23 or Table 25 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 21. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.26
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.44

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF52x processors.

Table 22. Static Current — $I_{DD-DEEPSLEEP}$ (mA) for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

	Voltage (V_{DDINT})[1]						
T_J (°C)[1]	1.2 V	1.25 V	1.3 V	1.35 V	1.4 V	1.45 V	1.5 V
–40	1.47	1.42	1.50	1.64	1.85	2.12	2.09
–20	1.67	1.81	1.89	1.95	2.01	2.07	2.12
0	1.97	2.07	2.15	2.22	2.30	2.39	2.47
25	2.49	2.66	2.79	2.92	3.07	3.20	3.36
40	3.12	3.37	3.57	3.75	3.96	4.18	4.40
55	4.07	4.47	4.82	5.11	5.41	5.73	6.06
70	5.77	6.28	6.71	7.17	7.61	8.09	8.60
85	8.32	8.88	9.56	10.25	10.94	11.63	12.36
100	12.11	12.93	13.94	14.76	15.76	16.77	17.83
105	13.78	14.72	15.74	16.81	17.91	19.06	20.27

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors on Page 28.

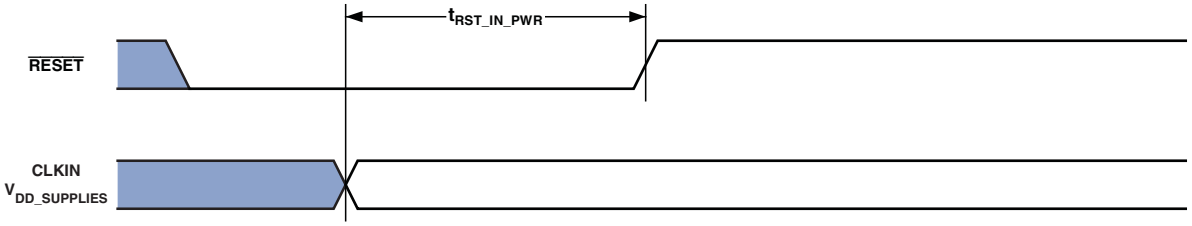
Table 23. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1] for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

f_{CCLK} (MHz)[2]	Voltage (V_{DDINT})[2]						
	1.2 V	1.25 V	1.3 V	1.35 V	1.4 V	1.45 V	1.5 V
400	N/A	N/A	91.41	95.7	100.11	104.51	109.01
350	N/A	N/A	80.56	84.37	88.26	92.17	96.17
300	63.31	66.51	69.78	73.09	76.51	79.93	83.42
250	53.36	56.10	58.88	61.72	64.64	67.56	70.55
200	43.49	45.76	48.08	50.44	52.86	55.28	57.77
100	23.6	24.93	26.29	27.68	29.12	30.56	32.04

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 32.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors on Page 28.

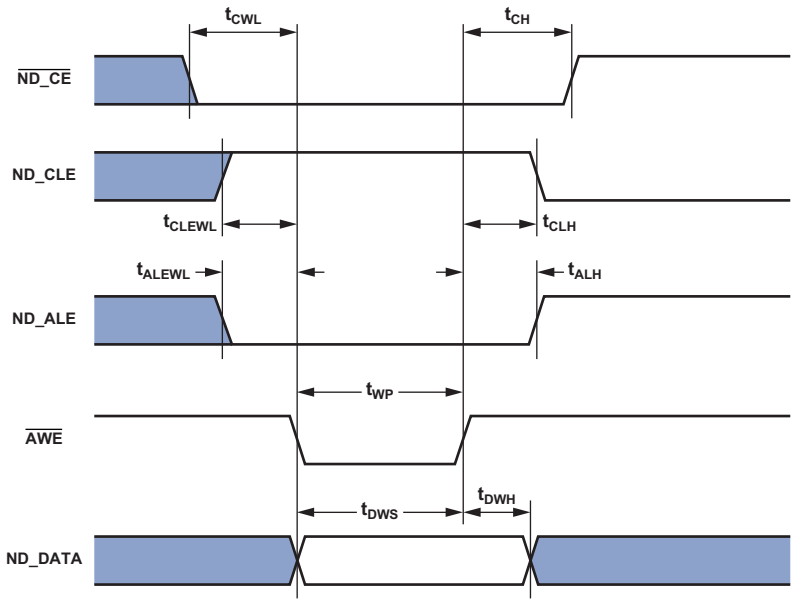
Table 33. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, V_{DDUSB}, V_{DDMEM}, V_{DDOTP}, and CLKIN Pins are Stable and Within Specification	$3500 \times t_{CKIN}$		ns



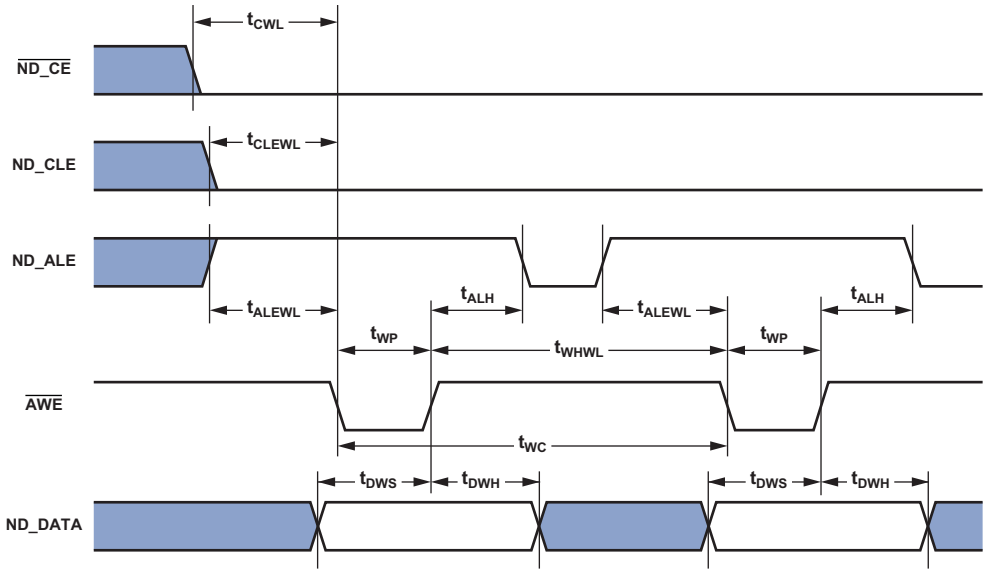
In Figure 10, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}, V_{DDUSB}, V_{DDMEM}, and V_{DDOTP}.

Figure 10. Power-Up Reset Timing



In Figure 13, ND_DATA is ND_D0–D7.

Figure 13. NAND Flash Controller Interface Timing — Command Write Cycle



In Figure 14, ND_DATA is ND_D0–D7.

Figure 14. NAND Flash Controller Interface Timing — Address Write Cycle

SDRAM Interface Timing

Table 37. SDRAM Interface Timing for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V or 3.3 V Nominal Min	V_{DDMEM} 2.5 V or 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	1.3		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	12.5		10		ns
t_{SCLKH}	CLKOUT Width High	5.0		4.0		ns
t_{SCLKL}	CLKOUT Width Low	5.0		4.0		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		5.0		4.0	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		5.5		5.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	0.0		0.0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 14 and Table 17. Package type and reduced supply voltages affect the best-case values listed here.
[2] Command balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

Table 38. SDRAM Interface Timing for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V or 3.3 V Nominal Min	V_{DDMEM} 2.5 V or 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	1.0		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	10		7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		2.5		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		4.0		4.0	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		5.0		4.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	0.0		0.0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 14 and Table 17. Package type and reduced supply voltages affect the best-case values listed here.
[2] Command balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

Parallel Peripheral Interface Timing

Table 41 and Figure 20 on Page 51, Figure 24 on Page 55, and Figure 27 on Page 57 describe parallel peripheral interface operations.

Table 41. Parallel Peripheral Interface Timing for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{PCLKW}	PPI_CLK Width[1]	6.4		6.4		ns
t_{PCLK}	PPI_CLK Period[1]	25.0		20.0		ns
Timing Requirements - GP Input and Frame Capture Modes						
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.2		1.2		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	4.1		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	2.0		1.6		ns
Switching Characteristics - GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.2		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	2.3		1.9		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.

Table 42. Parallel Peripheral Interface Timing for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{PCLKW}	PPI_CLK Width[1]	6.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		15.0		ns
Timing Requirements - GP Input and Frame Capture Modes						
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	2.0		1.6		ns
Switching Characteristics - GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.0		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	2.3		1.9		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.

Serial Ports

Table 43 through Table 47 on Page 57 and Figure 24 on Page 55 through Figure 27 on Page 57 describe serial port operations.

Table 43. Serial Ports—External Clock

		ADSP-BF522/ADSP-BF524/ ADSP-BF526				ADSP-BF523/ADSP-BF525/ ADSP-BF527				
		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements										
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx RSCLKx[1]	3.0		3.0		3.0		3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		3.0		3.0		3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		3.0		3.0		3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.5		3.0		3.5		3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	7.0		4.5		7.0		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	$2.0 \times t_{SCLK}$		$2.0 \times t_{SCLK}$		$2.0 \times t_{SCLK}$		$2.0 \times t_{SCLK}$		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[2]	$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[2]	$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		ns
Switching Characteristics										
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		10.0		10.0		10.0		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]	0.0		0.0		0.0		0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[3]		10.0		10.0		10.0		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[3]	0.0		0.0		0.0		0.0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested.
[3] Referenced to drive edge.

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 49 and Figure 29 describe SPI port slave operations.

Table 49. Serial Peripheral Interface (SPI) Port—Slave Timing

		ADSP-BF522/ADSP-BF524/ ADSP-BF526				ADSP-BF523/ADSP-BF525/ ADSP-BF527				
		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements										
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	2.0		1.6		1.6		1.6		ns
Switching Characteristics										
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	12.0	0	10.3	0	12.0	0	10.3	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	11.0	0	8.5	0	8.5	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		0		0		ns

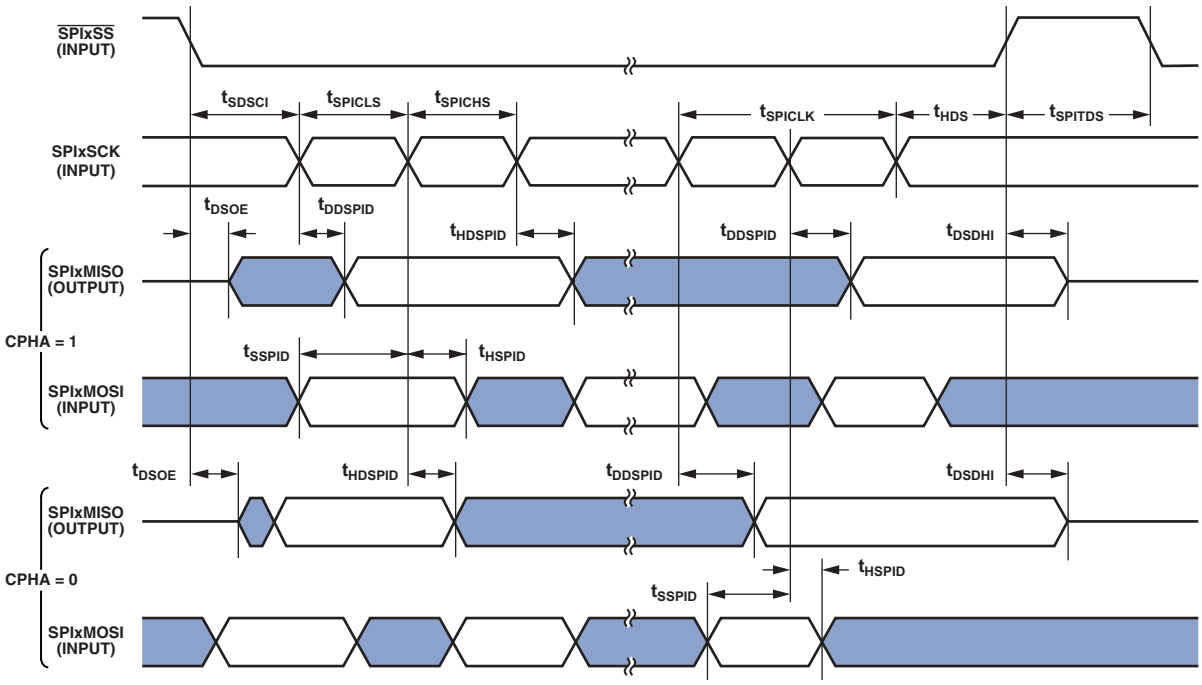


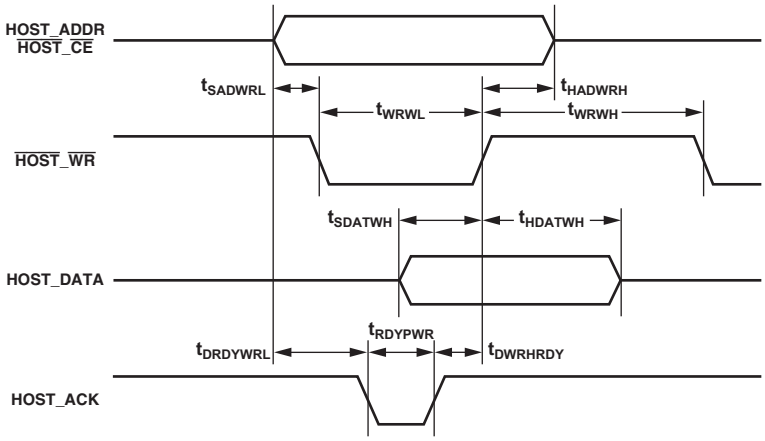
Figure 29. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing

Table 50 describes the USB On-The-Go receive and transmit operations.

Table 50. USB On-The-Go—Receive and Transmit Timing

		ADSP-BF522/ADSP-BF524/ADSP-BF526				ADSP-BF523/ADSP-BF525/ ADSP-BF527				
		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements										
f_{USBS}	USB_XI Frequency	12	33.3	12	33.3	9	33.3	9	33.3	MHz
FS_{USB}	USB_XI Clock Frequency Stability	–50	+50	–50	+50	–50	+50	–50	+50	ppm



In Figure 35, HOST_DATA is HOST_D0–D15.

Figure 35. HOSTDP A/C- Host Write Cycle

10/100 Ethernet MAC Controller Timing

Table 58 through Table 63 and Figure 36 through Figure 41 describe the 10/100 Ethernet MAC Controller operations.

Table 58. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Parameter[1]		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		Unit
		Min	Max	Min	Max	
Timing Requirements						
$t_{ERXCLKF}$	ERxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	None	25 + 1%	MHz
$t_{ERXCLKW}$	ERxCLK Width (t_{ERxCLK} = ERxCLK Period)	$t_{ERxCLK} \times 40\%$	$t_{ERxCLK} \times 60\%$	$t_{ERxCLK} \times 35\%$	$t_{ERxCLK} \times 65\%$	ns
$t_{ERXCLKIS}$	Rx Input Valid to ERxCLK Rising Edge (Data In Setup)	7.5		7.5		ns
$t_{ERXCLKIH}$	ERxCLK Rising Edge to Rx Input Invalid (Data In Hold)	7.5		7.5		ns

[1] MII inputs synchronous to ERxCLK are ERxD3–0, ERxDV, and ERxER.

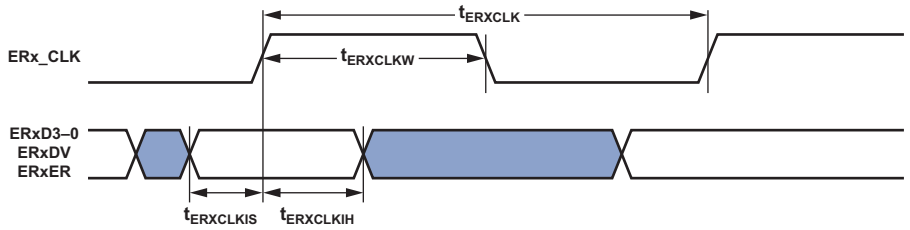


Figure 36. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Table 59. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

Parameter[1]		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		Unit
		Min	Max	Min	Max	
Switching Characteristics						
$t_{ETXCLKF}$	ETxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	None	25 + 1%	MHz
$t_{ETXCLKW}$	ETxCLK Width (t_{ETxCLK} = ETxCLK Period)	$t_{ETxCLK} \times 40\%$	$t_{ETxCLK} \times 60\%$	$t_{ETxCLK} \times 35\%$	$t_{ETxCLK} \times 65\%$	ns
$t_{ETXCLKOV}$	ETxCLK Rising Edge to Tx Output Valid (Data Out Valid)		20		20	ns
$t_{ETXCLKOH}$	ETxCLK Rising Edge to Tx Output Invalid (Data Out Hold)	0		0		ns

[1] MII outputs synchronous to ETxCLK are ETxD3–0.

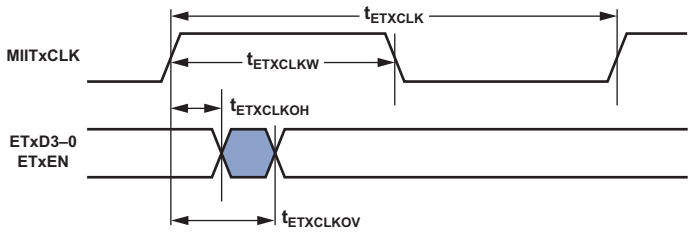


Figure 37. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

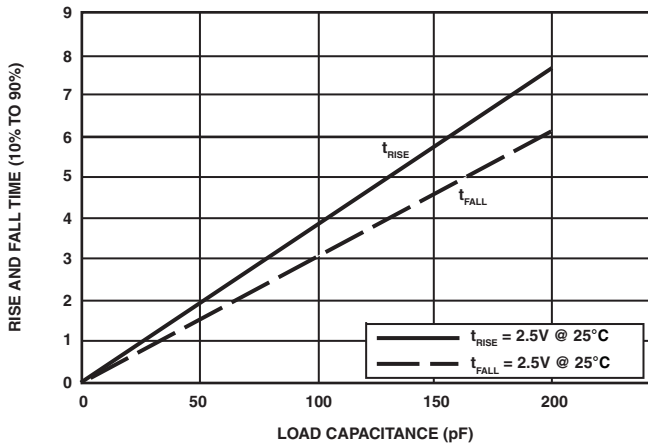


Figure 74. Driver Type G Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

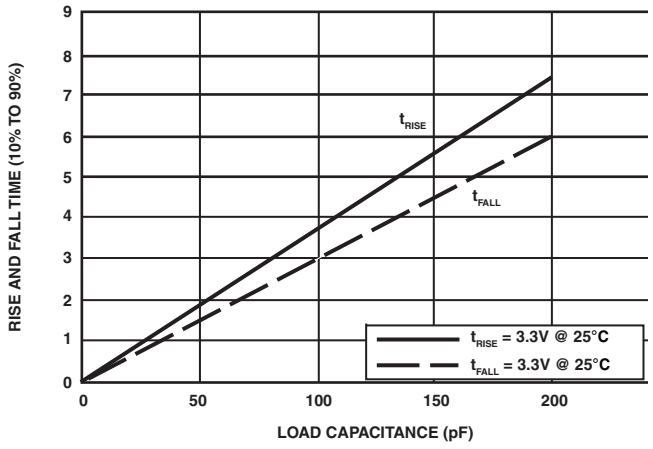


Figure 75. Driver Type G Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 66

P_D = Power dissipation — For a description, see Total Power Dissipation on Page 35.

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 66, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 65. Thermal Characteristics for BC-208-1 Package

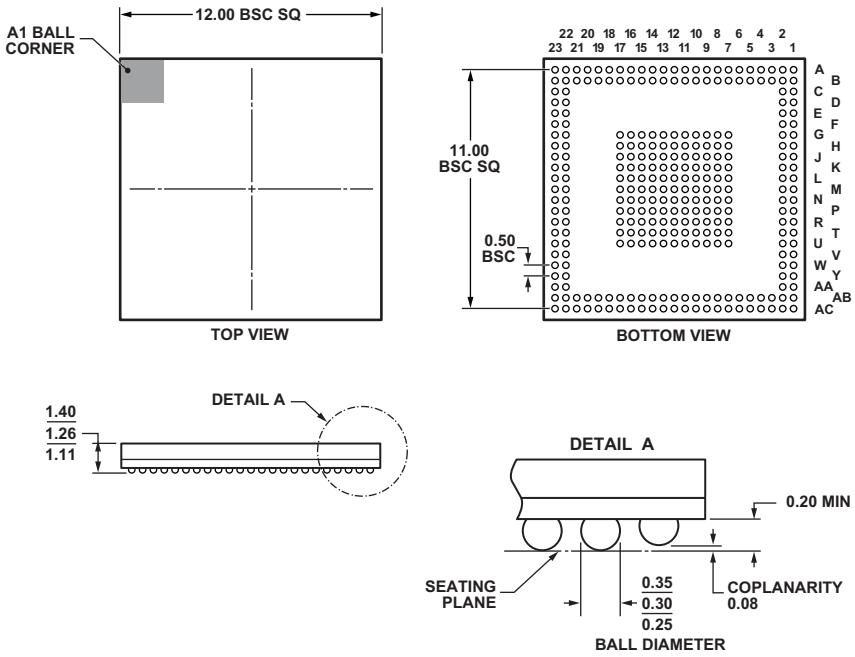
Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	23.20	°C/W
θ_{JMA}	1 linear m/s air flow	20.20	°C/W
θ_{JMA}	2 linear m/s air flow	19.20	°C/W
θ_{JB}		13.05	°C/W
θ_{JC}		6.92	°C/W
Ψ_{JT}	0 linear m/s air flow	0.18	°C/W
Ψ_{JT}	1 linear m/s air flow	0.27	°C/W
Ψ_{JT}	2 linear m/s air flow	0.32	°C/W

Table 66. Thermal Characteristics for BC-289-2 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	34.5	°C/W
θ_{JMA}	1 linear m/s air flow	31.1	°C/W
θ_{JMA}	2 linear m/s air flow	29.8	°C/W
θ_{JB}		20.3	°C/W
θ_{JC}		8.8	°C/W
Ψ_{JT}	0 linear m/s air flow	0.24	°C/W
Ψ_{JT}	1 linear m/s air flow	0.44	°C/W
Ψ_{JT}	2 linear m/s air flow	0.53	°C/W

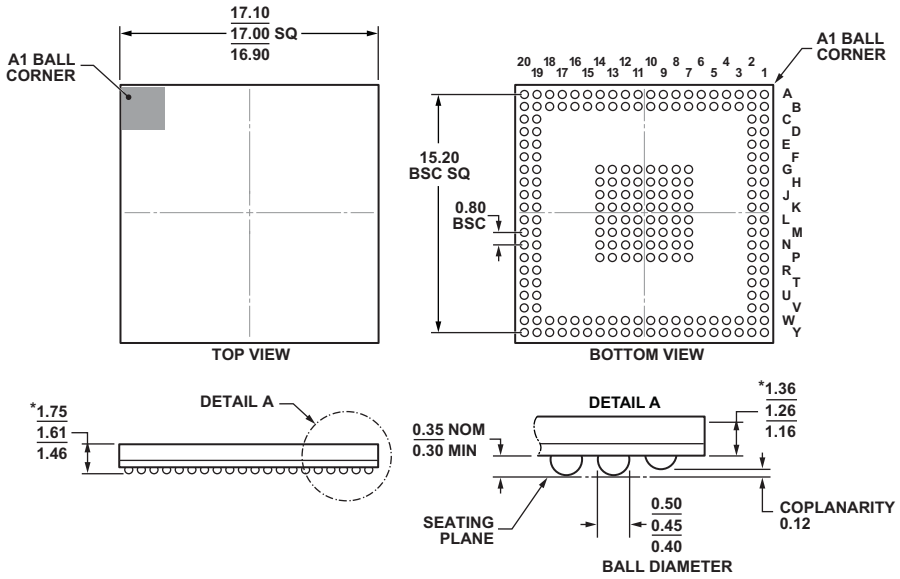
OUTLINE DIMENSIONS

Dimensions in the outline dimension figures (Figure 80 and Figure 81) are shown in millimeters.



*COMPLIANT WITH JEDEC STANDARD MO-275-GGCE-1

Figure 80. 289-Ball CSP_BGA (BC-289-2)



*COMPLIANT TO JEDEC STANDARDS MO-275-MMAB-1 WITH EXCEPTION TO PACKAGE HEIGHT AND THICKNESS.

Figure 81. 208-Ball CSP_BGA (BC-208-2)

SURFACE-MOUNT DESIGN

Table 71 is provided as an aid to PCB design. For industry-standard design recommendations, refer to *IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 71. Surface-Mount Design Supplement

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
289-Ball CSP_BGA	Solder Mask Defined	0.26 mm diameter	0.35 mm diameter
208-Ball CSP_BGA	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

AUTOMOTIVE PRODUCTS

The ADBF525W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 72 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific automotive Reliability reports for these models.

Table 72. Automotive Products

Automotive Models[1, 2]	Temperature Range[3]	Package Description	Package Option	Instruction Rate (Max)
ADBF525WBBCZ4xx	–40°C to +85°C	208-Ball CSP_BGA	BC-208-2	400 MHz
ADBF525WBBCZ5xx	–40°C to +85°C	208-Ball CSP_BGA	BC-208-2	533 MHz
ADBF525WYBCZxxx	–40°C to +105°C	208-Ball CSP_BGA	BC-208-2	For product details, please contact your ADI account representative.

[1] Z = RoHS Compliant Part.
[2] The information indicated by x in the model number will be provided by your ADI account representative.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors on Page 30 for junction temperature (T_J) specification which is the only temperature specification.