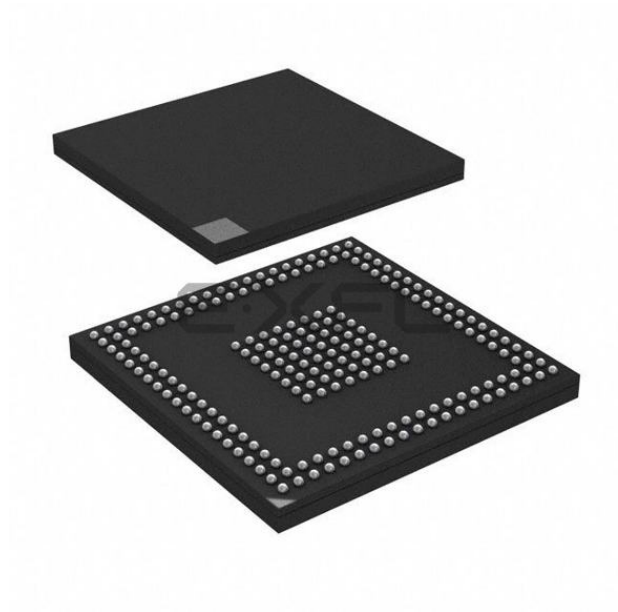


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	DMA, I²C, PPI, SPI, SPORT, UART, USB
Clock Rate	533MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf525wbbcz502

controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	$\overline{\text{RESET}}$	RST
2	Nonmaskable Interrupt	$\overline{\text{NMI}}$
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	General Purpose Interrupt (at $\overline{\text{RESET}}$)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Registers	
PLL Wakeup Interrupt	IVG7	0	0	IAR0	IMASK0, ISR0, IWR0
DMA Error 0 (generic)	IVG7	1	0	IAR0	IMASK0, ISR0, IWR0
DMAR0 Block Interrupt	IVG7	2	0	IAR0	IMASK0, ISR0, IWR0
DMAR1 Block Interrupt	IVG7	3	0	IAR0	IMASK0, ISR0, IWR0
DMAR0 Overflow Error	IVG7	4	0	IAR0	IMASK0, ISR0, IWR0
DMAR1 Overflow Error	IVG7	5	0	IAR0	IMASK0, ISR0, IWR0
PPI Error	IVG7	6	0	IAR0	IMASK0, ISR0, IWR0
MAC Status	IVG7	7	0	IAR0	IMASK0, ISR0, IWR0
SPORT0 Status	IVG7	8	0	IAR1	IMASK0, ISR0, IWR0
SPORT1 Status	IVG7	9	0	IAR1	IMASK0, ISR0, IWR0
Reserved	IVG7	10	0	IAR1	IMASK0, ISR0, IWR0
Reserved	IVG7	11	0	IAR1	IMASK0, ISR0, IWR0
UART0 Status	IVG7	12	0	IAR1	IMASK0, ISR0, IWR0
UART1 Status	IVG7	13	0	IAR1	IMASK0, ISR0, IWR0
RTC	IVG8	14	1	IAR1	IMASK0, ISR0, IWR0
DMA Channel 0 (PPI/NFC)	IVG8	15	1	IAR1	IMASK0, ISR0, IWR0
DMA Channel 3 (SPORT0 RX)	IVG9	16	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 4 (SPORT0 TX)	IVG9	17	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 5 (SPORT1 RX)	IVG9	18	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 6 (SPORT1 TX)	IVG9	19	2	IAR2	IMASK0, ISR0, IWR0
TWI	IVG10	20	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 7 (SPI)	IVG10	21	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 8 (UART0 RX)	IVG10	22	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 9 (UART0 TX)	IVG10	23	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 10 (UART1 RX)	IVG10	24	3	IAR3	IMASK0, ISR0, IWR0
DMA Channel 11 (UART1 TX)	IVG10	25	3	IAR3	IMASK0, ISR0, IWR0

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register — Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers — The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers — The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers — The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel analog-to-digital and digital-to-analog converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate, and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

1. Input mode — Frame syncs and data are inputs into the PPI.
2. Frame capture mode — Frame syncs are outputs from the PPI, but data are inputs.
3. Output mode — Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF52x processors control when to read from the video source(s). PPI_FS1 is an HSYNC output, and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

1. Active video only mode
2. Vertical blanking only mode
3. Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

USB ON-THE-GO DUAL-ROLE DEVICE CONTROLLER

The USB OTG dual-role device controller (USBDRC) provides a low-cost connectivity solution for consumer mobile devices such as cell phones, digital still cameras, and MP3 players, allowing these devices to transfer data using a point-to-point USB connection without the need for a PC host. The USBDRC module can operate in a traditional USB peripheral-only mode as well as the host mode presented in the On-the-Go (OTG) supplement to the USB 2.0 specification. In host mode, the USB module supports transfers at high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps) rates. Peripheral-only mode supports the high- and full-speed transfer rates.

The USB clock (USB_XI) is provided through a dedicated external crystal or crystal oscillator. See Universal Serial Bus (USB) On-The-Go—Receive and Transmit Timing on Page 60 for related timing requirements. If using a crystal to provide the USB clock, use a parallel-resonant, fundamental mode, microprocessor-grade crystal.

The USB on-the-go dual-role device controller includes a phase locked loop with programmable multipliers to generate the necessary internal clocking frequency for USB. The multiplier value should be programmed based on the USB_XI frequency to achieve the necessary 480 MHz internal clock for USB high speed operation. For example, for a USB_XI crystal frequency of 24 MHz, the USB_PLLOSC_CTRL register should be programmed with a multiplier value of 20 to generate a 480 MHz internal clock.

CODE SECURITY WITH LOCKBOX SECURE TECHNOLOGY

A security system consisting of a blend of hardware and software provides customers with a flexible and rich set of code security features with Lockbox™ Secure Technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets. See Lockbox Secure Technology Disclaimer on Page 22.

DYNAMIC POWER MANAGEMENT

The processor provides five operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. When configured for a 0 V core supply voltage, the processor enters the hibernate state. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Table 4. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full-On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the control input to the PLL by setting the PLL_OFF bit in the PLL control register. This register can be accessed with a user-callable routine in the on-chip ROM called bfrom_SysControl(). If disabled, the PLL control input must be re-enabled before transitioning to the full-on or sleep modes.

For more information about PLL controls, see the "Dynamic Power Management" chapter in the ADSP-BF52x Blackfin Processor Hardware Reference.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically, an external event or RTC activity wakes up the processor. When in the sleep mode, asserting a wakeup enabled in the SIC_IWRx registers causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full-on mode. If BYPASS is enabled, the processor transitions to the active mode.

version 2.1. An I^2C multiplexer can be used to select one processor at a time when booting multiple processors from a single TWI.

- Boot from UART0 host on Port G (BMODE = 0x7) — Using an autobaud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities.

  When performing the autobaud, the UART expects a "@" (0x40) character (eight bits data, one start bit, one stop bit, no parity bit) on the UART0RX pin to determine the bit rate. The UART then replies with an acknowledgement composed of 4 bytes (0xBF, the value of UART0_DLL, the value of UART0_DLH, then 0x00). The host can then download the boot stream. To hold off the host the Blackfin processor signals the host with the boot host wait (HWAIT) signal. Therefore, the host must monitor HWAIT before every transmitted byte.
- Boot from UART1 host on Port F (BMODE = 0x8). Same as BMODE = 0x7 except that the UART1 port is used.
- Boot from SDRAM (BMODE = 0xA) This is a warm boot scenario, where the boot kernel starts booting from address 0x0000 0010. The SDRAM is expected to contain a valid boot stream and the SDRAM controller must be configured by the OTP settings.
- Boot from OTP memory (BMODE = 0xB) — This provides a stand-alone booting method. The boot stream is loaded from on-chip OTP memory. By default, the boot stream is expected to start from OTP page 0x40 and can occupy all public OTP memory up to page 0xDF. This is 2560 bytes. Since the start page is programmable, the maximum size of the boot stream can be extended to 3072 bytes.
- Boot from 8-bit external NAND flash memory (BMODE = 0xC and BMODE = 0xD) — In this mode, auto detection of the NAND flash device is performed.

  BMODE = 0xC, the processor configures PORTF GPIO pins PF7:0 for the NAND data pins and PORTH pins PH15:10 for the NAND control signals.

  BMODE = 0xD, the processor configures PORTH GPIO pins PH7:0 for the NAND data pins and PORTH pins PH15:10 for the NAND control signals.

  For correct device operation pull-up resistors are required on both $\overline{\text{ND\_CE}}$ (PH10) and $\overline{\text{ND\_BUSY}}$ (PH13) signals. By default, a value of 0x0033 is written to the NFC_CTL register. The booting procedure always starts by booting from byte 0 of block 0 of the NAND flash device.

  NAND flash boot supports the following features:

  — Device Auto Detection

  — Error Detection & Correction for maximum reliability

  — No boot stream size limitation

  — Peripheral DMA providing efficient transfer of all data (excluding the ECC parity data)

  — Software-configurable boot mode for booting from boot streams spanning multiple blocks, including bad blocks

  — Software-configurable boot mode for booting from multiple copies of the boot stream, allowing for handling of bad blocks and uncorrectable errors

  — Configurable timing via OTP memory

  Small page NAND flash devices must have a 512-byte page size, 32 pages per block, a 16-byte spare area size, and a bus configuration of 8 bits. By default, all read requests from the NAND flash are followed by four address cycles. If the NAND flash device requires only three address cycles, the device must be capable of ignoring the additional address cycles.

  The small page NAND flash device must comply with the following command set:

  — Reset: 0xFF

  — Read lower half of page: 0x00

  — Read upper half of page: 0x01

  — Read spare area: 0x50

  For large-page NAND-flash devices, the four-byte electronic signature is read in order to configure the kernel for booting, which allows support for multiple large-page devices. The fourth byte of the electronic signature must comply with the specification in Table 9 on Page 20.

  Any NAND flash array configuration from Table 9, excluding 16-bit devices, that also complies with the command set listed below are directly supported by the boot kernel. There are no restrictions on the page size or block size as imposed by the small-page boot kernel.

  For devices consisting of a five-byte signature, only four are read. The fourth must comply as outlined above.

  Large page devices must support the following command set:

  — Reset: 0xFF

  — Read Electronic Signature: 0x90

  — Read: 0x00, 0x30 (confirm command)

  Large-page devices must not support or react to NAND flash command 0x50. This is a small-page NAND flash command used for device auto detection.

  By default, the boot kernel will always issue five address cycles; therefore, if a large page device requires only four cycles, the device must be capable of ignoring the additional address cycles.
- Boot from 16-Bit Host DMA (BMODE = 0xE) — In this mode, the host DMA port is configured in 16-bit Acknowledge mode, with little endian data formatting. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually into the Host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT

SIGNAL DESCRIPTIONS

Signal definitions for the ADSP-BF52x processors are listed in Table 10. In order to maintain maximum function and reduce package size and ball count, some balls have dual, multiplexed functions. In cases where ball function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 10.

All I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs, as noted in Table 10.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements. If no IBIS simulation is performed, it is strongly recommended to add series resistor terminations for all Driver Types A, C and D.

The termination resistors should be placed near the processor to reduce transients and improve signal integrity. The resistance value, typically 33 Ω or 47 Ω, should be chosen to match the average board trace impedance.

Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 10. Signal Descriptions

Signal Name	Type	Function	Driver Type[1]
EBIU			
ADDR19–1	O	Address Bus	A
DATA15–0	I/O	Data Bus	A
$\overline{\text{ABE1–0}}$/*SDQM1–0*	O	Byte Enables/*Data Mask*	A
$\overline{\text{AMS3–0}}$	O	Asynchronous Memory Bank Selects (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control	
$\overline{\text{AOE}}$	O	Asynchronous Output Enable	A
$\overline{\text{ARE}}$	O	Asynchronous Read Enable	A
$\overline{\text{AWE}}$	O	Asynchronous Write Enable	A
$\overline{\text{SRAS}}$	O	SDRAM Row Address Strobe	A
$\overline{\text{SCAS}}$	O	SDRAM Column Address Strobe	A
$\overline{\text{SWE}}$	O	SDRAM Write Enable	A
SCKE	O	SDRAM Clock Enable (Requires a pull-down if hibernate with SDRAM self-refresh is used.)	A
CLKOUT	O	SDRAM Clock Output	B
SA10	O	SDRAM A10 Signal	A
$\overline{\text{SMS}}$	O	SDRAM Bank Select	A

Table 11 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

Table 11. TWI_DT Field Selections and V_{DDEXT}/V_{BUSTWI}

TWI_DT	V_{DDEXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nominal	V_{BUSTWI} Max	Unit
000 (default)[1]	3.3	2.97	3.3	3.63	V
001	1.8	1.7	1.8	1.98	V
010	2.5	2.97	3.3	3.63	V
011	1.8	2.97	3.3	3.63	V
100	3.3	4.5	5	5.5	V
101	1.8	2.25	2.5	2.75	V
110	2.5	2.25	2.5	2.75	V
111 (reserved)	–	–	–	–	–

[1] Designs must comply with the V_{DDEXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Table 12 describes the core clock timing requirements for the ADSP-BF522/ADSP-BF524/ADSP-BF526 processors. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock (see Table 14). Table 13 describes phase-locked loop operating conditions.

Table 12. Core Clock (CCLK) Requirements (All Instruction Rates[1]) for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Parameter		Nominal Voltage Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} =1.33 V minimum)	1.40 V	400[2]	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.235 V minimum)	1.30 V	300	MHz

[1] See the Ordering Guide on Page 88.
[2] Applies to 400 MHz models only. See the Ordering Guide on Page 88.

Table 13. Phase-Locked Loop Operating Conditions for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	70	Instruction Rate[1]	MHz

[1] See the Ordering Guide on Page 88.

Table 14. SCLK Conditions for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

		V_{DDEXT}/V_{DDMEM} 1.8 V Nominal[1]	V_{DDEXT}/V_{DDMEM} 2.5 V or 3.3 V Nominal	
Parameter		Max	Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.33 V)[2]	80	100	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.33 V)	80	80	MHz

[1] If either V_{DDEXT} or V_{DDMEM} are operating at 1.8 V nominal, f_{SCLK} is constrained to 80 MHz.
[2] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 37 on Page 47.

OPERATING CONDITIONS FOR ADSP-BF523/ADSP-BF525/ADSP-BF527 PROCESSORS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive models[2]	0.95		1.26	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 533 MHz models[3]	1.093	1.15	1.26	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 400 MHz models[3]	1.045	1.10	1.20	V
V_{DDEXT}	External Supply Voltage[4, 5]	Nonautomotive models, Internal Voltage Regulator Disabled	1.7	1.8	1.9	V
V_{DDEXT}	External Supply Voltage[4, 5]	Nonautomotive models	2.25	2.5	2.75	V
V_{DDEXT}	External Supply Voltage[4, 5]	Nonautomotive models	3	3.3	3.6	V
V_{DDEXT}	External Supply Voltage[4, 5]	Automotive models	2.7	3.3	3.6	V
V_{DDRTC}	RTC Power Supply Voltage[6]	Nonautomotive models	2.25		3.6	V
V_{DDRTC}	RTC Power Supply Voltage[6]	Automotive models	2.7	3.3	3.6	V
V_{DDMEM}	MEM Supply Voltage[4, 7]	Nonautomotive models	1.7	1.8	1.9	V
V_{DDMEM}	MEM Supply Voltage[4, 7]	Nonautomotive models	2.25	2.5	2.75	V
V_{DDMEM}	MEM Supply Voltage[4, 7]	Nonautomotive models	3	3.3	3.6	V
V_{DDMEM}	MEM Supply Voltage[4, 7]	Automotive models	2.7	3.3	3.6	V
V_{DDOTP}	OTP Supply Voltage[4]		2.25	2.5	2.75	V
V_{PPOTP}	OTP Programming Voltage[4]		2.25	2.5	2.75	V
V_{DDUSB}	USB Supply Voltage[8]		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage[9, 10]	V_{DDEXT}/V_{DDMEM} = 1.90 V	1.1			V
V_{IH}	High Level Input Voltage[10, 11]	V_{DDEXT}/V_{DDMEM} = 2.75 V	1.7			V
V_{IH}	High Level Input Voltage[10, 11]	V_{DDEXT}/V_{DDMEM} = 3.6 V	2.0			V
V_{IHTWI}	High Level Input Voltage[12]	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{BUSTWI}		V_{BUSTWI}	V
V_{IL}	Low Level Input Voltage[9, 10]	V_{DDEXT}/V_{DDMEM} = 1.7 V			0.6	V
V_{IL}	Low Level Input Voltage[10, 11]	V_{DDEXT}/V_{DDMEM} = 2.25 V			0.7	V
V_{IL}	Low Level Input Voltage[10, 11]	V_{DDEXT}/V_{DDMEM} = 3.0 V			0.8	V
V_{ILTWI}	Low Level Input Voltage	V_{DDEXT} = Minimum			0.3 × V_{BUSTWI}[13]	V
T_J	Junction Temperature	289-Ball CSP_BGA @ $T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C
T_J	Junction Temperature	289-Ball CSP_BGA @ $T_{AMBIENT}$ = –40°C to +70°C	–40		+105	°C
T_J	Junction Temperature	208-Ball CSP_BGA @ $T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C
T_J	Junction Temperature	208-Ball CSP_BGA @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] The voltage regulator can generate V_{DDINT} at levels of 1.00 V to 1.20 V with –5% to +5% tolerance when VRCTL is programmed with the bfrom_SysControl() API. This specification is only guaranteed when the API is used.

[2] See Ordering Guide on Page 88.

[3] See Automotive Products on Page 87.

[4] Must remain powered (even if the associated function is not used).

[5] V_{DDEXT} is the supply to the voltage regulator and GPIO.

[6] If not used, power with V_{DDEXT}.

[7] Balls that use V_{DDMEM} are DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AOE}$, $\overline{AMS3–0}$, ARDY, SA10, $\overline{SWE}$, $\overline{SCAS}$, CLKOUT, $\overline{SRAS}$, $\overline{SMS}$, SCKE. These balls are not tolerant to voltages higher than V_{DDMEM}.

[8] When not using the USB peripheral on the ADSP-BF525/ADSP-BF527 or terminating V_{DDUSB} on the ADSP-BF523, V_{DDUSB} must be powered by V_{DDEXT}.

[9] Bidirectional balls (PF15–0, PG15–0, PH15–0) and input balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF52x processors are 2.5 V tolerant (always accept up to 2.7 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[10] Parameter value applies to all input and bidirectional balls, except USB_DP, USB_DM, USB_VBUS, SDA, and SCL.

[11] Bidirectional balls (PF15–0, PG15–0, PH15–0) and input balls (RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF52x processors are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[12] The V_{IHTWI} min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See V_{BUSTWI} min and max values in Table 11 on Page 29.

[13] SDA and SCL are pulled up to V_{BUSTWI}. See Table 11 on Page 29.

Clock Related Operating Conditions for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Table 15 describes the core clock timing requirements for the ADSP-BF523/ADSP-BF525/ADSP-BF527 processors. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock (see Table 17). Table 16 describes phase-locked loop operating conditions.

Use the nominal voltage setting (Table 15) for internal and external regulators.

Table 15. Core Clock (CCLK) Requirements (All Instruction Rates[1]) for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		Nominal Voltage Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V minimum)	1.20 V	600[2]	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.093 V minimum)	1.15 V	533[3]	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V minimum)[4]	1.10 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V minimum)	1.0 V	400	MHz

[1] See the Ordering Guide on Page 88.
[2] Applies to 600 MHz models only. See the Ordering Guide on Page 88.
[3] Applies to 533 MHz and 600 MHz models only. See the Ordering Guide on Page 88.
[4] Applies only to automotive products. See Automotive Products on Page 87.

Table 16. Phase-Locked Loop Operating Conditions for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency (Commercial/Industrial Models)	60	Instruction Rate[1]	MHz
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency (Automotive Models)	70	Instruction Rate[1]	MHz

[1] See the Ordering Guide on Page 88.

Table 17. SCLK Conditions for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

		V_{DDEXT}/V_{DDMEM} 1.8 V Nominal[1]	V_{DDEXT}/V_{DDMEM} 2.5 V or 3.3 V Nominal	
Parameter		Max	Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.14 V)[2]	100	133[3]	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)[2]	100	100	MHz

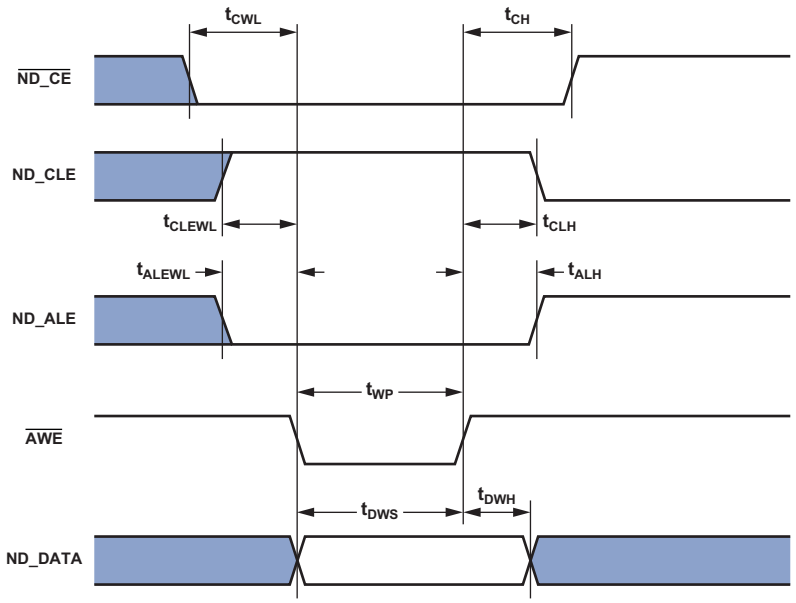
[1] If either V_{DDEXT} or V_{DDMEM} are operating at 1.8 V nominal, f_{SCLK} is constrained to 100 MHz.
[2] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 38 on Page 47.
[3] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 38 on Page 47.

ELECTRICAL CHARACTERISTICS

Table 18. Common Electrical Characteristics for All ADSP-BF52x Processors

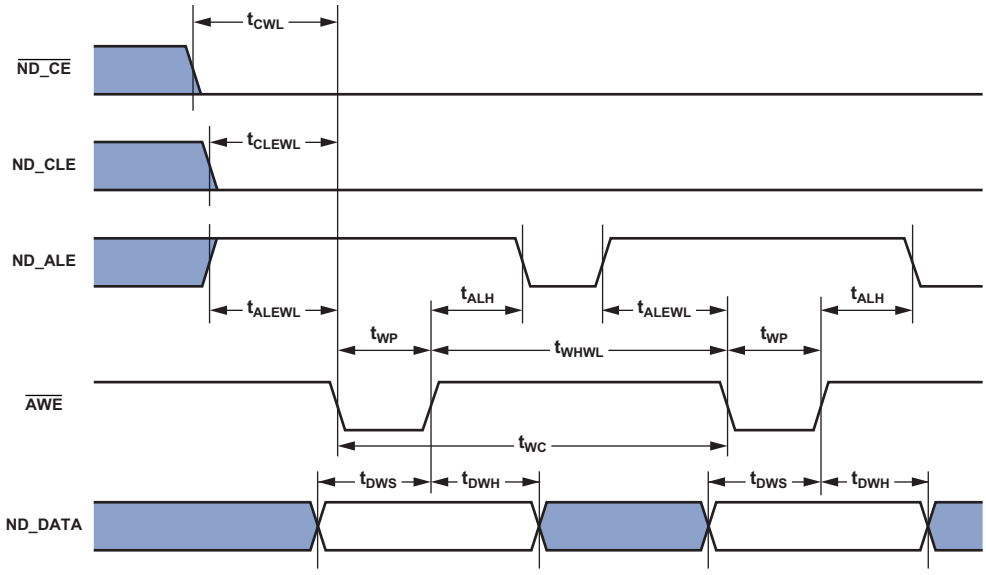
Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 2.25 V, I_{OH} = –0.5 mA	2.0			V
V_{OH}	High Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT}/V_{DDMEM} = 1.7 V/2.25 V/ 3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[1]	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{IL}	Low Level Input Current[1]	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10.0	µA
I_{IHP}	High Level Input Current JTAG[2]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			75.0	µA
I_{OZH}	Three-State Leakage Current[3]	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{OZHTWI}	Three-State Leakage Current[4]	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10.0	µA
I_{OZL}	Three-State Leakage Current[3]	V_{DDEXT}/V_{DDMEM} = 3.6 V, V_{IN} = 0 V			10.0	µA
C_{IN}	Input Capacitance[5,6]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		5	8	pF
C_{INTWI}	Input Capacitance[4,6]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			15	pF

[1] Applies to input balls.
[2] Applies to JTAG input balls (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[3] Applies to three-statable balls.
[4] Applies to bidirectional balls SCL and SDA.
[5] Applies to all signal balls, except SCL and SDA.
[6] Guaranteed, but not tested.



In Figure 13, ND_DATA is ND_D0–D7.

Figure 13. NAND Flash Controller Interface Timing — Command Write Cycle



In Figure 14, ND_DATA is ND_D0–D7.

Figure 14. NAND Flash Controller Interface Timing — Address Write Cycle

SDRAM Interface Timing

Table 37. SDRAM Interface Timing for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V or 3.3 V Nominal Min	V_{DDMEM} 2.5 V or 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	1.3		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	12.5		10		ns
t_{SCLKH}	CLKOUT Width High	5.0		4.0		ns
t_{SCLKL}	CLKOUT Width Low	5.0		4.0		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		5.0		4.0	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		5.5		5.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	0.0		0.0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 14 and Table 17. Package type and reduced supply voltages affect the best-case values listed here.
[2] Command balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

Table 38. SDRAM Interface Timing for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		V_{DDMEM} 1.8 V Nominal Min	V_{DDMEM} 1.8 V Nominal Max	V_{DDMEM} 2.5 V or 3.3 V Nominal Min	V_{DDMEM} 2.5 V or 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SSDAT}	Data Setup Before CLKOUT	1.5		1.5		ns
t_{HSDAT}	Data Hold After CLKOUT	1.0		0.8		ns
Switching Characteristics						
t_{SCLK}	CLKOUT Period[1]	10		7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		2.5		ns
t_{DCAD}	Command, Address, Data Delay After CLKOUT[2]		4.0		4.0	ns
t_{HCAD}	Command, Address, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		5.0		4.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	0.0		0.0		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification discussed in Table 14 and Table 17. Package type and reduced supply voltages affect the best-case values listed here.
[2] Command balls include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

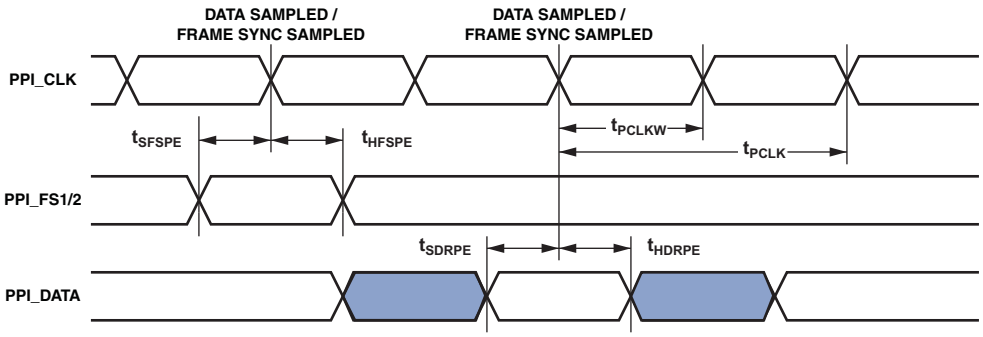


Figure 20. PPI GP Rx Mode with External Frame Sync Timing

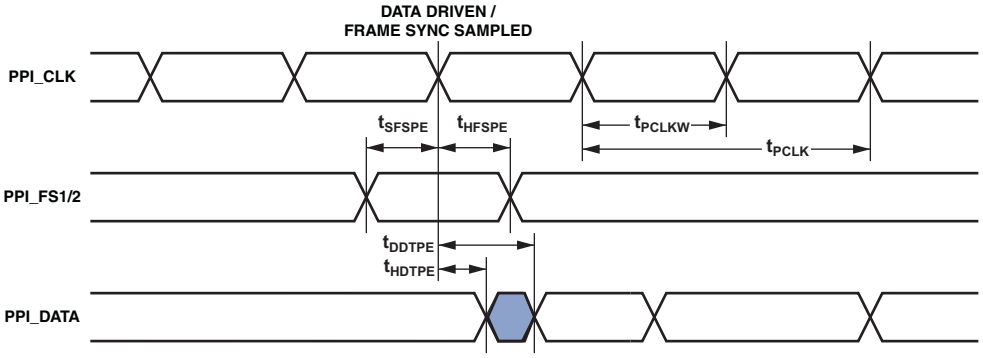


Figure 21. PPI GP Tx Mode with External Frame Sync Timing

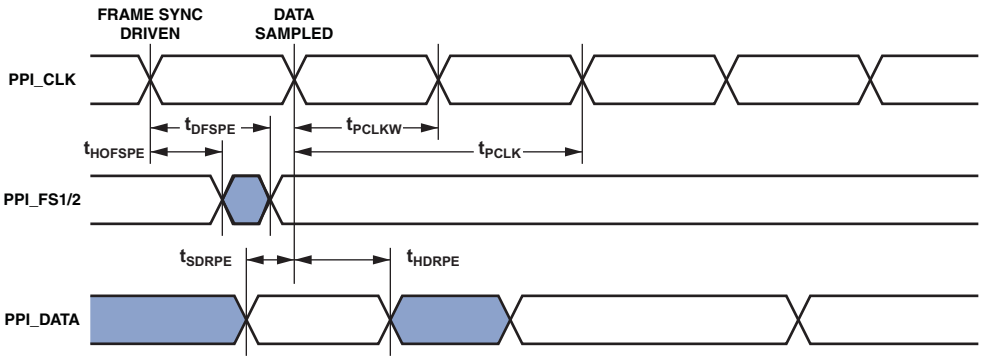


Figure 22. PPI GP Rx Mode with Internal Frame Sync Timing

Serial Ports

Table 43 through Table 47 on Page 57 and Figure 24 on Page 55 through Figure 27 on Page 57 describe serial port operations.

Table 43. Serial Ports—External Clock

		ADSP-BF522/ADSP-BF524/ ADSP-BF526				ADSP-BF523/ADSP-BF525/ ADSP-BF527				
		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements										
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx RSCLKx[1]	3.0		3.0		3.0		3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		3.0		3.0		3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		3.0		3.0		3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.5		3.0		3.5		3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	7.0		4.5		7.0		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	$2.0 \times t_{SCLK}$		$2.0 \times t_{SCLK}$		$2.0 \times t_{SCLK}$		$2.0 \times t_{SCLK}$		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[2]	$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[2]	$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		$4.0 \times t_{SCLKE}$		ns
Switching Characteristics										
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		10.0		10.0		10.0		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]	0.0		0.0		0.0		0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[3]		10.0		10.0		10.0		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[3]	0.0		0.0		0.0		0.0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested.
[3] Referenced to drive edge.

Table 44. Serial Ports—Internal Clock for ADSP-BF522/ADSP-BF524/ADSP-BF526 Processors

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V or 3.3 V Nominal Min	V_{DDEXT} 2.5 V or 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	11.0		9.6		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–1.5		–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	11.0		9.6		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	–1.5		–1.5		ns
Switching Characteristics						
t_{SCLKIW}	TSCLKx/RSCLKx Width	10.0		8.0		ns
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	–2.0		–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[2]		3.0		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[2]	–1.8		–1.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 45. Serial Ports—Internal Clock for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors

Parameter		V_{DDEXT} 1.8 V Nominal Min	V_{DDEXT} 1.8 V Nominal Max	V_{DDEXT} 2.5 V or 3.3 V Nominal Min	V_{DDEXT} 2.5 V or 3.3 V Nominal Max	Unit
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	11.0		9.6		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–1.5		–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	11.0		9.6		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	–1.5		–1.5		ns
Switching Characteristics						
t_{SCLKIW}	TSCLKx/RSCLKx Width	4.5		4.5		ns
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	–1.0		–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[2]		3.0		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[2]	–1.8		–1.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Serial Peripheral Interface (SPI) Port—Master Timing

Table 48 and Figure 28 describe SPI port master operations.

Table 48. Serial Peripheral Interface (SPI) Port—Master Timing

		ADSP-BF522/ADSP-BF524/ ADSP-BF526				ADSP-BF523/ADSP-BF525/ ADSP-BF527				
		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		
Parameter		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements										
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	11.6		9.6		11.6		9.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		–1.5		ns
Switching Characteristics										
t_{SDSCIM}	$\overline{SPISELx}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		–1.0		–1.0		ns

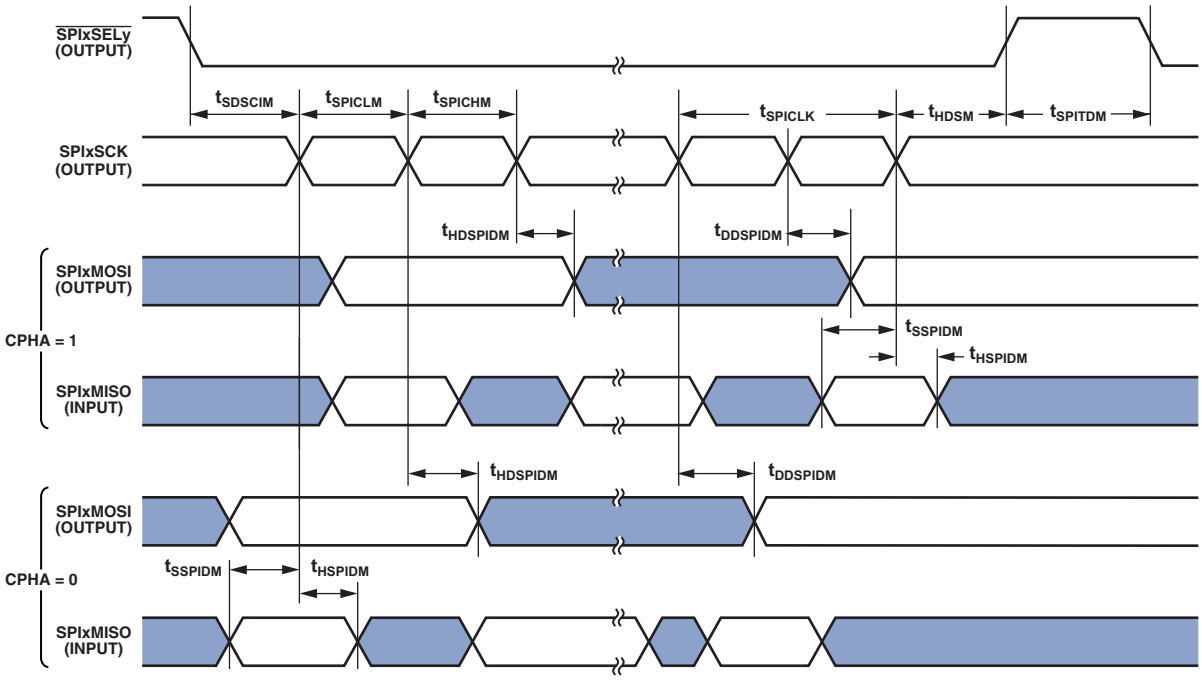


Figure 28. Serial Peripheral Interface (SPI) Port—Master Timing

HOSTDP A/C Timing- Host Read Cycle

Table 56 describes the HOSTDP A/C Host Read Cycle timing requirements.

Table 56. Host Read Cycle Timing Requirements

Parameter		ADSP-BF522/ADSP-BF524/ADSP-BF526				ADSP-BF523/ADSP-BF525/ADSP-BF527				Unit
		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		V_{DDEXT} 1.8 V Nominal		V_{DDEXT} 2.5 V or 3.3 V Nominal		
		Min	Max	Min	Max	Min	Max	Min	Max	
Timing Requirements										
t_{SADRDL}	HOST_ADDR and $\overline{HOST\_CE}$ Setup before $\overline{HOST\_RD}$ falling edge	4		4		4		4		ns
t_{HADRDH}	HOST_ADDR and $\overline{HOST\_CE}$ Hold after $\overline{HOST\_RD}$ rising edge	2.5		2.5		2.5		2.5		ns
t_{RDWL}	$\overline{HOST\_RD}$ pulse width low (ACK mode)	$t_{DRDYRDL}$ + t_{RDYPRD} + $t_{DRDHRDY}$		$t_{DRDYRDL}$ + t_{RDYPRD} + $t_{DRDHRDY}$		$t_{DRDYRDL}$ + t_{RDYPRD} + $t_{DRDHRDY}$		$t_{DRDYRDL}$ + t_{RDYPRD} + $t_{DRDHRDY}$		ns
t_{RDWL}	$\overline{HOST\_RD}$ pulse width low (INT mode)	1.5 × t_{SCLK} + 8.7		1.5 × t_{SCLK} + 8.7		1.5 × t_{SCLK} + 8.7		1.5 × t_{SCLK} + 8.7		ns
t_{RDWH}	$\overline{HOST\_RD}$ pulse width high or time between $\overline{HOST\_RD}$ rising edge and $\overline{HOST\_WR}$ falling edge	2 × t_{SCLK}		2 × t_{SCLK}		2 × t_{SCLK}		2 × t_{SCLK}		ns
$t_{DRDHRDY}$	$\overline{HOST\_RD}$ rising edge delay after HOST_ACK rising edge (ACK mode)	2.0		2.0		0		0		ns
Switching Characteristics										
$t_{SDATRDY}$	Data valid prior HOST_ACK rising edge (ACK mode)	4.5		3.5		4.5		3.5		ns
$t_{DRDYRDL}$	Host_ACK falling edge after $\overline{HOST\_CE}$ (ACK mode)		12.5		11.25		11.25		11.25	ns
t_{RDYPRD}	HOST_ACK low pulse-width for Read access (ACK mode)		NM[1]		NM[1]		NM[1]		NM[1]	ns
t_{DDARWH}	Data disable after $\overline{HOST\_RD}$		11.0		9.0		9.0		9.0	ns
t_{ACC}	Data valid after $\overline{HOST\_RD}$ falling edge (INT mode)		1.5 × t_{SCLK}		1.5 × t_{SCLK}		1.5 × t_{SCLK}		1.5 × t_{SCLK}	ns
t_{HDARWH}	Data hold after $\overline{HOST\_RD}$ rising edge	1.0		1.0		1.0		1.0		ns

[1] NM (Not Measured) — This parameter is based on t_{SCLK}. It is not measured because the number of SCLK cycles for which HOST_ACK is low depends on the Host DMA FIFO status and is system design dependent.

OUTPUT DRIVE CURRENTS

Figure 43 through Figure 57 show typical current-voltage characteristics for the output drivers of the ADSP-BF52x processors.

The curves represent the current drive capability of the output drivers. See Table 10 on Page 23 for information about which driver type corresponds to a particular ball.

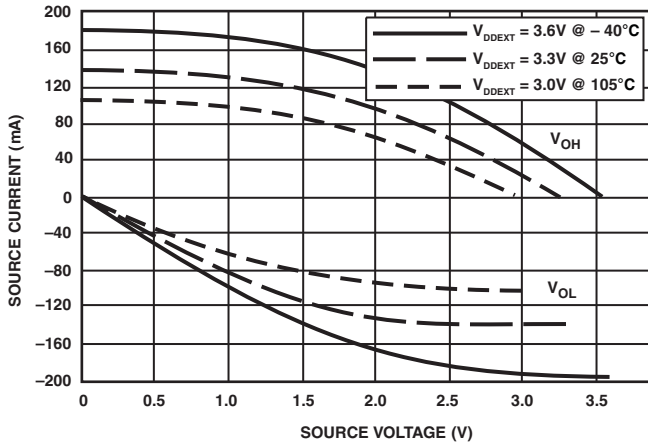


Figure 43. Driver Type A Current (3.3V V_{DDEXT}/V_{DDMEM})

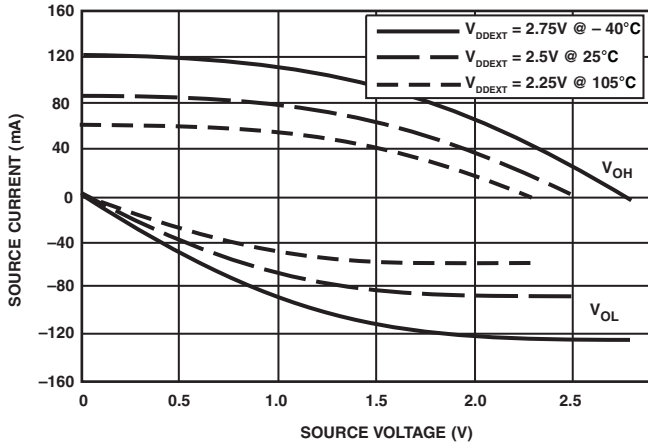


Figure 44. Driver Type A Current (2.5V V_{DDEXT}/V_{DDMEM})

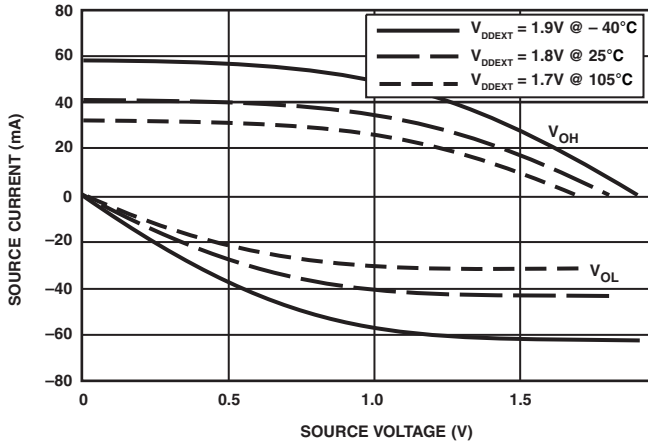


Figure 45. Driver Type A Current (1.8V V_{DDEXT}/V_{DDMEM})

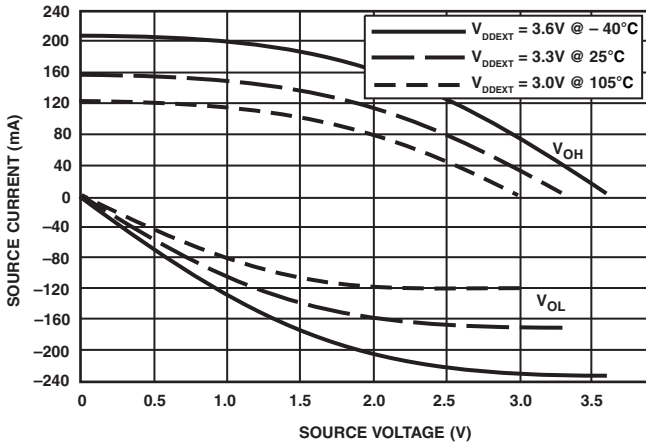


Figure 46. Driver Type B Current (3.3V V_{DDEXT}/V_{DDMEM})

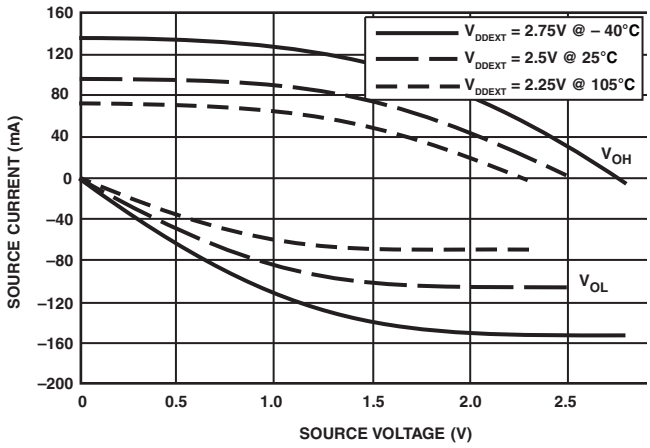


Figure 47. Driver Type B Current (2.5V V_{DDEXT}/V_{DDMEM})

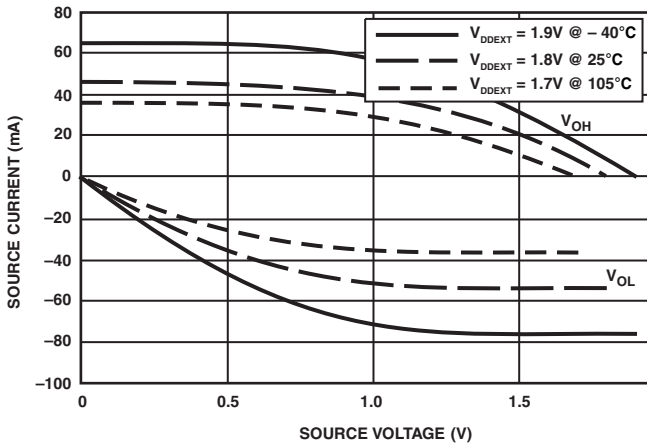


Figure 48. Driver Type B Current (1.8V V_{DDEXT}/V_{DDMEM})

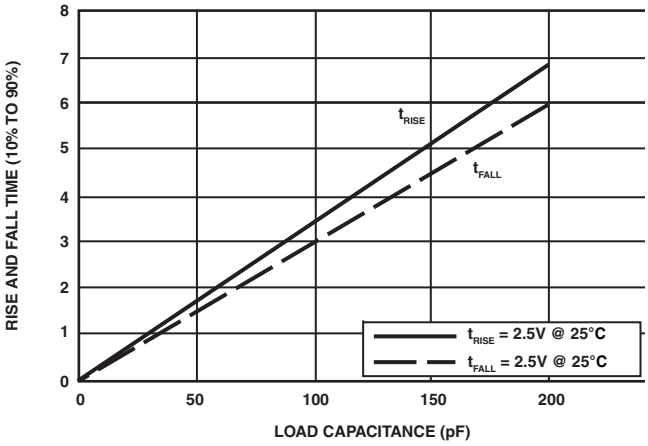


Figure 62. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

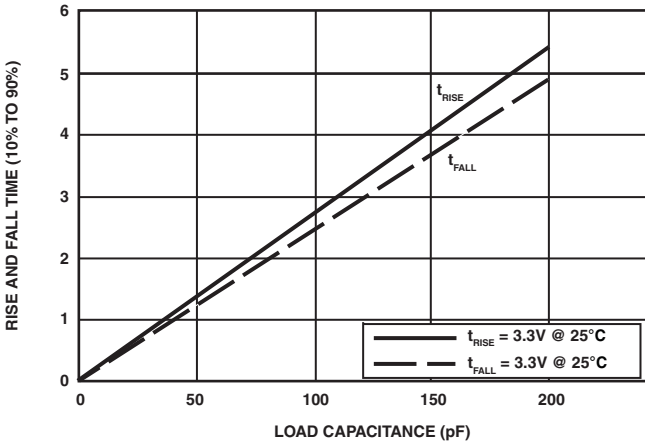


Figure 63. Driver Type A Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

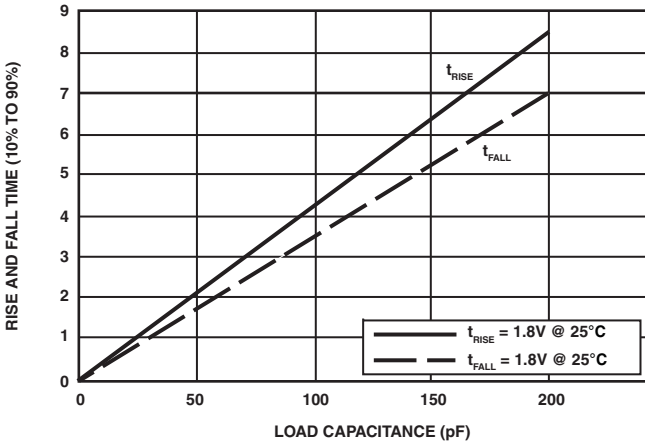


Figure 64. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

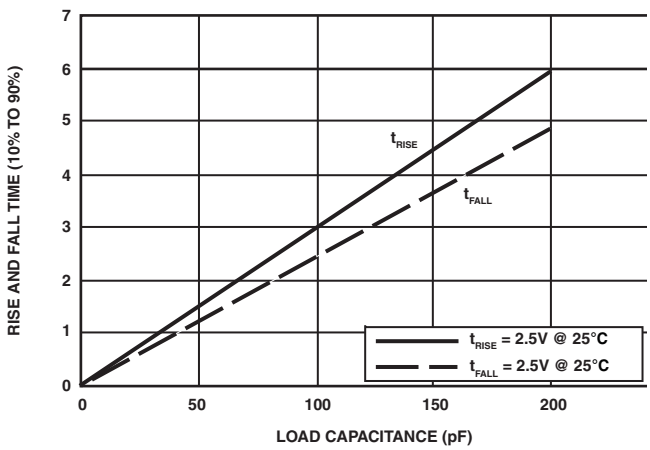


Figure 65. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (2.5V V_{DDEXT}/V_{DDMEM})

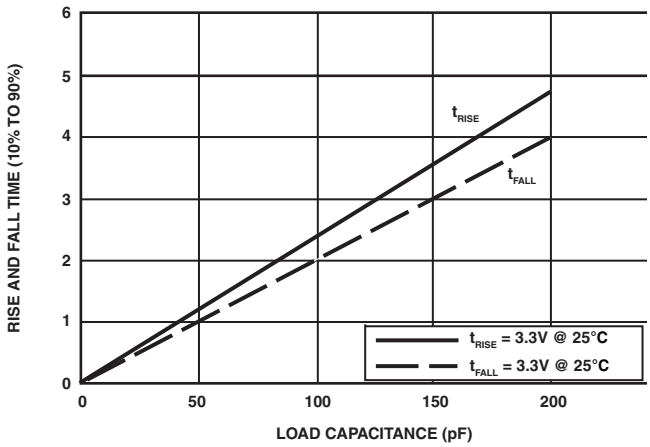


Figure 66. Driver Type B Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (3.3V V_{DDEXT}/V_{DDMEM})

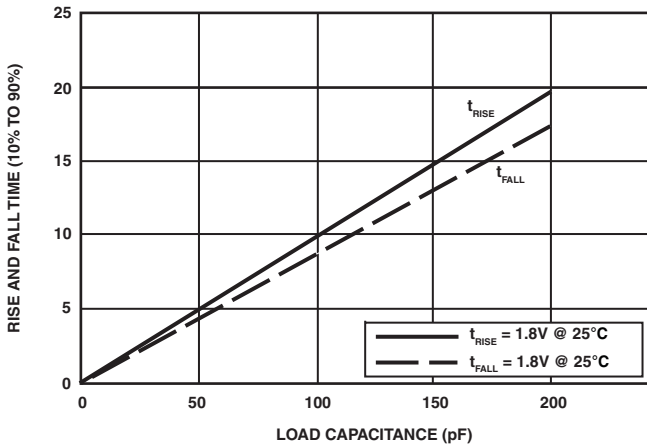


Figure 67. Driver Type C Typical Rise and Fall Times (10%–90%) vs. Load Capacitance (1.8V V_{DDEXT}/V_{DDMEM})

Figure 76 shows the top view of the BC-289-2 CSP_BGA ball configuration. Figure 77 shows the bottom view of the BC-289-2 CSP_BGA ball configuration.

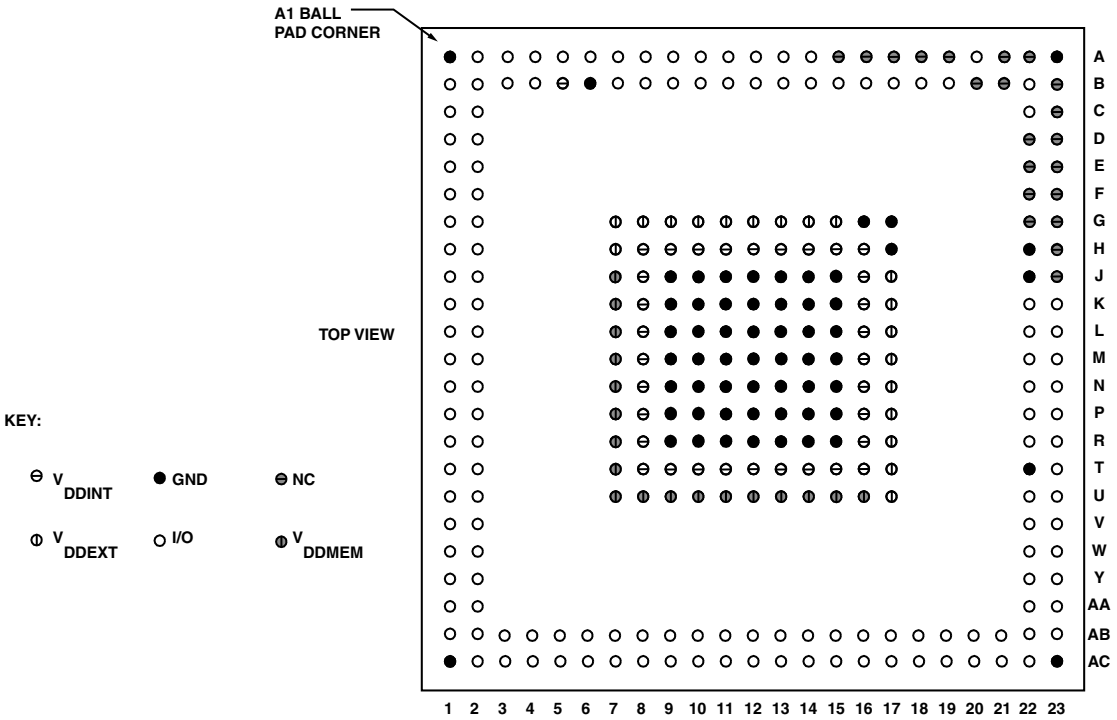


Figure 76. 289-Ball CSP_BGA Ball Configuration (Top View)

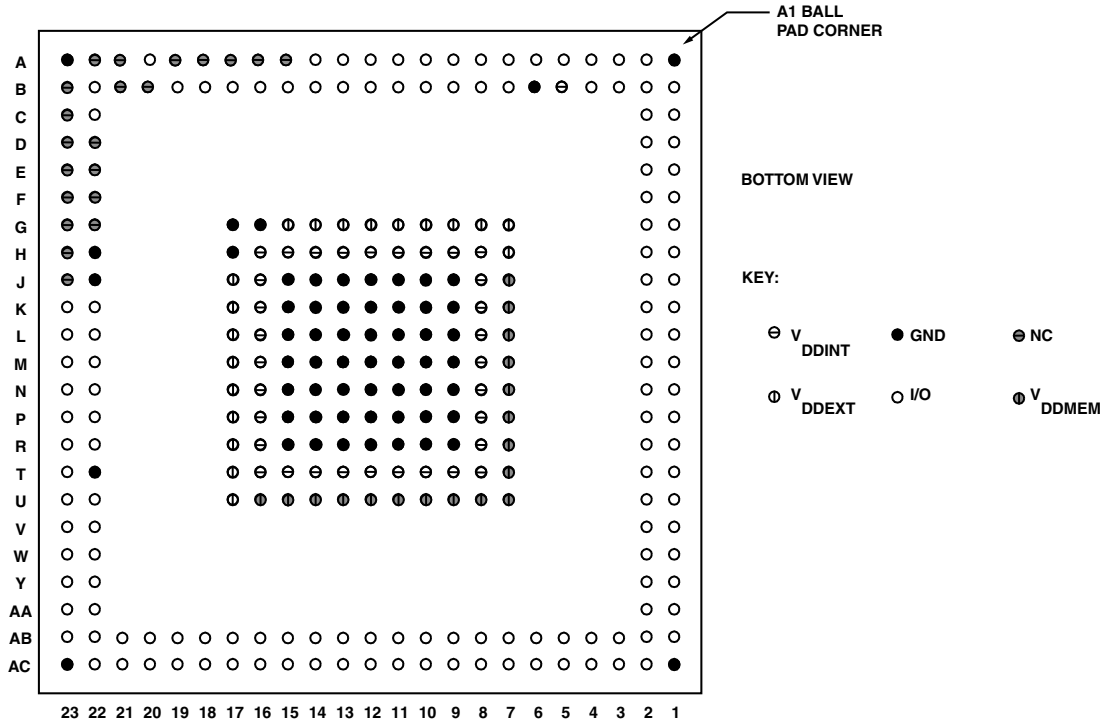


Figure 77. 289-Ball CSP_BGA Ball Configuration (Bottom View)

SURFACE-MOUNT DESIGN

Table 71 is provided as an aid to PCB design. For industry-standard design recommendations, refer to *IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 71. Surface-Mount Design Supplement

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
289-Ball CSP_BGA	Solder Mask Defined	0.26 mm diameter	0.35 mm diameter
208-Ball CSP_BGA	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

AUTOMOTIVE PRODUCTS

The ADBF525W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 72 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific automotive Reliability reports for these models.

Table 72. Automotive Products

Automotive Models[1, 2]	Temperature Range[3]	Package Description	Package Option	Instruction Rate (Max)
ADBF525WBBCZ4xx	–40°C to +85°C	208-Ball CSP_BGA	BC-208-2	400 MHz
ADBF525WBBCZ5xx	–40°C to +85°C	208-Ball CSP_BGA	BC-208-2	533 MHz
ADBF525WYBCZxxx	–40°C to +105°C	208-Ball CSP_BGA	BC-208-2	For product details, please contact your ADI account representative.

[1] Z = RoHS Compliant Part.
[2] The information indicated by x in the model number will be provided by your ADI account representative.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for ADSP-BF523/ADSP-BF525/ADSP-BF527 Processors on Page 30 for junction temperature (T_J) specification which is the only temperature specification.