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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	EBI/EMI, Ethernet, FIFO, SCI, SIO
Peripherals	DMA, POR, WDT
Number of I/O	78
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 1.89V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	176-UFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds76191b125bgv

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's

Table 7.10 16-Bit External Device/Little Endian Access and Data Alignment

	Data Bus				Strobe Signals			
Operation	**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**	**$\overline{WE3}$(BE3), DQMUU**	**$\overline{WE2}$(BE2), DQMUL**	**$\overline{WE1}$(BE1), DQMLU**	**$\overline{WE0}$(BE0), DQMLL**
Byte access at 0	—	—	—	Data 7 to 0	—	—	—	Assert
Byte access at 1	—	—	Data 7 to 0	—	—	—	Assert	—

12.2.11 FIFO Depth Register (FDR)

FDR is a 32-bit readable/writable register that specifies the depth of the transmit and receive FIFOs.

Bit	Bit Name	Initial value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	TFD2 to TFD0	B'001	R/W	Transmit FIFO Depth These bits specify the depth of the transmit FIFO. After the start of the transmission and reception, the setting cannot be changed. 000: 256 bytes 001: 512 bytes Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RFD2 to RFD0	B'001	R/W	Receive FIFO Depth These bits specify the depth of the receive FIFO. After the start of the transmission and reception, the setting cannot be changed. 000: 256 bytes 001: 512 bytes Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
7	REG5	0	R/W*	HIF Internal Register Select
6	REG4	0	R/W*	These bits specify which register among HIFGSR, HIFSCR, HIFMCR, HIFIICR, HIFEICR, HIFADR, HIFDATA, and HIFBCR is accessed by an external device.
5	REG3	0	R/W*	
4	REG2	0	R/W*	
3	REG1	0	R/W*	000000: HIFGSR
2	REG0	0	R/W*	000001: HIFSCR
				000010: HIFMCR
				000011: HIFIICR
				000100: HIFEICR
				000101: HIFADR
				000110: HIFDATA
				001111: HIFBCR
				Other than above: Setting prohibited

20.3.8 Notes

1. The CPU reads from or writes to the UBC registers via the I bus. A desired break may not occur until the instruction to rewrite the UBC registers are executed and the actual values are reflected. In order to know the timing the UBC register is changed, read the last written register. Instructions after then are valid for the newly written register value.
2. UBC cannot monitor access to the L bus and I bus in the same channel.
3. Note on specification of sequential break:

   A condition match occurs when a B-channel match occurs in a bus cycle after an A-channel match occurs in another bus cycle in sequential break setting. Therefore, no break occurs even if a bus cycle, in which an A-channel match and a channel B match occur simultaneously, is set.
4. When user breaks and other exceptions occur by the same instruction, they are handled according to the priority listed in table 5.1 of section 5, Exception Handling. When an exception with a higher priority is generated, no user break occurs.
   - A break before the execution of an instruction is accepted with a priority over other exceptions.
   - When a break after the execution of an instruction or a data access break occurs simultaneously with a re-execution-type exception with a higher priority (including a break before the execution of an instruction), the re-execution-type exception is accepted and the condition match flag is not set (however, there is an exception as explained in 5. of section 20.3.8, Notes). When the exception source of the re-execution type is cleared by exception handling and the same instruction is executed again and completed, the break is generated again and the flag is set.
   - When a break after the execution of an instruction or a data access break occurs simultaneously with a completion-type exception with a higher priority (TRAPA), no break occurs but the condition match flag is set.
5. Note on exception of 4. of section 20.3.8, Notes

   When a break after the execution of an instruction or a data access break occurs during the execution of the instruction in which a CPU address error is generated by data access, the CPU address error has a priority over the break and occurs before the break. The condition match flag is also set at this time.
6. Note when a break occurs in the delay slot

   When a break before the execution of an instruction is set to the delay slot instruction of the RTE instruction, the break does not occur before executing the branch destination of the RTE instruction.
7. User breaks are disabled during USB module standby mode. Do not read from or write to the UBC registers during USB module standby mode; the values are not guaranteed.