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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f16g-a-qfn24

2. Ordering Information

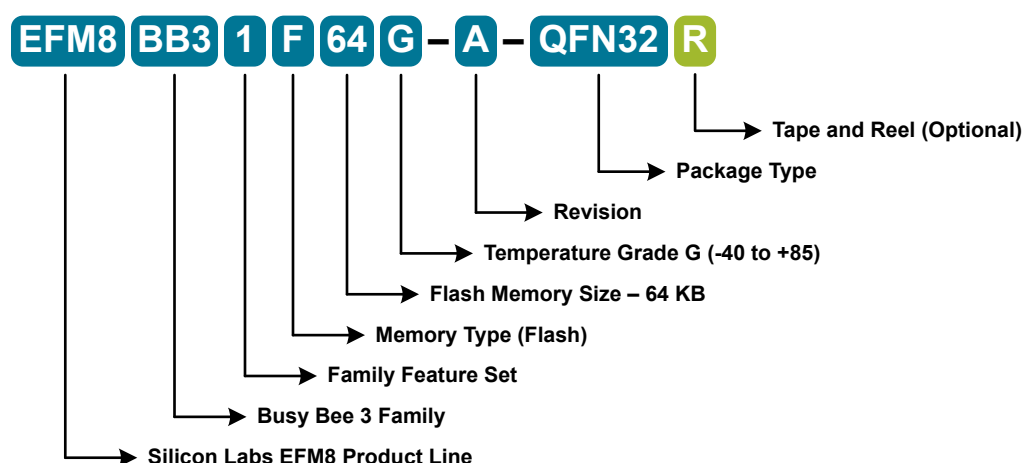


Figure 2.1. EFM8BB3 Part Numbering

All EFM8BB3 family members have the following features:

- CIP-51 Core running up to 49 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-XRAM data transfer
- Two Voltage Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8BB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F64G-A-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F64G-A-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +85 °C	QFN24

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to $\pm 2\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External Crystal / RC / C Oscillator.
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
 - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
 - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 13](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO ^{2,3}	V _{IO}		TBD	—	V _{DD}	V
System Clock Frequency	f _{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T _A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz ²	—	TBD	TBD	mA
		F _{SYSCLK} = 24.5 MHz ²	—	4.5	TBD	mA
		F _{SYSCLK} = 1.53 MHz ²	—	615	TBD	μA
		F _{SYSCLK} = 80 kHz ³	—	155	TBD	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz ²	—	TBD	TBD	mA
		F _{SYSCLK} = 24.5 MHz ²	—	2.8	TBD	mA
		F _{SYSCLK} = 1.53 MHz ²	—	455	TBD	μA
		F _{SYSCLK} = 80 kHz ³	—	145	TBD	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	TBD	μA
		LFO Stopped	—	120	TBD	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	26	TBD	μA
		LFO Stopped	—	21	TBD	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I _{DD}		—	120	TBD	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I _{DD}		—	0.2	—	μA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I _{HFOSC0}	Operating at 24.5 MHz, T _A = 25 °C	—	55	—	μA
High-Frequency Oscillator 1	I _{HFOSC1}	Operating at 49 MHz, T _A = 25 °C	—	TBD	—	μA
Low-Frequency Oscillator	I _{LFOSC}	Operating at 80 kHz, T _A = 25 °C	—	5	—	μA
ADC0 ⁴	I _{ADC}	TBD	—	TBD	TBD	μA
Internal ADC0 Reference ⁵	I _{VREFFS}	Normal Power Mode	—	680	TBD	μA
		Low Power Mode	—	160	TBD	μA
On-chip Precision Reference	I _{VREFP}		—	75	—	μA
Temperature Sensor	I _{TSENSE}		—	75	120	μA
Digital-to-Analog Converters (DAC0, DAC1) ⁶	I _{DAC}		—	125	—	μA

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC0}}$	$T_A = 25^\circ\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC0}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	40	—	ppm/°C
High Frequency Oscillator 1 (49 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	48.25	49	49.75	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC1}}$	$T_A = 25^\circ\text{C}$	—	TBD	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC1}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	TBD	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$\text{PSS}_{\text{LFOSC}}$	$T_A = 25^\circ\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	$V_{\text{DD}} = 3.0\text{ V}$	—	65	—	ppm/°C

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Temperature Coefficient	TC _{OFF}		—	TBD	—	LSB/°C
Slope Error	E _M	12 Bit Mode	—	TBD	TBD	%
		10 Bit Mode	—	TBD	—	%
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	—	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	TBD	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB

Note:

1. Conversion Time does not include Tracking Time. Total Conversion Time is:

$$\text{Total Conversion Time} = [\text{RPT} \times (\text{ADTK} + \text{NUMBITS} + 1) \times \text{T}(\text{SARCLK})] + (\text{T}(\text{ADCCLK}) \times 4)$$

where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC.

2. Absolute input pin voltage is limited by the V_{IO} supply.

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	TBD	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	TBD	—	mV
Slope	M		—	TBD	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	TBD	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity			—	TBD	—	$^{\circ}\text{C}$
Turn-on Time			—	TBD	—	μs

Note:

1. Represents one standard deviation from the mean.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	—	V _{IO} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N _{bits}		6			bits
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	—	dB
Power Supply Rejection Ratio	PSRR _{CP}		—	72	—	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		—	3.5	—	μV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t _{DLY}	Through single CLU	TBD	—	TBD	ns
Clocking Frequency	F _{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 28 shows a typical connection diagram for the power pins of the device.

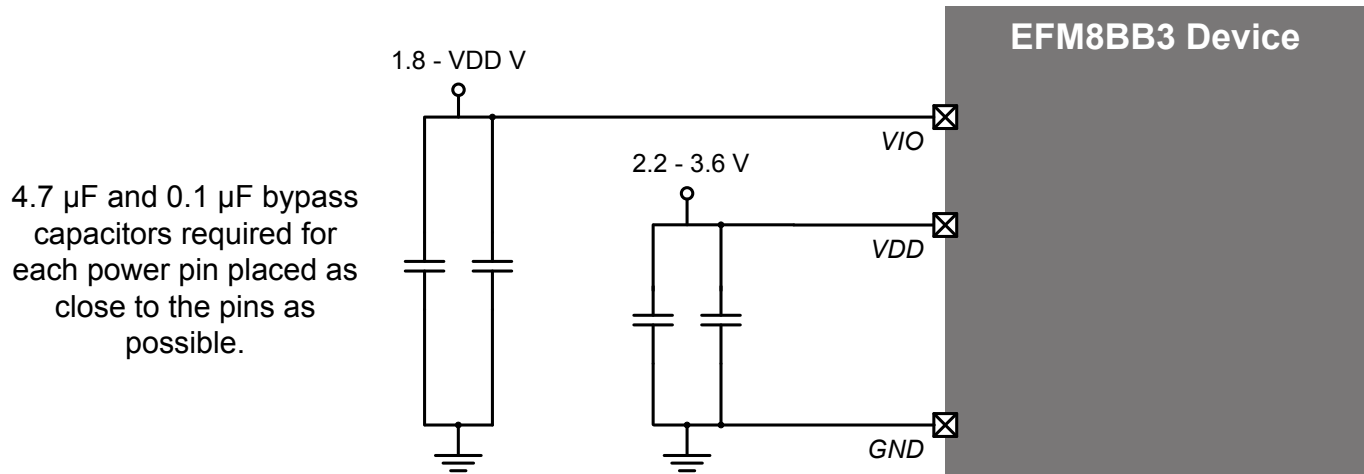


Figure 5.1. Power Connection Diagram

6. Pin Definitions

6.1 EFM8BB3x-QFN32 Pin Definitions

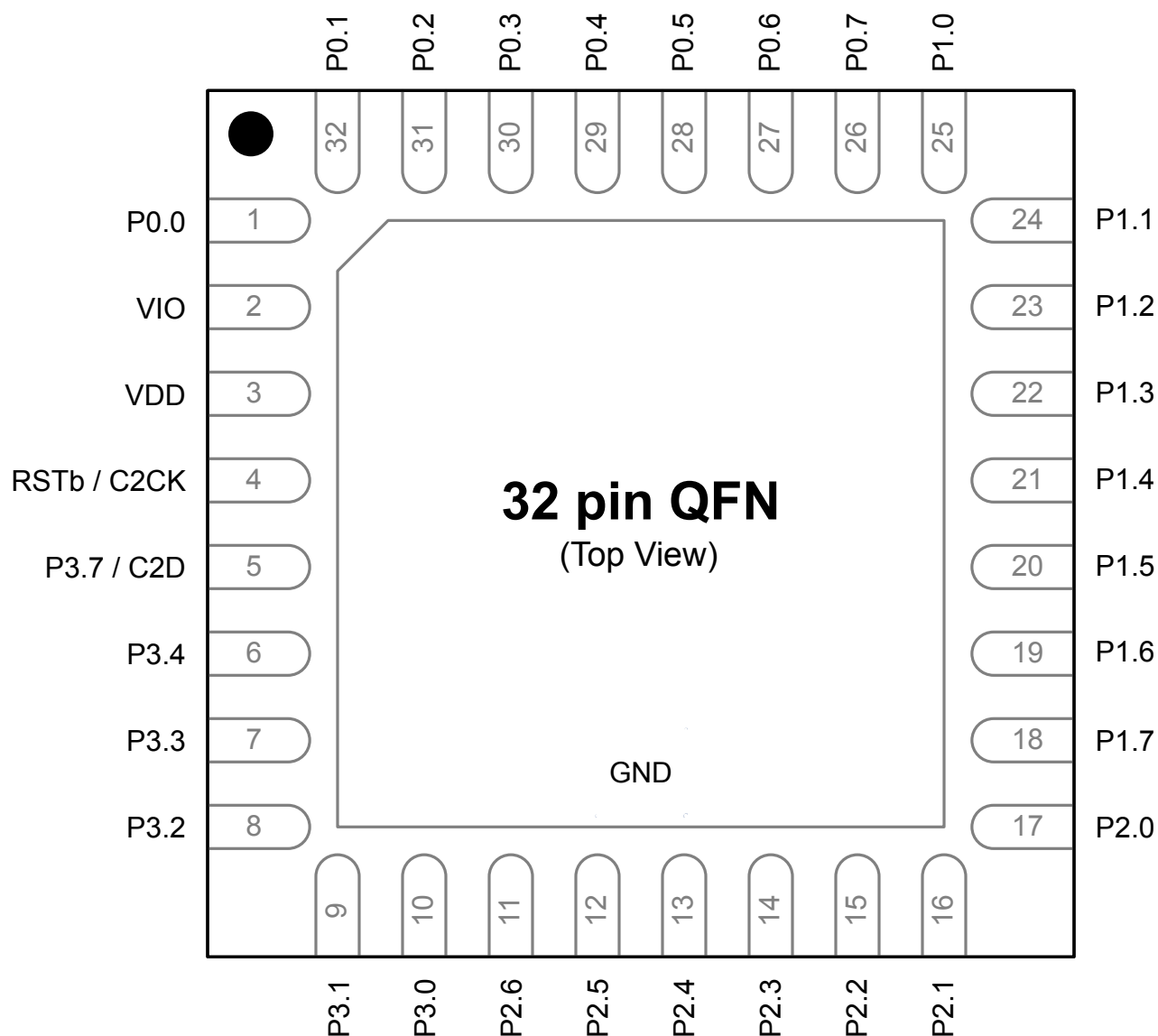


Figure 6.1. EFM8BB3x-QFN32 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

Dimension	Min	Typ	Max
Note: <ol style="list-style-type: none"> All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and Tolerancing per ANSI Y14.5M-1994. This drawing conforms to JEDEC Solid State Outline MO-220. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components. 			

Dimension	Min	Max
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm. 5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 7. The stencil thickness should be 0.125 mm (5 mils). 8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad. 10. A No-Clean, Type-3 solder paste is recommended. 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. 		

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

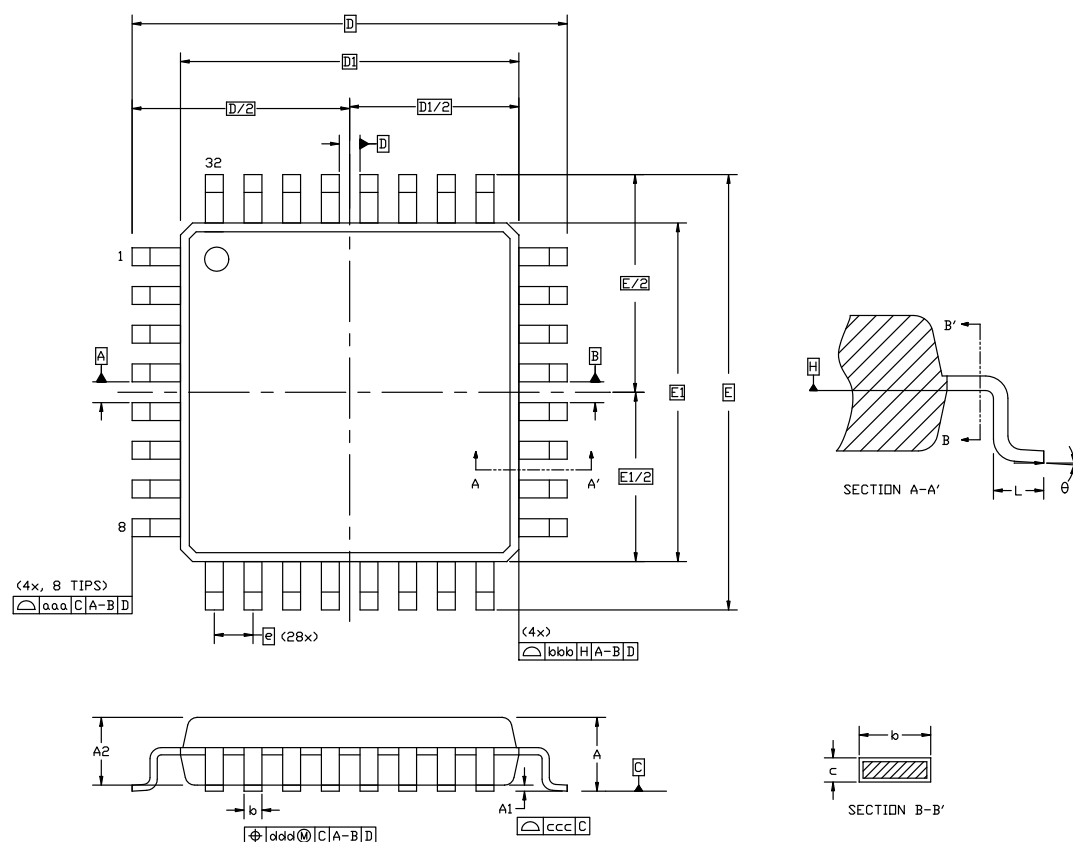


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.50	0.60	0.70

8.2 QFP32 PCB Land Pattern

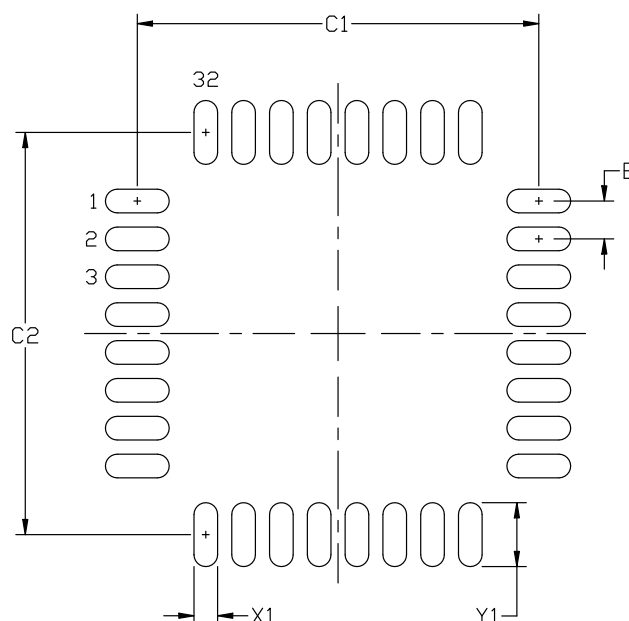


Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 QFP32 Package Marking

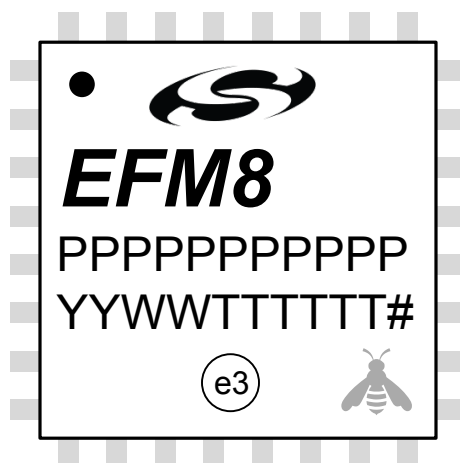


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.