

Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f32g-a-qfn24

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-A-QFN32	32	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-A-QFP32	32	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-A-QFN24	32	2304	20	2	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-A-QSOP24	32	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-A-QFN32	16	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-A-QFP32	16	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-A-QSOP24	16	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> Core halted All peripherals clocked and fully operational Code resumes execution on wake event 	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in normal bias mode for fast wake Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SUSPEND bit in PCON1 	<ul style="list-style-type: none"> Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Rising Edge CLUn Interrupt-Enabled Event
Stop	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on any reset source 	<ol style="list-style-type: none"> Clear STOPCF bit in REG0CN Set STOP bit in PCON0 	Any reset source
Snooze	<ul style="list-style-type: none"> Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in low bias current mode for energy savings Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SNOOZE bit in PCON1 	<ul style="list-style-type: none"> Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Rising Edge CLUn Interrupt-Enabled Event
Shutdown	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on pin or power-on reset 	<ol style="list-style-type: none"> Set STOPCF bit in REG0CN Set STOP bit in PCON0 	<ul style="list-style-type: none"> RSTb pin reset Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation
- Single-byte buffer on transmit and receive

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- Supports external clock frequencies up to 12 Mbps in master or slave mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparators (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Comparator Reference	I_{CPREF}		—	TBD	—	μA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	μA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate.
6. DAC supply current for each enabled DA and not including external load on pin.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to $V_{DD} > 2.2$ V	10	—	—	μs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} > V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	μs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	μs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{SYSCLK} > 1$ MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	μs

4.1.12 DACs

Table 4.12. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}		12			Bits
Throughput Rate	f_S		—	—	200	ksps
Integral Nonlinearity	INL		TBD	± 0.5	TBD	LSB
Differential Nonlinearity	DNL		TBD	± 5	TBD	LSB
Output Noise	$V_{\text{REF}} = 2.4 \text{ V}$ $f_S = 0.1 \text{ Hz to } 300 \text{ kHz}$		—	110	—	μV_{RMS}
Slew Rate	SLEW		—	± 1	—	V/ μs
Output Settling Time to 1 LSB	t_{SETTLE}	V_{OUT} change between 25% and 75% Full Scale	—	2.6	5	μs
Power-on Time	t_{PWR}		—	—	10	μs
Voltage Reference Range	V_{REF}		1.15	—	V_{DD}	V
Power Supply Rejection Ratio	PSRR	DC, $V_{\text{OUT}} = 50\%$ Full Scale	—	110	—	dB
		1 kHz, $V_{\text{OUT}} = 50\%$ Full Scale	—	60	—	dB
Total Harmonic Distortion	THD	$V_{\text{OUT}} = 10 \text{ kHz}$ sine wave, 10% to 90%	60	—	—	dB
Offset Error	E_{OFF}	$V_{\text{REF}} = 2.4 \text{ V}$	TBD	± 0.5	TBD	LSB
Offset Temperature Coefficient	TC_{OFF}		—	TBD	—	ppm/ $^{\circ}\text{C}$
Full-Scale Error	E_{FS}	$V_{\text{REF}} = 2.4 \text{ V}$	TBD	± 5	TBD	LSB
Full-Scale Error Tempco	TC_{FS}		—	TBD	—	ppm/ $^{\circ}\text{C}$
External Load Impedance	R_{LOAD}		2	—	—	k Ω
External Load Capacitance	C_{LOAD}		TBD	—	100	pF
Load Regulation		$V_{\text{OUT}} = 50\%$ Full Scale $I_{\text{OUT}} = -2 \text{ to } 2 \text{ mA}$	—	100	TBD	$\mu\text{V}/\text{mA}$

4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	μ s
		-100 mV Differential	—	3.5	—	μ s
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	$I_{OH} = -7 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -3.3 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.8 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (High Drive)	V_{OL}	$I_{OL} = 13.5 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 7 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 3.6 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output High Voltage (Low Drive)	V_{OH}	$I_{OH} = -4.75 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -2.25 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.2 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (Low Drive)	V_{OL}	$I_{OL} = 6.5 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 3.5 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 1.8 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Input High Voltage	V_{IH}		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage	V_{IL}		—	—	$0.3 \times V_{IO}$	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current ($V_{IN} = 0 \text{ V}$)	I_{PU}	$V_{DD} = 3.6$	-30	-20	-10	μA
Input Leakage (Pullups off or Analog)	I_{LK}	$\text{GND} < V_{IN} < V_{IO}$	TBD	—	TBD	μA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	$V_{IO} < V_{IN} < V_{IO} + 2.5 \text{ V}$ Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	μA

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

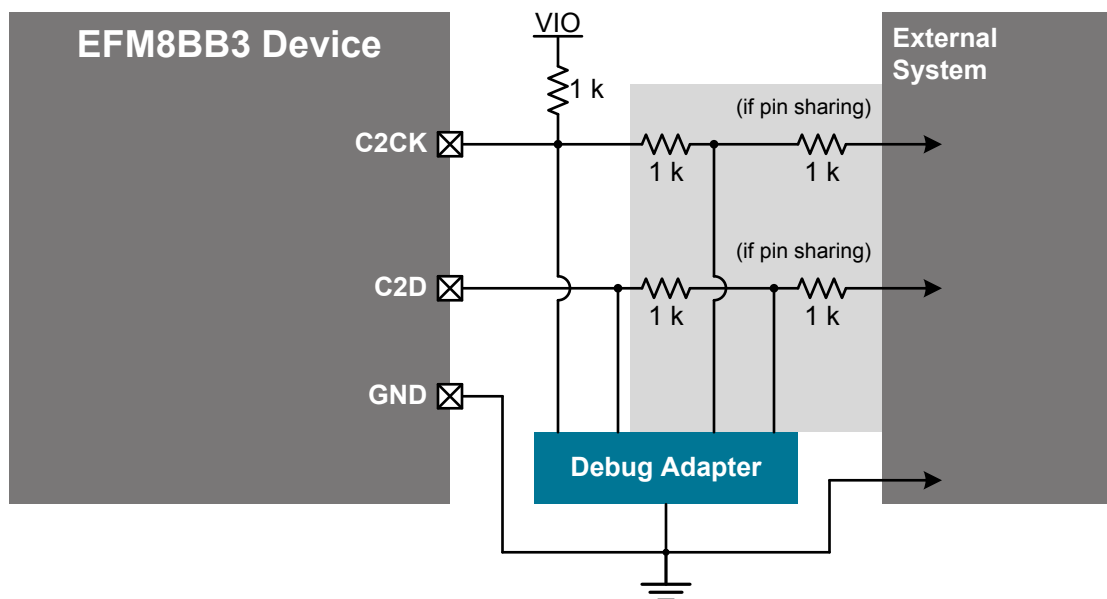


Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

6.2 EFM8BB3x-QFP32 Pin Definitions

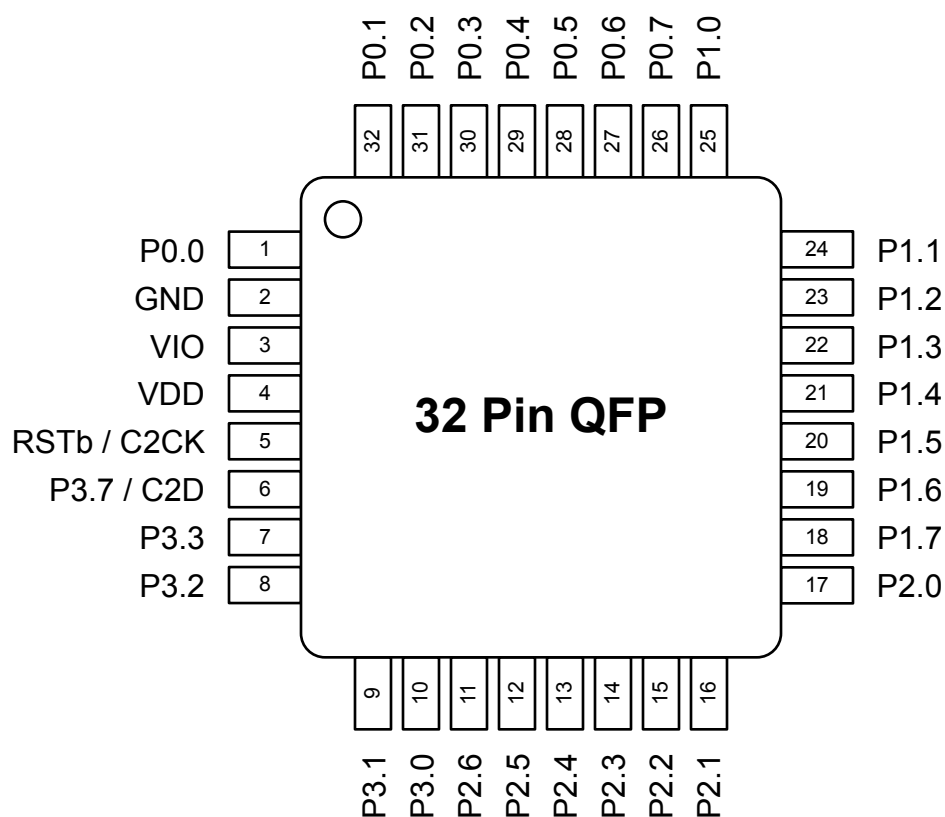


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

6.3 EFM8BB3x-QFN24 Pin Definitions

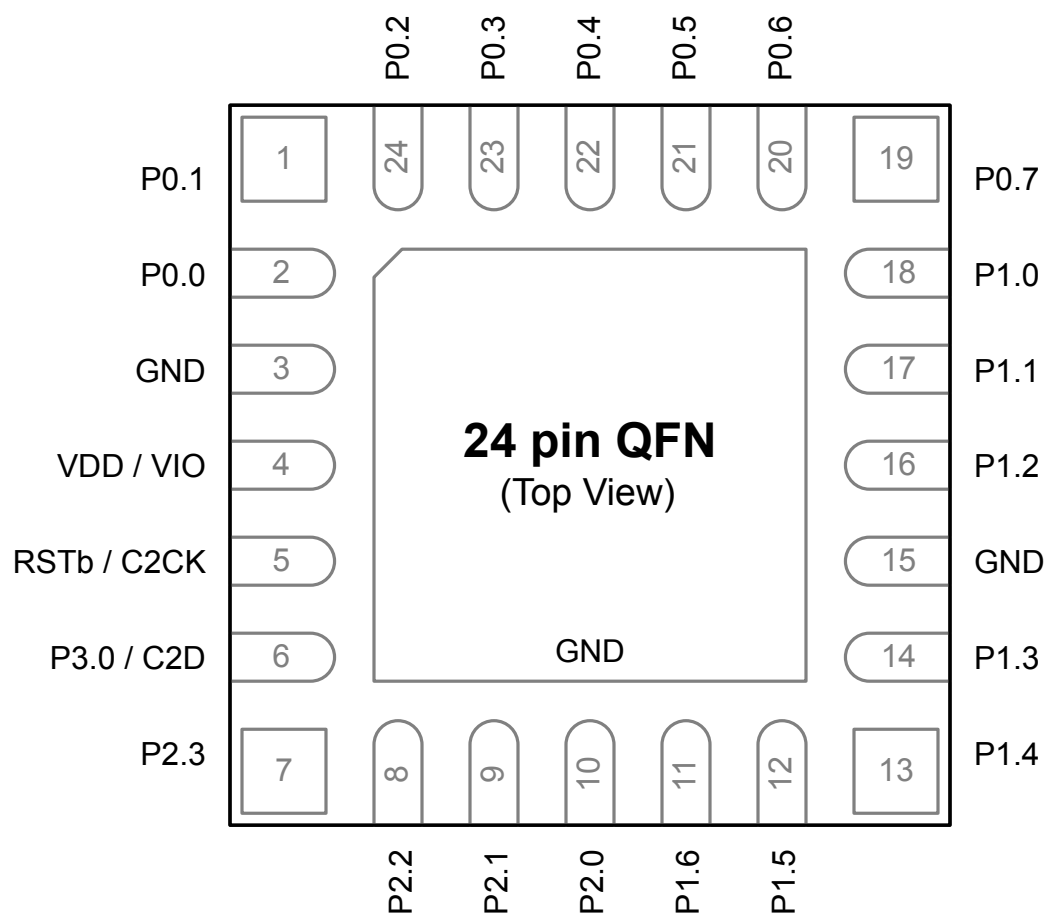


Figure 6.3. EFM8BB3x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9	ADC0.3 CMP0P.3 CMP0N.3
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

7.2 QFN32 PCB Land Pattern

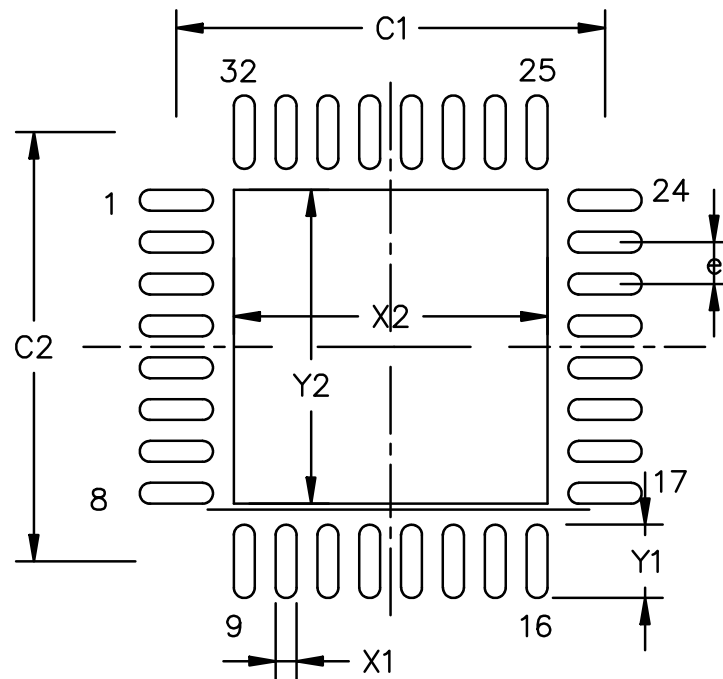


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	—	4.00
C2	—	4.00
X1	—	0.2
X2	—	2.8
Y1	—	0.75
Y2	—	2.8
e	—	0.4

8.2 QFP32 PCB Land Pattern

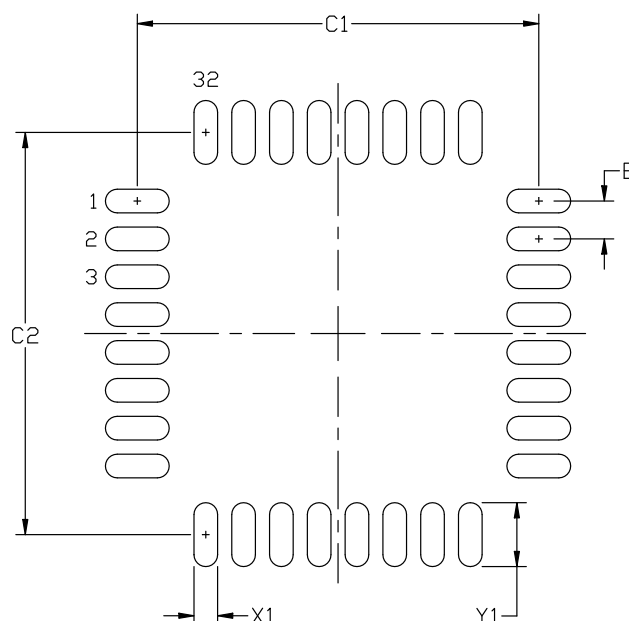


Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions

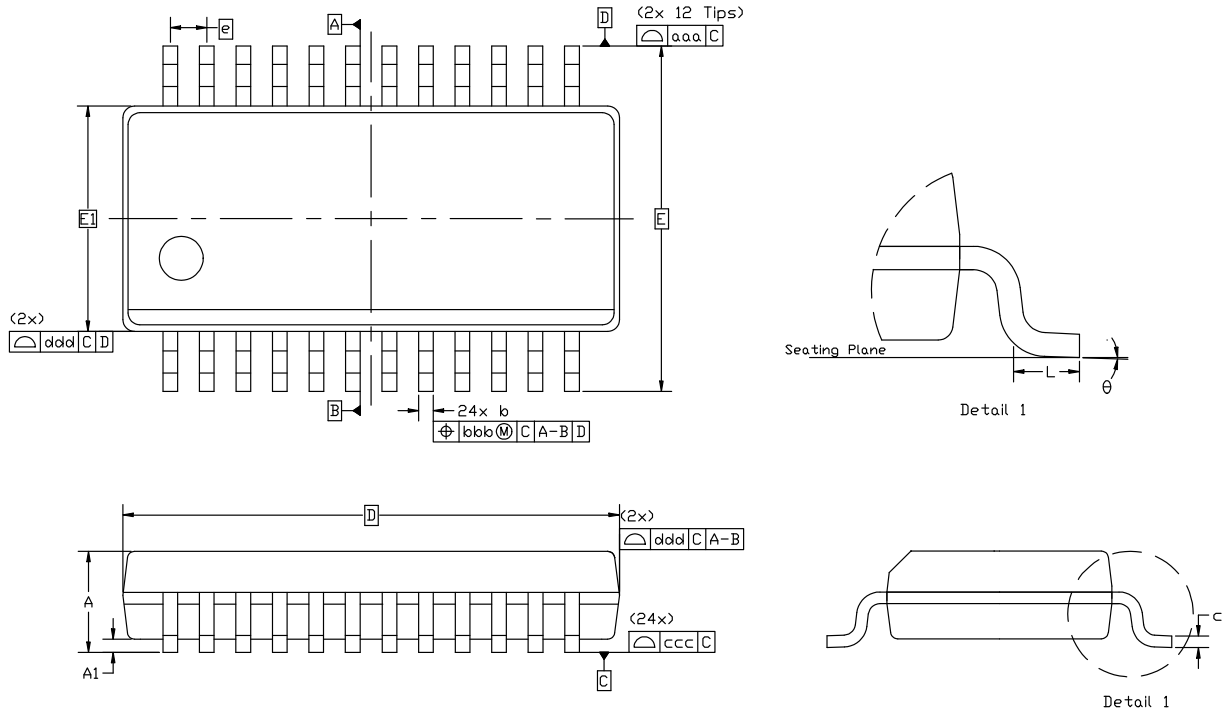


Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).