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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 13x10/12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f32g-a-qsop24

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-A-QFN32	32	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-A-QFP32	32	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-A-QFN24	32	2304	20	2	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-A-QSOP24	32	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-A-QFN32	16	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-A-QFP32	16	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-A-QSOP24	16	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

3.7 Analog

12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 400 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 13](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO ^{2, 3}	V _{IO}		TBD	—	V _{DD}	V
System Clock Frequency	f _{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T _A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{\text{REFFS}}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, T = 25 °C	TBD	1.2	TBD	V
		2.4 V Output, T = 25 °C	TBD	2.4	TBD	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	—	ms
		0.1 μF ceramic bypass on VREF pin	—	100	—	μs
Load Regulation	LR_{VREFP}	Load = 0 to 200 μA to GND	—	TBD	—	μV/μA
Load Capacitor	C_{VREFP}	Load = 0 to 200 μA to GND	0.1	—	—	μF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{\text{VREFP}}$		—	TBD	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	μA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	TBD	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	TBD	—	mV
Slope	M		—	TBD	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	TBD	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity			—	TBD	—	$^{\circ}\text{C}$
Turn-on Time			—	TBD	—	μs

Note:

1. Represents one standard deviation from the mean.

4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	μ s
		-100 mV Differential	—	3.5	—	μ s
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.10

6.2 EFM8BB3x-QFP32 Pin Definitions

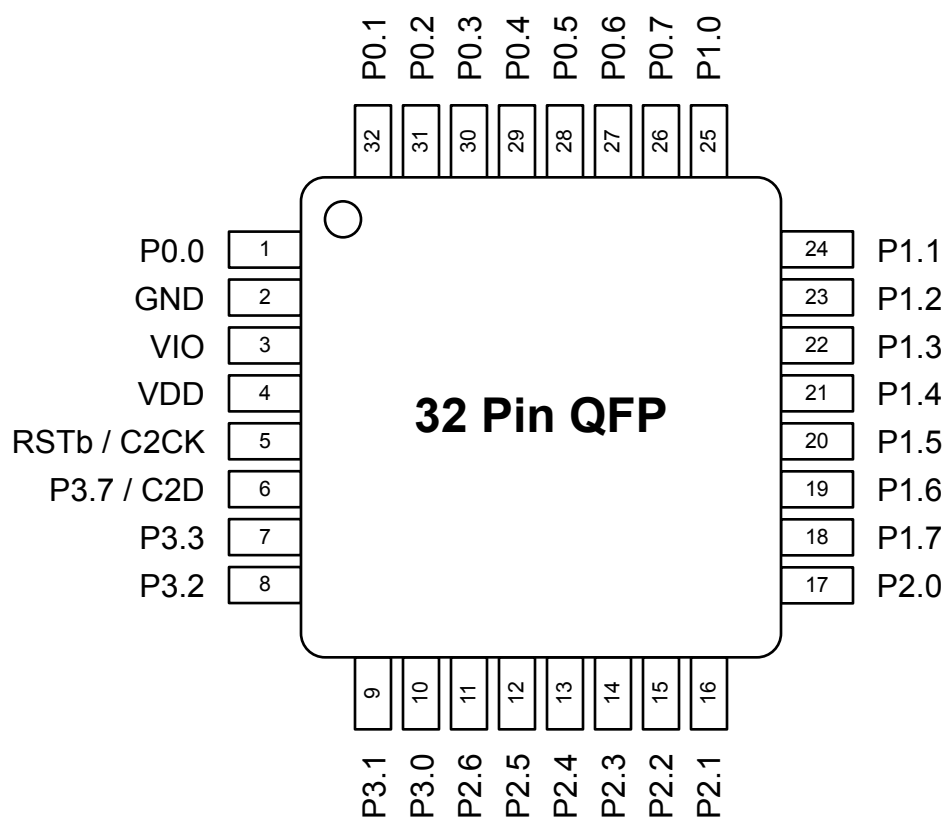


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.10 CMP1P.4 CMP1N.4
13	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.9 CMP1P.3 CMP1N.3
14	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8
17	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7
18	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9	ADC0.3 CMP0P.3 CMP0N.3
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

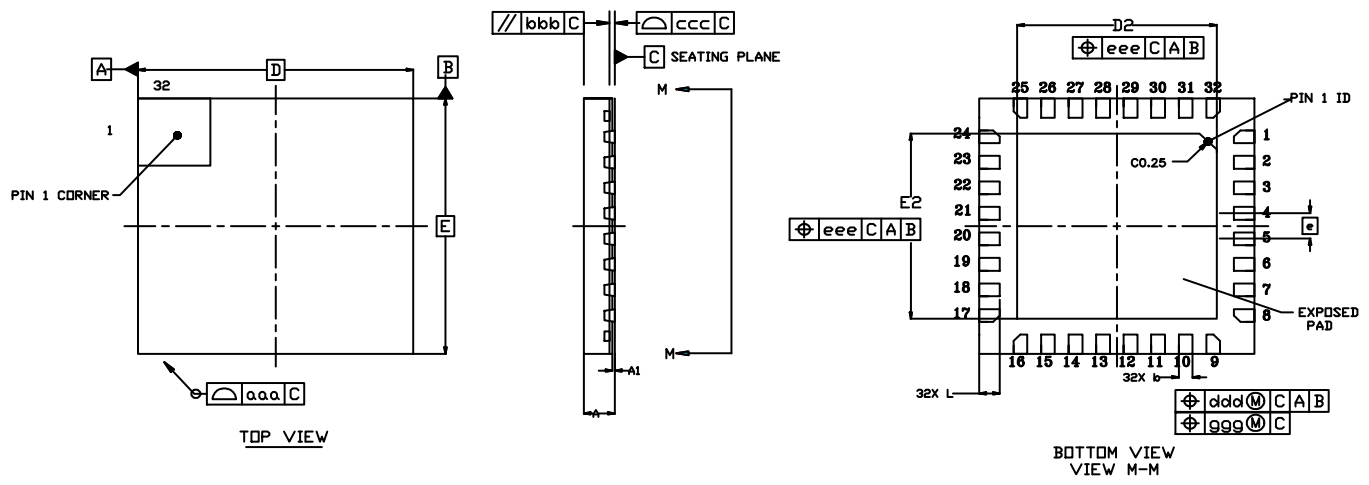


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

Dimension	Min	Typ	Max
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to JEDEC Solid State Outline MO-220. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components. 			

8.2 QFP32 PCB Land Pattern

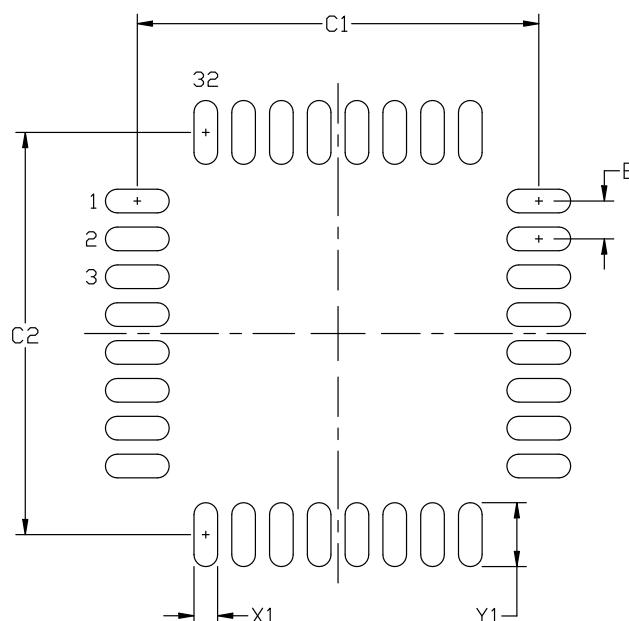


Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 QFP32 Package Marking

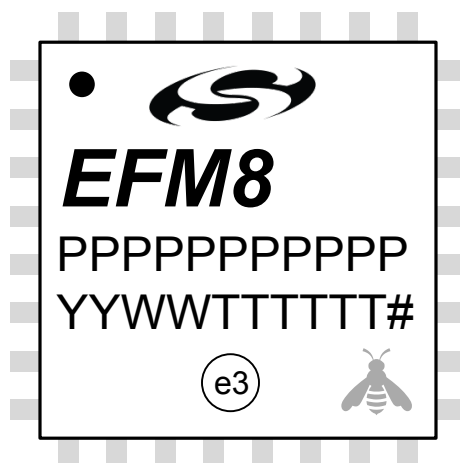


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Max
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-SM-782 guidelines. 4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 6. The stencil thickness should be 0.125 mm (5 mils). 7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 8. A 2 x 1 array of 1.20 mm x 0.95 mm openings on a 1.15 mm pitch should be used for the center pad. 9. A No-Clean, Type-3 solder paste is recommended. 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. 		

9.3 QFN24 Package Marking

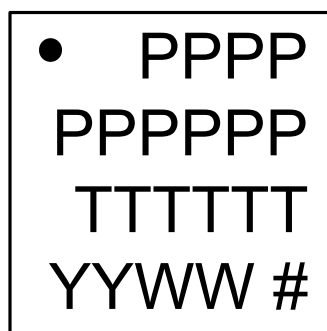


Figure 9.3. QFN24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10.2 QSOP24 PCB Land Pattern

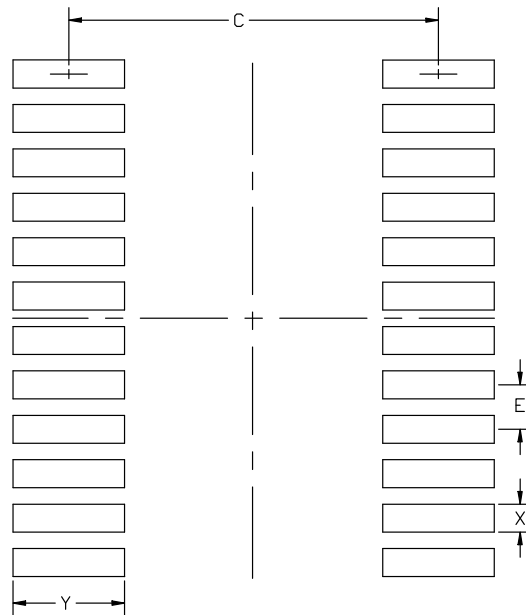


Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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