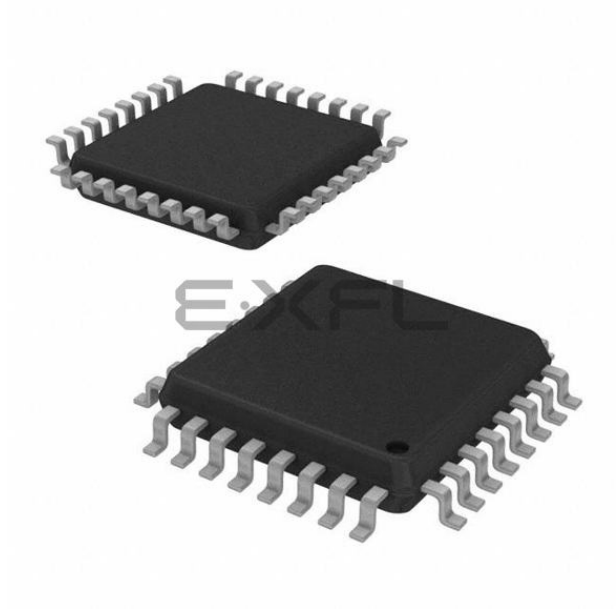

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-a-qfp32

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-A-QFN32	32	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-A-QFP32	32	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-A-QFN24	32	2304	20	2	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-A-QSOP24	32	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-A-QFN32	16	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-A-QFP32	16	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-A-QSOP24	16	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

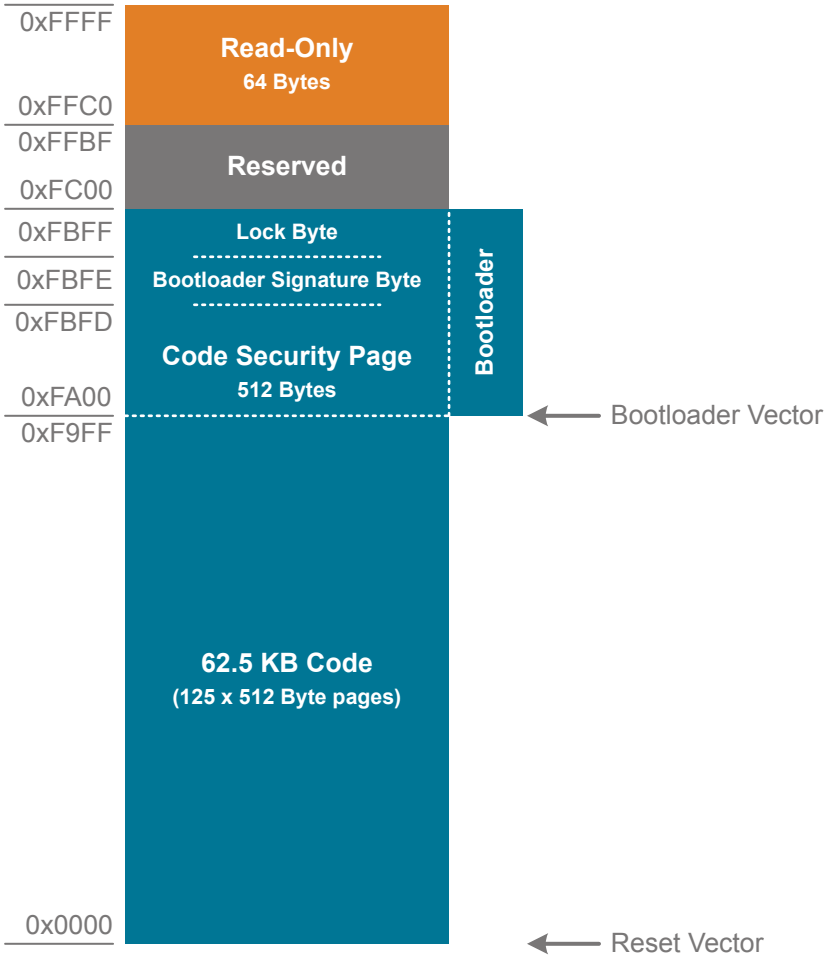

Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 13, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO[2, 3]	V_{IO}		TBD	—	V_{DD}	V
System Clock Frequency	f_{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 49 MHz[2]	—	TBD	TBD	mA
		F_{SYSCLK} = 24.5 MHz[2]	—	4.5	TBD	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	615	TBD	µA
		F_{SYSCLK} = 80 kHz[3]	—	155	TBD	µA
Idle Mode-Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 49 MHz[2]	—	TBD	TBD	mA
		F_{SYSCLK} = 24.5 MHz[2]	—	2.8	TBD	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	455	TBD	µA
		F_{SYSCLK} = 80 kHz[3]	—	145	TBD	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I_{DD}	LFO Running	—	125	TBD	µA
		LFO Stopped	—	120	TBD	µA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I_{DD}	LFO Running	—	26	TBD	µA
		LFO Stopped	—	21	TBD	µA
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I_{DD}		—	120	TBD	µA
Shutdown Mode—Core halted and all clocks stopped,Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	55	—	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 49 MHz, T_A = 25 °C	—	TBD	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	5	—	µA
ADC0[4]	I_{ADC}	TBD	—	TBD	TBD	µA
Internal ADC0 Reference[5]	I_{VREFFS}	Normal Power Mode	—	680	TBD	µA
		Low Power Mode	—	160	TBD	µA
On-chip Precision Reference	I_{VREFP}		—	75	—	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Digital-to-Analog Converters (DAC0, DAC1)[6]	I_{DAC}		—	125	—	µA

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1,2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1,2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming[3]	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUSPENDWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	12	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (49 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	48.25	49	49.75	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	TBD	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	TBD	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, T = 25 °C	TBD	1.2	TBD	V
		2.4 V Output, T = 25 °C	TBD	2.4	TBD	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	3	—	ms
		0.1 µF ceramic bypass on VREF pin	—	100	—	µs
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to GND	—	TBD	—	µV/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to GND	0.1	—	—	µF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	TBD	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V_{IN}		-0.25	—	V_{IO}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N_{bits}			6		bits
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t_{DLY}	Through single CLU	TBD	—	TBD	ns
Clocking Frequency	F_{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 3.6 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.2 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Input High Voltage	V_{IH}		0.7 x V_{IO}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.3 x V_{IO}	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	TBD	—	TBD	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.5 V Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	µA

4.2 Thermal Conditions

Table 4.16. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN24 Packages	—	TBD	—	°C/W
		QFN32 Packages	—	TBD	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.17 Absolute Maximum Ratings on page 27 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.17. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO[2]	V_{IO}		GND-0.3	V_{DD}+0.3	V
Voltage on I/O pins or RSTb, excluding P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V_{IN}	V_{IO} > TBD V	GND-0.3	TBD	V
		V_{IO} < TBD V	GND-0.3	TBD	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V_{IN}		GND-0.3	V_{DD}+0.3	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA

Note:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

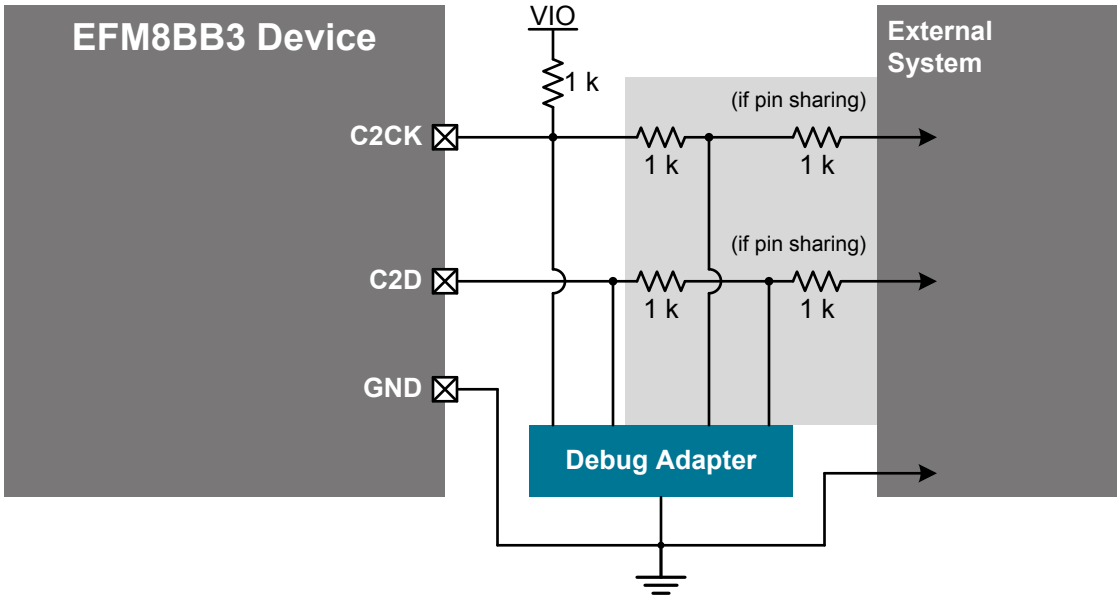

Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2

6.3 EFM8BB3x-QFN24 Pin Definitions

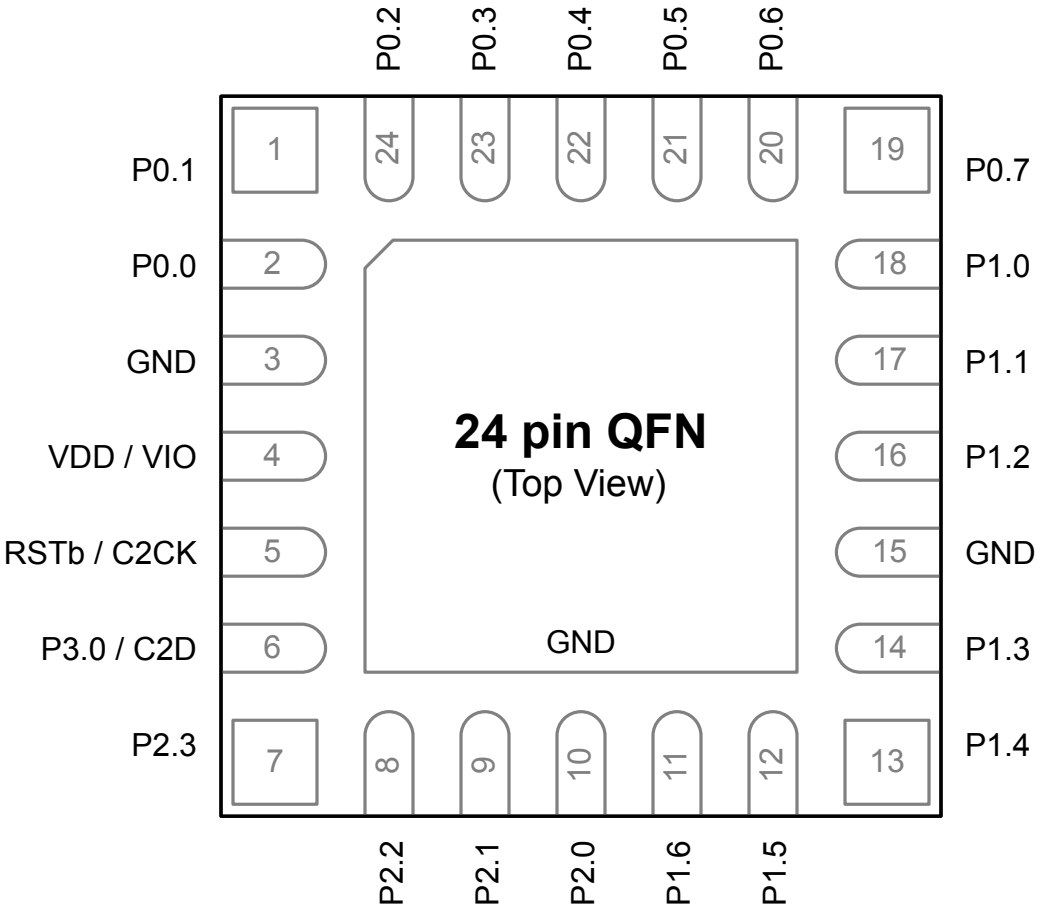

Figure 6.3. EFM8BB3x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

6.4 EFM8BB3x-QSOP24 Pin Definitions

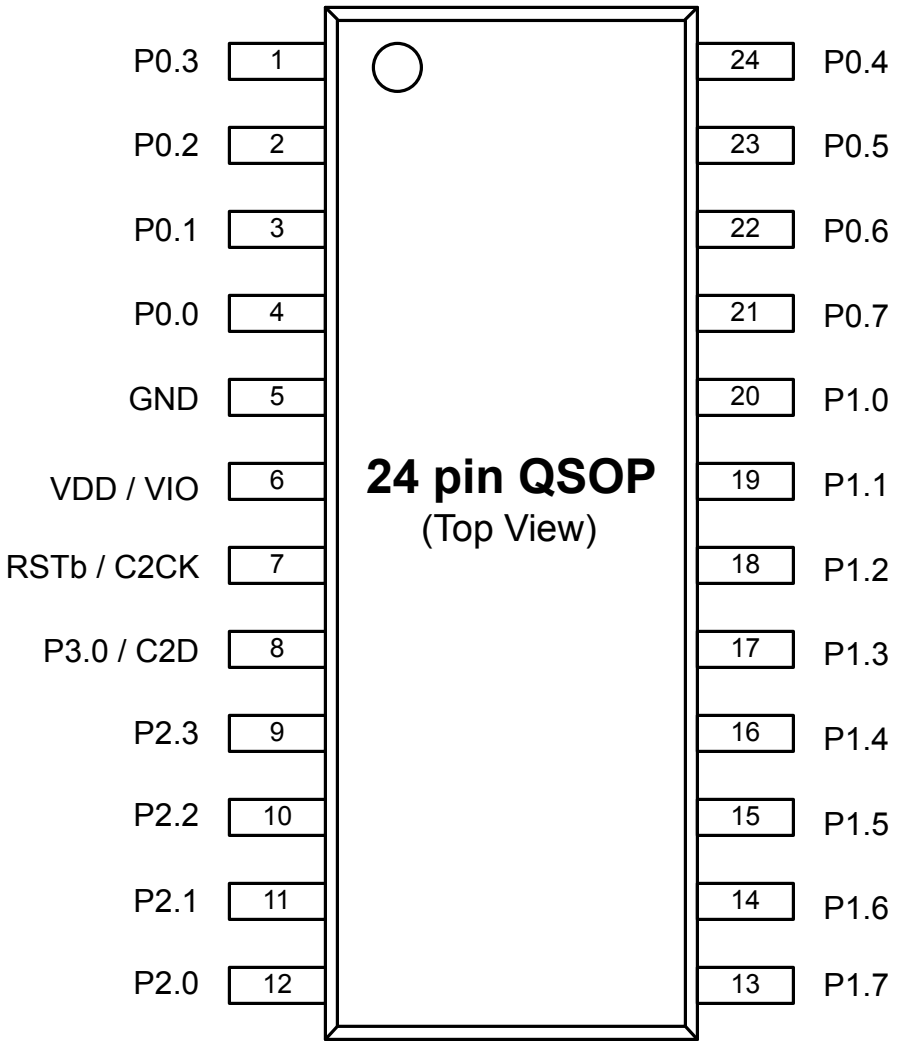

Figure 6.4. EFM8BB3x-QSOP24 Pinout

Table 6.4. Pin Definitions for EFM8BB3x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

11. Revision History

11.1 Revision 0.1

Initial release.

11.2 Revision 0.2

Added information on the bootloader to 3.10 Bootloader.

Updated some characterization TBD values.

Table of Contents