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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-QFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-a-qfp32r">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-a-qfp32r</a>

## 3.7 Analog

### 12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 400 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

### 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 13](#), unless stated otherwise.

#### 4.1.1 Recommended Operating Conditions

**Table 4.1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V <sub>DD</sub>		2.2	—	3.6	V
Operating Supply Voltage on VIO <sup>2,3</sup>	V <sub>IO</sub>		TBD	—	V <sub>DD</sub>	V
System Clock Frequency	f <sub>SYSCLK</sub>		0	—	50	MHz
Operating Ambient Temperature	T <sub>A</sub>		-40	—	85	°C

**Note:**

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

#### 4.1.6 Internal Oscillators

**Table 4.6. Internal Oscillators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	$f_{\text{HFOSC0}}$	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC0}}$	$T_A = 25^\circ\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC0}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	40	—	ppm/ $^\circ\text{C}$
High Frequency Oscillator 1 (49 MHz)						
Oscillator Frequency	$f_{\text{HFOSC1}}$	Full Temperature and Supply Range	48.25	49	49.75	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC1}}$	$T_A = 25^\circ\text{C}$	—	TBD	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC1}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	TBD	—	ppm/ $^\circ\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	$f_{\text{LFOSC}}$	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$\text{PSS}_{\text{LFOSC}}$	$T_A = 25^\circ\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{LFOSC}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	65	—	ppm/ $^\circ\text{C}$

#### 4.1.7 External Clock Input

**Table 4.7. External Clock Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	$f_{\text{CMOS}}$		0	—	50	MHz
External Input CMOS Clock High Time	$t_{\text{CMOSH}}$		9	—	—	ns
External Input CMOS Clock Low Time	$t_{\text{CMOSL}}$		9	—	—	ns

#### 4.1.11 Temperature Sensor

**Table 4.11. Temperature Sensor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	$V_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	TBD	—	mV
Offset Error <sup>1</sup>	$E_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	TBD	—	mV
Slope	M		—	TBD	—	mV/ $^{\circ}\text{C}$
Slope Error <sup>1</sup>	$E_M$		—	TBD	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity			—	TBD	—	$^{\circ}\text{C}$
Turn-on Time			—	TBD	—	$\mu\text{s}$

**Note:**

1. Represents one standard deviation from the mean.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS <sub>CP-</sub>	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V <sub>IN</sub>		-0.25	—	V <sub>IO</sub> +0.25	V
Input Pin Capacitance	C <sub>CP</sub>		—	7.5	—	pF
Internal Reference DAC Resolution	N <sub>bits</sub>		6			bits
Common-Mode Rejection Ratio	CMRR <sub>CP</sub>		—	70	—	dB
Power Supply Rejection Ratio	PSRR <sub>CP</sub>		—	72	—	dB
Input Offset Voltage	V <sub>OFF</sub>	T <sub>A</sub> = 25 °C	-10	0	10	mV
Input Offset Tempco	TC <sub>OFF</sub>		—	3.5	—	μV/°

#### 4.1.14 Configurable Logic

**Table 4.14. Configurable Logic**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t <sub>DLY</sub>	Through single CLU	TBD	—	TBD	ns
Clocking Frequency	F <sub>CLK</sub>	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

#### 4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	$V_{OH}$	$I_{OH} = -7 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -3.3 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.8 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (High Drive)	$V_{OL}$	$I_{OL} = 13.5 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 7 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 3.6 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output High Voltage (Low Drive)	$V_{OH}$	$I_{OH} = -4.75 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -2.25 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.2 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (Low Drive)	$V_{OL}$	$I_{OL} = 6.5 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 3.5 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 1.8 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Input High Voltage	$V_{IH}$		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage	$V_{IL}$		—	—	$0.3 \times V_{IO}$	V
Pin Capacitance	$C_{IO}$		—	7	—	pF
Weak Pull-Up Current ( $V_{IN} = 0 \text{ V}$ )	$I_{PU}$	$V_{DD} = 3.6$	-30	-20	-10	$\mu\text{A}$
Input Leakage (Pullups off or Analog)	$I_{LK}$	$\text{GND} < V_{IN} < V_{IO}$	TBD	—	TBD	$\mu\text{A}$
Input Leakage Current with $V_{IN}$ above $V_{IO}$	$I_{LK}$	$V_{IO} < V_{IN} < V_{IO} + 2.5 \text{ V}$ Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	$\mu\text{A}$

## 5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

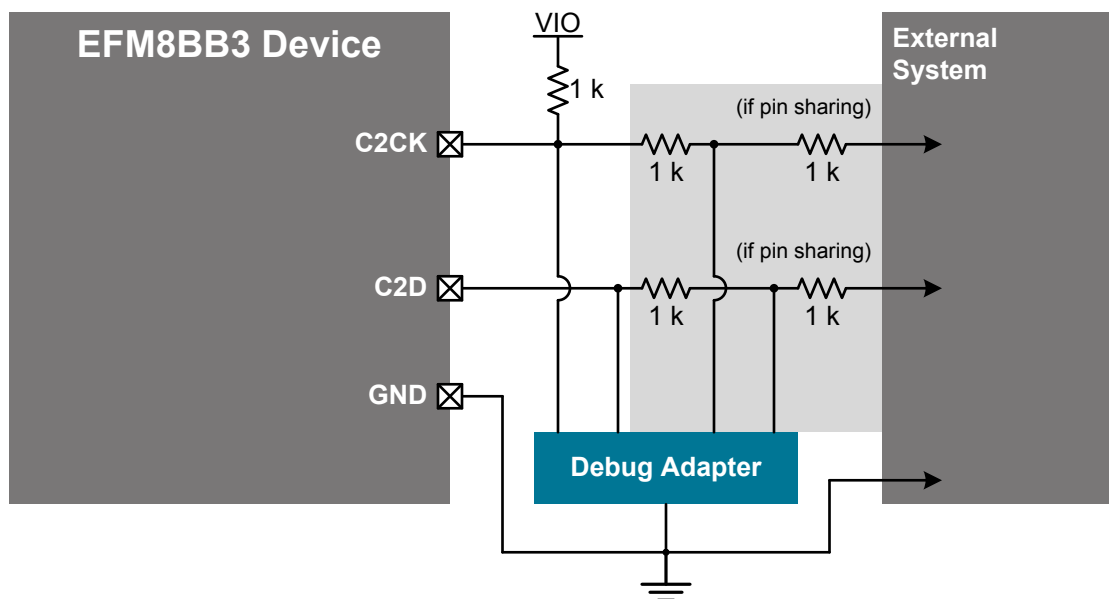


Figure 5.2. Debug Connection Diagram

## 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)).



## 6.2 EFM8BB3x-QFP32 Pin Definitions

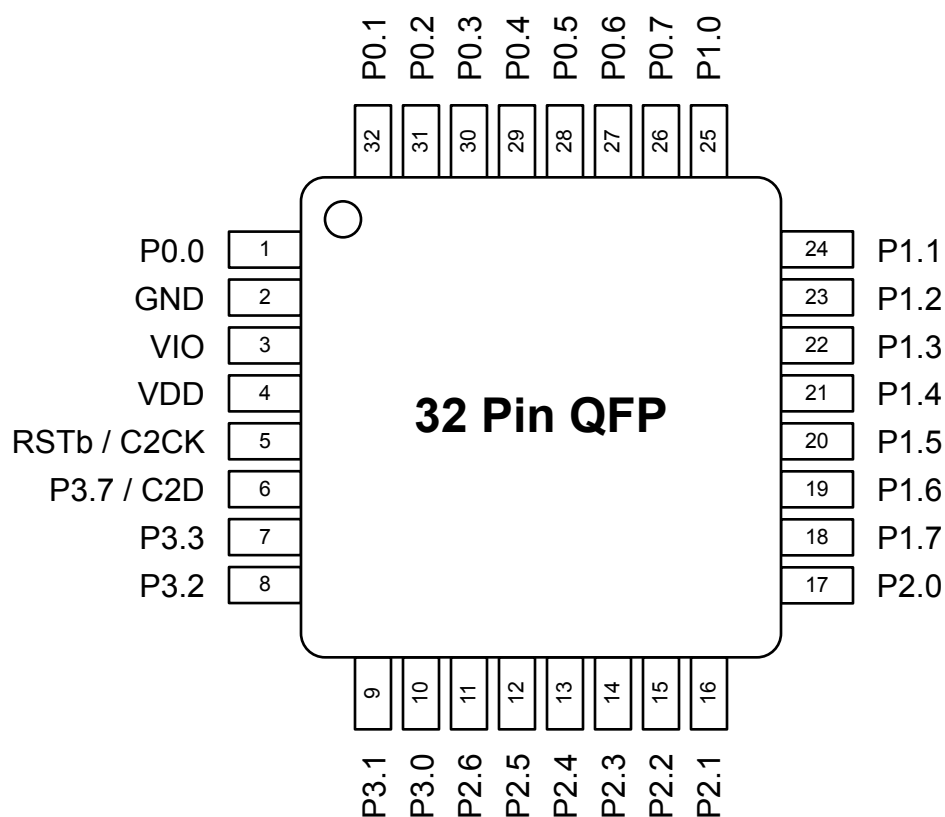


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.10 CMP1P.4 CMP1N.4
13	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.9 CMP1P.3 CMP1N.3
14	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8
17	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7
18	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2

Dimension	Min	Typ	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li> <li>3. This drawing conforms to JEDEC Solid State Outline MO-220.</li> <li>4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.</li> </ol>			

## 9. QFN24 Package Specifications

### 9.1 QFN24 Package Dimensions

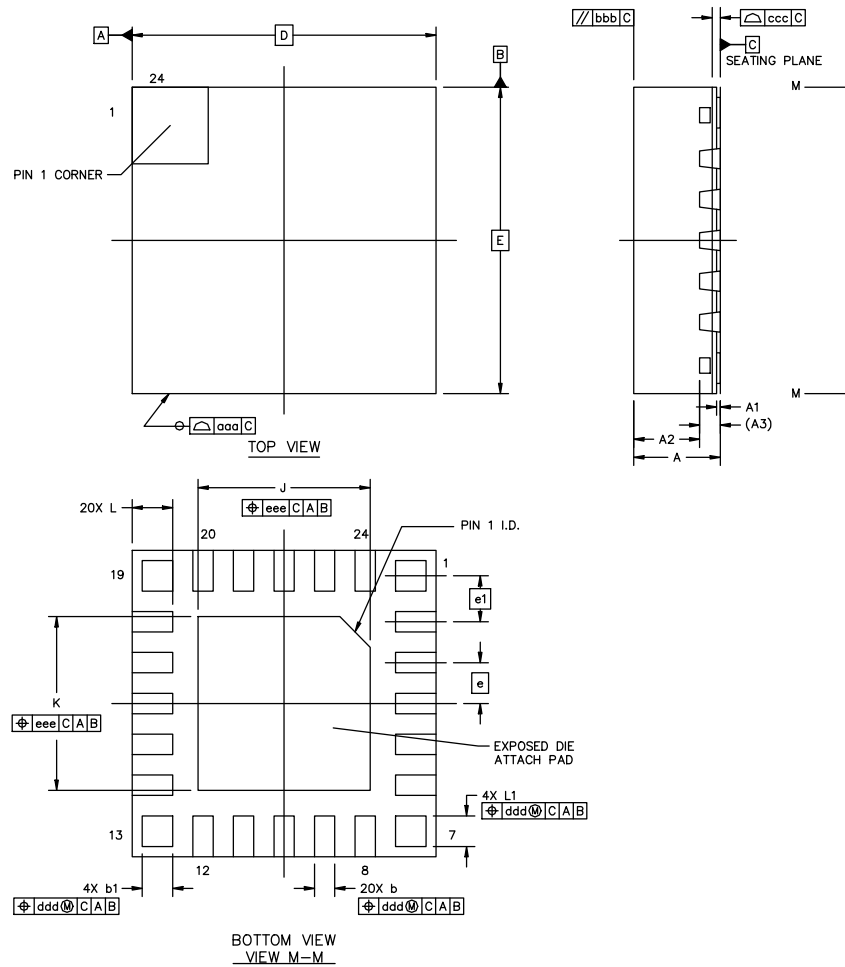


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		



Dimension	Min	Typ	Max
e	0.40 BSC		
e1	0.45 BSC		
J	1.60	1.70	1.80
K	1.60	1.70	1.80
L	0.35	0.40	0.45
L1	0.25	0.30	0.35
aaa	—	0.10	—
bbb	—	0.10	—
ccc	—	0.08	—
ddd	—	0.1	—
eee	—	0.1	—

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 9.2 QFN24 PCB Land Pattern

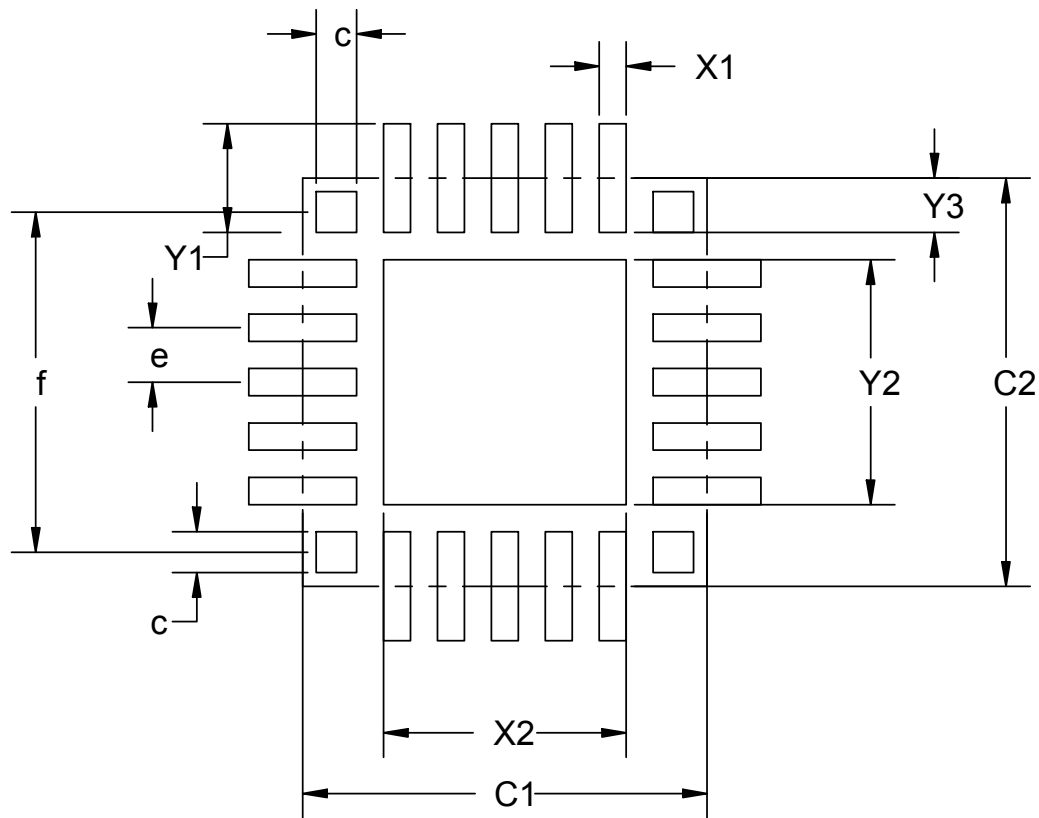
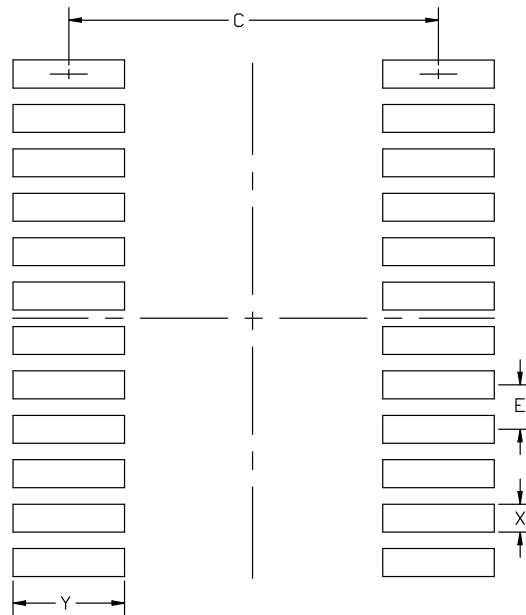


Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.00
C2		3.00
e		0.4 REF
X1		0.20
X2		1.80
Y1		0.80
Y2		1.80
Y3		0.4
f		2.50 REF
c	0.25	0.35

## 10.2 QSOP24 PCB Land Pattern



**Figure 10.2. QSOP24 PCB Land Pattern Drawing**

**Table 10.2. QSOP24 PCB Land Pattern Dimensions**

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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