# E·XFL



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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

## Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	50MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 13x10/12b SAR; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb31f64g-a-qsop24r

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## 2. Ordering Information



## Figure 2.1. EFM8BB3 Part Numbering

All EFM8BB3 family members have the following features:

- · CIP-51 Core running up to 49 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- · 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- · Six 16-bit Timers
- Four Configurable Logic Units
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and directto-XRAM data transfer
- Two Voltage Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- 16-bit CRC Unit
- · AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8BB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

l able 2.1.	Product Selection Guide	

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F64G-A-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F64G-A-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +85 °C	QFN24

## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- · 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- · Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- · LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- · External pin capture
- · LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- · Programmable timeout interval
- · Runs from the low-frequency oscillator
- · Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

## Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- · Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- · Automatic start and stop generation
- · Single-byte buffer on transmit and receive

#### I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- · Support for slave mode only
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave address recognition
- · Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

#### 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- · Byte-level bit reversal
- · Automatic CRC of flash contents on one or more 256-byte blocks
- · Initial seed selection of 0x0000 or 0xFFFF

## Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- · Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- · Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- · Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- · Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- · Asynchronous output may be used to wake from low-power states

## Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- · Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- · Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- · Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - · Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- · Programmable response time
- · Interrupts generated on rising, falling, or both edges
- · PWM output kill feature

## 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- · Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- · External reset pin
- · Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- · Watchdog timer reset
- · Missing clock detector reset
- Flash error reset

## 3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

## 4.1.8 Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Crystal Frequency	f <sub>XTAL</sub>		0.02	_	25	MHz
Crystal Drive Current	I <sub>XTAL</sub>	XFCN = 0	—	0.5	—	μA
		XFCN = 1	_	1.5	_	μA
		XFCN = 2	—	4.8	_	μA
		XFCN = 3	—	14	_	μA
		XFCN = 4	_	40	_	μA
		XFCN = 5	_	120	_	μA
		XFCN = 6	_	550	_	μA
		XFCN = 7		2.6		mA

## Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit			
Offset Temperature Coefficient	TC <sub>OFF</sub>		_	TBD	-	LSB/°C			
Slope Error	E <sub>M</sub>	12 Bit Mode	_	TBD	TBD	%			
		10 Bit Mode	_	TBD	_	%			
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin									
Signal-to-Noise	SNR	12 Bit Mode	_	TBD	_	dB			
		10 Bit Mode	_	TBD	_	dB			
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	TBD	TBD	_	dB			
		10 Bit Mode	_	TBD	_	dB			
Total Harmonic Distortion (Up to	THD	12 Bit Mode	—	TBD	_	dB			
5th Harmonic)		10 Bit Mode	_	TBD	_	dB			
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	TBD	-	dB			
		10 Bit Mode	_	TBD	_	dB			

## Note:

1. Conversion Time does not include Tracking Time. Total Conversion Time is:

Total Conversion Time = [RPT × (ADTK + NUMBITS + 1) × T(SARCLK)] + (T(ADCCLK) × 4)

where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC.

2. Absolute input pin voltage is limited by the  $V_{\text{IO}}$  supply.

## 4.1.11 Temperature Sensor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit	
Offset	V <sub>OFF</sub>	T <sub>A</sub> = 0 °C	_	TBD	_	mV	
Offset Error <sup>1</sup>	E <sub>OFF</sub>	T <sub>A</sub> = 0 °C	_	TBD	_	mV	
Slope	М		—	TBD	_	mV/°C	
Slope Error <sup>1</sup>	E <sub>M</sub>			TBD	_	μV/°C	
Linearity			—	TBD	—	°C	
Turn-on Time			—	TBD	_	μs	
Note: 1. Represents one standard deviation from the mean.							

## 4.1.13 Comparators

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Response Time, CPMD = 00	t <sub>RESP0</sub>	+100 mV Differential		100	_	ns
(Highest Speed)		-100 mV Differential	_	150	_	ns
Response Time, CPMD = 11 (Low-	t <sub>RESP3</sub>	+100 mV Differential		1.5	_	μs
est Power)		-100 mV Differential		3.5		μs
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00		0.4	_	mV
Mode 0 (CPMD = 00)		CPHYP = 01		8		mV
		CPHYP = 10		16		mV
		CPHYP = 11		32	_	mV
Negative Hysteresis	HYS <sub>CP-</sub>	CPHYN = 00		-0.4		mV
Mode 0 (CPMD = 00)		CPHYN = 01		-8	_	mV
		CPHYN = 10		-16	_	mV
		CPHYN = 11		-32	_	mV
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00		0.5	_	mV
Mode 1 (CPMD = 01)		CPHYP = 01		6	_	mV
		CPHYP = 10	_	12	_	mV
		CPHYP = 11	_	24	_	mV
Negative Hysteresis	HYS <sub>CP-</sub>	CPHYN = 00	_	-0.5	_	mV
Mode 1 (CPMD = 01)		CPHYN = 01	_	-6	_	mV
		CPHYN = 10	_	-12	_	mV
		CPHYN = 11	_	-24	_	mV
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00	_	0.7	_	mV
Mode 2 (CPMD = 10)		CPHYP = 01	_	4.5	_	mV
		CPHYP = 10	_	9	_	mV
		CPHYP = 11	_	18	_	mV
Negative Hysteresis	HYS <sub>CP-</sub>	CPHYN = 00	_	-0.6	_	mV
Mode 2 (CPMD = 10)		CPHYN = 01	_	-4.5	_	mV
		CPHYN = 10	_	-9	_	mV
		CPHYN = 11		-18	_	mV
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00	_	1.5	_	mV
Mode 3 (CPMD = 11)		CPHYP = 01	_	4	_	mV
		CPHYP = 10	_	8	_	mV
		CPHYP = 11		16	_	mV

## Table 4.13. Comparators

## 6. Pin Definitions

## 6.1 EFM8BB3x-QFN32 Pin Definitions



Figure 6.1. EFM8BB3x-QFN32 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
28	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
29	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
30	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.10	
				CLU3A.9	
31	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
32	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	
Center	GND	Ground			



Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2.	Pin Definitions	for EFM8BB3x-QFP32
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Pin	Pin Name	Description	Crossbar Capability	Additional Digital	Analog Functions
Number				Functions	
1	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb /	Active-low Reset /			
	С2СК	C2 Debug Clock			

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
6	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	
15	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.15
				CLU2OUT	CMP1P.4
				CLU1A.15	CMP1N.4
				CLU2B.14	
				CLU3A.14	
16	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.14
				I2C0 SCL	CMP1P.3
				 CLU1B.14	CMP1N.3
				CLU2A.15	
				CI U3B.15	
17	P2.0	Multifunction I/O	Yes	P2MAT.0	CMP1P.2
				12C0 SDA	CMP1N.2
				ULU3B.14	

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1 5	Multifunction I/O	Yes	P1MAT 5	
	1 1.0				CMP1P 4
					CMP1N 4
				CLU1A 13	
				CLU2B.13	
				CLU3B.11	
13	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
				CLU3B.10	
14	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	
				CLU1A.11	
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
17	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.12	
18	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
20	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
21	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
22	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
23	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.10	
				CLU3A.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	

#### 8.2 QFP32 PCB Land Pattern



Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2.	QFP32 PCB	Land Pattern	Dimensions
------------	-----------	--------------	------------

Dimension	Min	Мах	
C1	8.40	8.50	
C2	8.40	8.50	
E	0.80 BSC		
X1	0.55		
Y1	1.5		

#### Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

## 9. QFN24 Package Specifications

## 9.1 QFN24 Package Dimensions



Figure 9.1. QFN24 Package Drawing

Dimension	Min	Тур	Мах	
A	0.8 0.85		0.9	
A1	0.00	—	0.05	
A2	—	0.65	—	
A3	0.203 REF			
b	0.15	0.2	0.25	
b1	0.25	0.3	0.35	
D	3.00 BSC			
E	3.00 BSC			

Dimension	Min	Тур	Мах
е		0.40 BSC	
e1	0.45 BSC		
J	1.60	1.70	1.80
К	1.60	1.70	1.80
L	0.35	0.40	0.45
L1	0.25	0.30	0.35
ааа	_	0.10	—
bbb	—	0.10	—
ссс	_	0.08	—
ddd	_	0.1	_
eee	_	0.1	—

## Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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