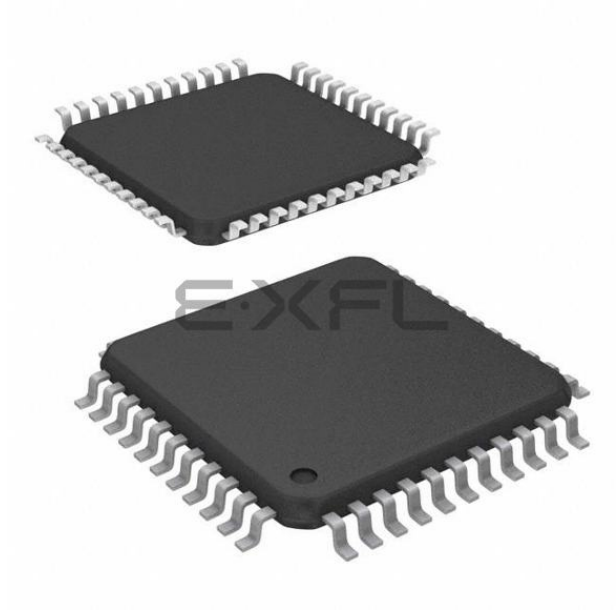
Analog Devices Inc./Maxim Integrated - DS89C420-ECS Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c420-ecs

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C)* (Figure 1, Figure 2, and Figure 3)

PARAMETER		SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
System Clock (Note 1)	External Oscillator (25MHz, 33MHz)	1 / t_{CLCL}	0	25	0	25	0	25	0	25	0	25	MHz
			0	33	0	33	0	33	0	33	0	33	
	External Crystal (25MHz, 33MHz)		1	25	1	25	1	25	1	25	1	25	
			1	33	1	33	1	33	1	33	1	33	
ALE Pulse Width (Note 2)		t_{LHLL}	$0.5t_{CLCL}$ - 2 + t_{STC3}		t_{CLCL} - 2 + t_{STC3}		$2t_{CLCL}$ - 4 + t_{STC3}		$1.5t_{CLCL}$ - 5 + t_{STC3}		$1.5t_{CLCL}$ - 5 + t_{STC3}		ns
Port 0 Instruction Address Valid to ALE Low		t_{AVLL}							t_{CLCL} - 2		$0.5t_{CLCL}$ - 2		ns
Port 2 Instruction Address Valid to ALE Low		t_{AVLL2}	$0.5t_{CLCL}$ - 4		$0.5t_{CLCL}$ - 4		$1.5t_{CLCL}$ - 5		$0.5t_{CLCL}$ - 2		t_{CLCL} - 2		ns
Port 0 Data AddressValid to ALE Low		t_{AVLL3}							t_{CLCL} - 2 + t_{STC3}		$0.5t_{CLCL}$ - 2 + t_{STC3}		ns
Program Address Hold After ALE Low		t_{LLAX}	$0.5t_{CLCL}$ - 8		$1.5t_{CLCL}$ - 8		$2.5t_{CLCL}$ - 8		$0.5t_{CLCL}$ - 8		$0.5t_{CLCL}$ - 8		ns
Address Hold After ALE Low MOVX Write		t_{LLAX2}	$0.5t_{CLCL}$ - 8 + t_{STC4}		$1.5t_{CLCL}$ - 8 + t_{STC4}		$2.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		ns
Address Hold After ALE Low MOVX Read		t_{LLAX3}	$0.5t_{CLCL}$ - 8 + t_{STC4}		$1.5t_{CLCL}$ - 8 + t_{STC4}		$2.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		ns
ALE Low to Valid Instruction In		t_{LLIV}								$2.5t_{CLCL}$ - 20		$2.5t_{CLCL}$ - 20	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}							$1.5t_{CLCL}$ - 6		$0.5t_{CLCL}$ - 6		ns
$\overline{PSEN}$ Pulse Width for Program Fetch		t_{PLPH}	t_{CLCL} - 5		t_{CLCL} - 5		$2t_{CLCL}$ - 5		t_{CLCL} - 5		$2t_{CLCL}$ - 5		ns

PARAMETER	SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		t_{CLCL} - 18		t_{CLCL} - 18		$2t_{CLCL}$ - 18		t_{CLCL} - 18		$2t_{CLCL}$ - 18	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		0		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}								$1.5t_{CLCL}$ - 20		$3t_{CLCL}$ - 20	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}		t_{CLCL} - 18		$1.5t_{CLCL}$ - 18		$2.5t_{CLCL}$ - 18		$3t_{CLCL}$ - 20		$3.5t_{CLCL}$ - 20	ns
$\overline{PSEN}$ Low to Port 0 Address Float	t_{PLAZ}								0		0	ns
$\overline{RD}$ Pulse Width (P3.7) (Note 2)	t_{RLRH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{WR}$ Pulse Width (P3.6) (Note 2)	t_{WLWH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{RD}$ (P3.7) Low to Valid Data In (Note 2)	t_{RLDV}		t_{CLCL} - 15 + t_{STC1}		t_{CLCL} - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}	ns
Data Hold After $\overline{RD}$ (P3.7)	t_{RHDX}	0		0		0		0		0		ns
Data Float After $\overline{RD}$ (P3.7)	t_{RHDZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
MOVX ALE Low to Input Data Valid (Note 2)	t_{LLDV}								$2.5t_{CLCL}$ - 20 + t_{STC1}		$2.5t_{CLCL}$ - 20 + t_{STC1}	ns
Port 0 Address to Valid Data In (Note 2)	t_{AVDV0}								$3t_{CLCL}$ - 20 + t_{STC1}		$3t_{CLCL}$ - 20 + t_{STC1}	ns

Figure 2. Page-Mode 1 Timing

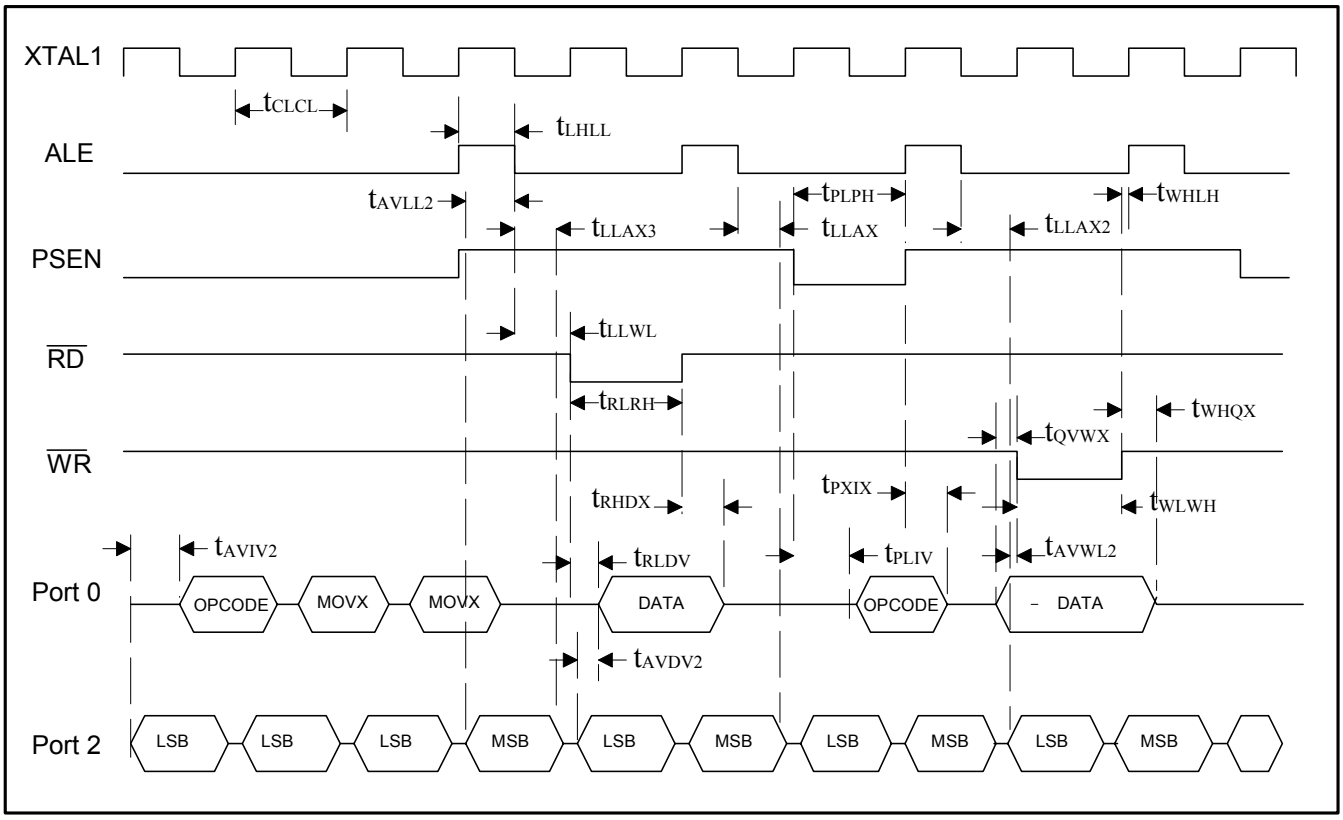
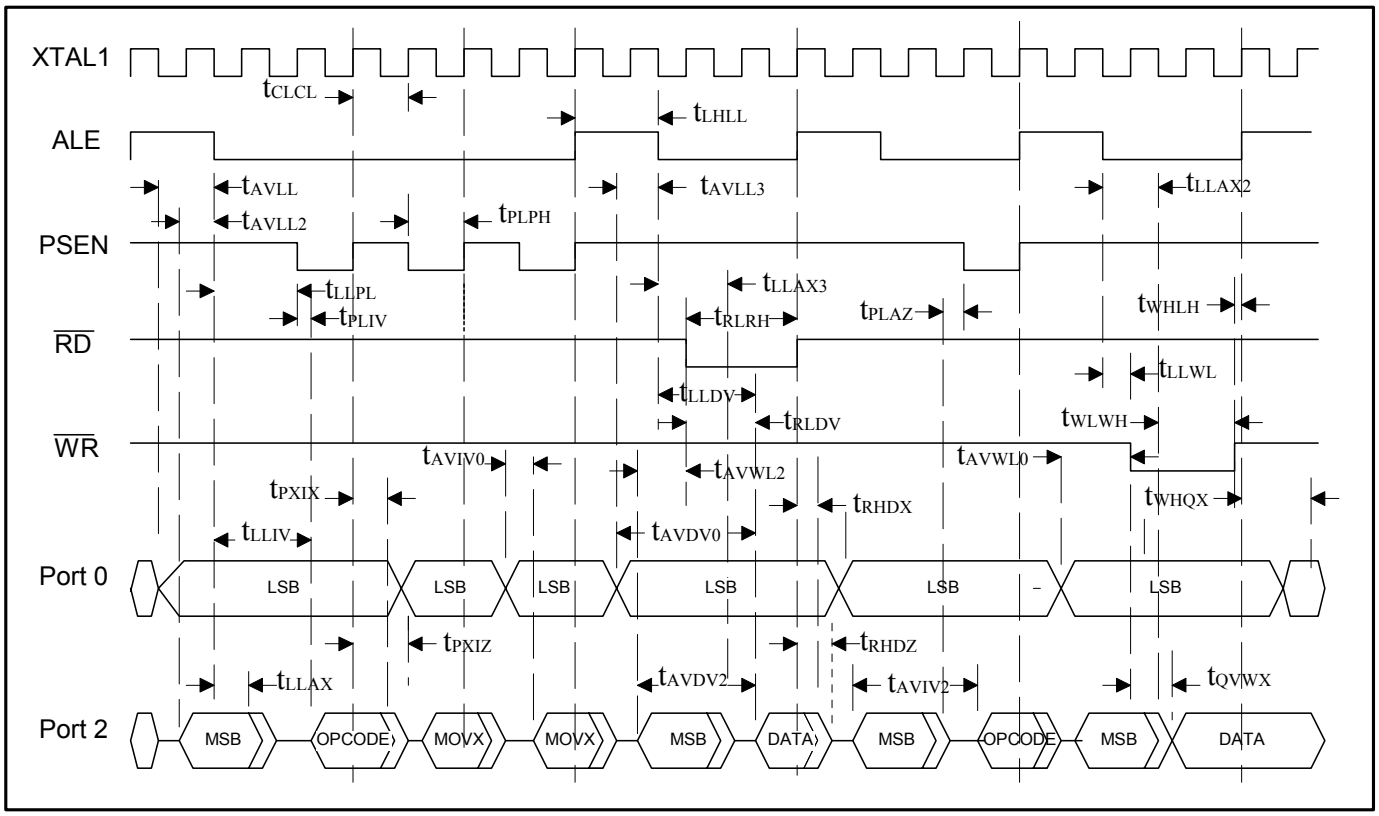


Figure 3. Page-Mode 2 Timing



EXTERNAL CLOCK CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)*

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)* (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	

Note: SM2 is the serial port 0, mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial-port clock cycle.

**Specifications to -40°C are guaranteed by design and not production tested.*

POWER CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Startup Time	t_{CSU}	(Note 2)		8		ms
Power-On Reset Delay	t_{POR}	(Note 3)		65,536		t_{CLCL}

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: Startup time for a crystal varies with load capacitance and manufacturer. Time shown is for a 11.0592MHz crystal manufactured by Fox Electronics.
Note 3: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = +21°C to +27°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	1 / t_{CLCL}		4		6	MHz
Address Setup to $\overline{PROG}$ Low	t_{AVGL}		$48t_{CLCL}$			
Address Hold After $\overline{PROG}$	t_{GHAX}		$48t_{CLCL}$			
Data Setup to $\overline{PROG}$ Low	t_{DVGL}		$48t_{CLCL}$			
Data Hold After $\overline{PROG}$	t_{GHDX}		$48t_{CLCL}$			
$\overline{PROG}$ Pulse Width	t_{GLGH}		85		100	µs
Address to Data Valid	t_{AVQV}				$48t_{CLCL}$	
Enable Low to Data Valid	t_{ELQV}				$48t_{CLCL}$	
Data Float After Enable	t_{EHQZ}		0		$48t_{CLCL}$	
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}		10			µs

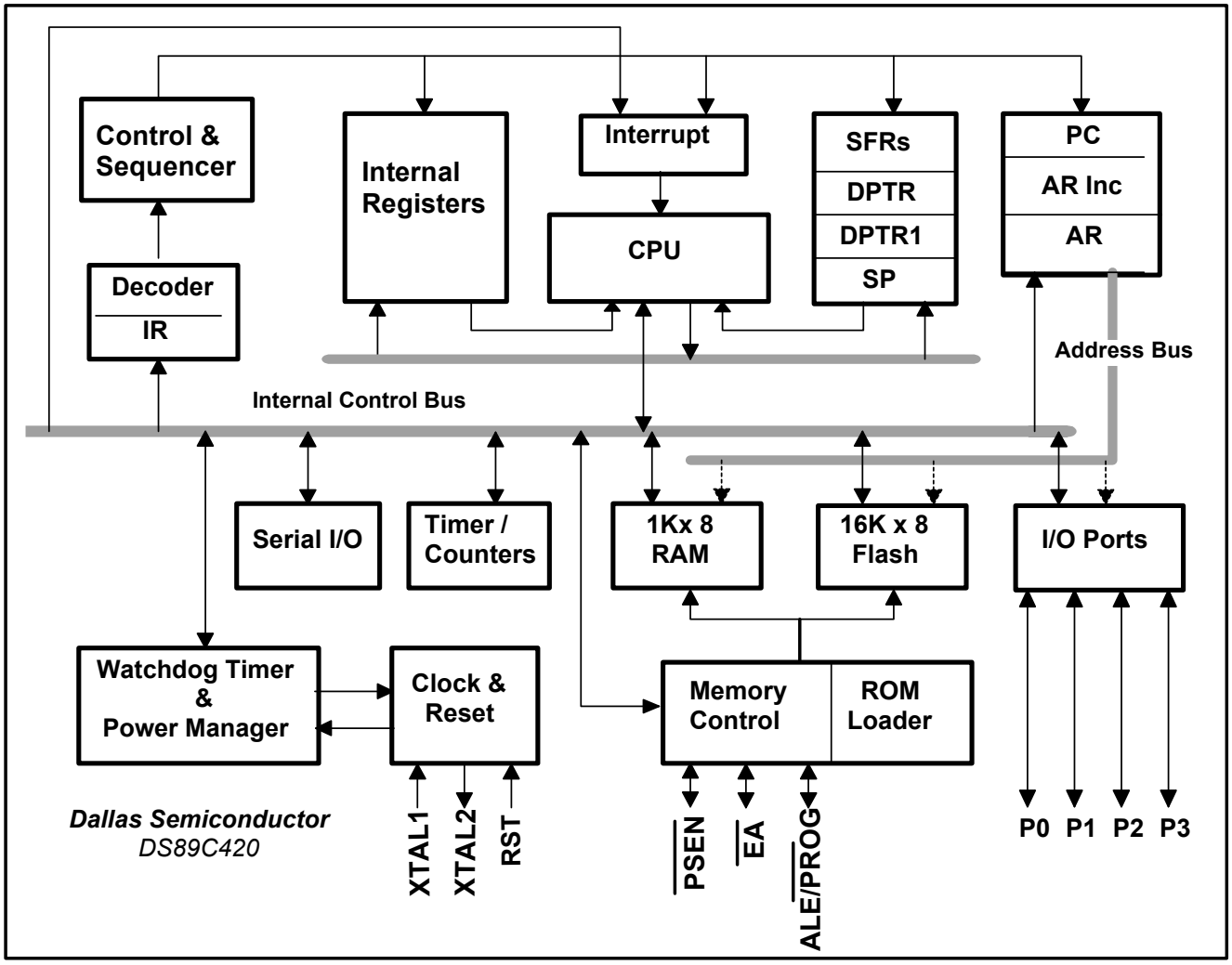
PIN DESCRIPTION

PIN			NAME	FUNCTION		
DIP	PLCC	TQFP				
40	12, 44	6, 38	V_{CC}	V_{CC} - +5V		
20	1, 22, 23, 34	16, 17, 28, 39	GND	Logic Ground		
9	10	4	RST	External Reset. The RST input pin is bidirectional and contains a Schmitt trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, since the device provides this function internally.		
19	21	15	XTAL1	XTAL1, XTAL2. The crystal oscillator pins XTAL1 and XTAL2 provide support for fundamental mode parallel resonant, AT cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.		
18	20	14	XTAL2			
29	32	26	$\overline{PSEN}$	Program Store Enable. This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In 1-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.		
30	33	27	ALE/$\overline{PROG}$	Address Latch Enable. Functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.		
39	43	37	P0.0 (AD0)	Port 0 (AD0–7), I/O. Port 0 is an open-drain 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of Port 0 is three-state. Pullup resistors are required when using Port 0 as an I/O port.		
38	42	36	P0.1 (AD1)			
37	41	35	P0.2 (AD2)			
36	40	34	P0.3 (AD3)			
35	39	33	P0.4 (AD4)			
34	38	32	P0.5 (AD5)			
33	37	31	P0.6 (AD6)			
32	36	30	P0.7 (AD7)			
1–8	2–9	40–44, 1–3	P1.0–P1.7	Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of Port 1 are outlined below.		
				PORT	**ALTERNATE**	**FUNCTION**
1	2	40		P1.0	T2	External I/O for Timer/Counter 2
2	3	41		P1.1	T2EX	Timer 2 Capture/Reload Trigger
3	4	42		P1.2	RXD1	Serial Port 1 Receive
4	5	43		P1.3	TXD1	Serial Port 1 Transmit
5	6	44		P1.4	INT2	External Interrupt 2 (Positive Edge Detect)
6	7	1		P1.5	$\overline{INT3}$	External Interrupt 3 (Negative Edge Detect)
7	8	2		P1.6	INT4	External Interrupt 4 (Positive Edge Detect)
8	9	3		P1.7	$\overline{INT5}$	External Interrupt 5 (Negative Edge Detect)

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th colspan="3">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>PDIP</th><th></th><th></th><th></th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td colspan="3" rowspan="8">Port 2 (A8–15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus; in page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2 (A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3 (A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4 (A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5 (A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6 (A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7 (A15)</td></tr>
<tr><td rowspan="2">10–17</td><td rowspan="2">11, 13–19</td><td rowspan="2">5, 7–13</td><td rowspan="2">P3.0–P3.7</td><td colspan="3">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.</td></tr>
<tr><td>PORT</td><td>ALTERNATE</td><td>FUNCTION</td></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Receive</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Transmit</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td colspan="3">External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C420 to use an external memory-program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

Figure 5. Block Diagram



DETAILED DESCRIPTION

The DS89C420 is pin compatible with all three packages of the standard 8051 and includes standard resources such as three timer/counters, four 8-bit I/O ports, and a serial port. It features 16kB of in-system programmable flash memory, which can be programmed in-system from an I/O port using a built-in program memory loader. It can also be loaded externally using standard commercially available programmers.

Besides greater speed, the DS89C420 includes 1kB of data RAM, a second full-hardware serial port, seven additional interrupts, two more levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. The device also provides dual data pointers (DPTRs) to speed up block-data memory moves. This feature is further enhanced with a new selectable automatic increment/decrement and toggle-select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycle times for flexibility in selecting external memory and peripherals.

A power management mode (PMM) significantly consumes less power by slowing the CPU execution rate from 1 clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable a normal speed response to interrupts.

The EMI reduction feature disables the ALE signal when the processor is not accessing external memory.

COMPATIBILITY

The DS89C420 is a fully static CMOS 8051-compatible microcontroller similar to the DS87C520 in functional features, but with much higher performance. In most cases the DS89C420 can drop into an existing socket for the 8xC51 family to improve the operation significantly. While remaining familiar to 8051 family users, it has many new features. The DS89C420 runs the standard 8051 family instruction set and is pin compatible with DIP, PLCC, and TQFP packages. In general, software written for existing 8051-based systems works without DS89C420 modification, with the exception of critical timing routines, since the DS89C420 performs its instructions much faster than the original for any given crystal selection.

The DS89C420 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to a 12 clock-per-cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 1 clock-per-cycle if desired. The DS89C420 provides several new hardware features implemented by new SFRs.

PERFORMANCE OVERVIEW

The DS89C420 features a completely redesigned high-speed 8051-compatible core and allows operation at a higher clock frequency, but the updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS89C420, the same machine cycle takes 1 clock. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement reduces when using external memory access modes that require more than 1 clock per cycle.

Improvement of individual programs depends on the actual instructions used. Speed-sensitive applications make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architecture improvements produce instruction cycle times as low as 30ns (33MIPs). The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is also identical. However, the timing of each instruction is different in both absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using information in the “Instruction Set” table of the *Ultra-High-Speed Flash Microcontroller User’s Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at lower numbers of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C420, the MOVX instruction takes as little as two machine cycles or two oscillator cycles but the “MOV direct, direct” uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C420 usually uses one machine cycle for each instruction byte and requires one cycle for execution. The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes.

SPECIAL FUNCTION REGISTERS (SFRS)

All peripherals and operations that are not explicit instructions in the DS89C420 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers (DPTRs), stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function’s status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs whose addresses end in 0h or 8h are bit-addressable.

4kB (1000h) boundary or above the 16kB (3FFFh) boundary so that it is unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

For non-page mode operations, off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip program memory access also occurs if the $\overline{EA}$ pin is logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when port 0 and port 2 fetch from external program memory.

The $\overline{RD}$ and $\overline{WR}$ signals are used to control the external data memory device. Data memory is accessed by MOVX instructions. The MOVX@Ri instruction uses the value in the designated working register to provide the LSB of the address, while port 2 supplies the address MSB. The MOVX@DPTR instruction uses one of the two data pointers to move data over the entire 64kB external data memory space. Software selects the data pointer to be used by writing to the SEL bit (DPS.0).

The DS89C420 also provides a user option for high-speed external memory access by reconfiguring the external memory interface into page mode operation.

Note: When using the original 8051 expanded bus structure, the throughput is reduced by 75% compared with that of internal operations. This is due to the CPU being stalled for three out of four clocks waiting for the data fetch, which takes four clocks. Page Mode 1 is the only external addressing mode where the CPU does not require stalls for external memory access, but page misses result in reduced external access performance.

ON-CHIP PROGRAM MEMORY

The processor can fetch the full on-chip program memory range automatically. The reset routines and all interrupt vectors are located in the lower 128 bytes of the on-chip program memory area.

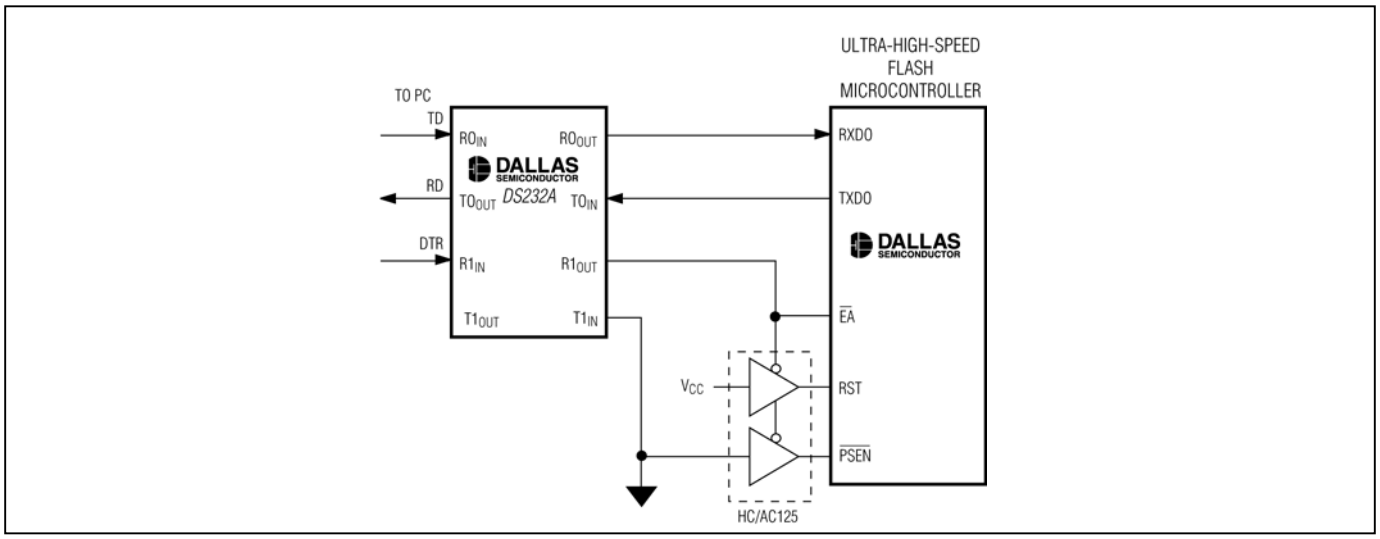
On-chip program memory is logically divided into two 8kB flash memory banks and is designed to be programmed with the standard 5V V_{CC} supply by using a built-in program memory loader. It can also be programmed in standard flash or EPROM programmers. The DS89C420 incorporates a memory management unit (MMU) and other hardware to support any of the two programming methods. The MMU controls program and data memory access, and provides sequencing and timing controls for programming the on-chip program memory. There is also a separate security flash block that is used to support a standard three-level lock, a 64-byte encryption array, and other flash options.

SECURITY FEATURES

The DS89C420 incorporates a 64-byte encryption array, allowing the user to verify program codes while viewing the data in encrypted form. The encryption array is implemented in a security flash memory block that has the same electrical and timing characteristics as the on-chip program memory. Once the encryption array is programmed to non-FFh, the data presented in the verify mode is encrypted. Each byte of data is XNORed with a byte in the encryption array during verification.

A three-level lock restricts viewing of the internal program and data memory contents. By programming the three lock bits, the user can select a level of security as specified in Table 3. Once a security level is selected and programmed, the setting of the lock bits remains. Only a mass erase can erase these bits to allow reprogramming the security level to a less restricted protection.

Figure 7. Interfacing the Bootloader to a PC



PARALLEL PROGRAMMING

The DS89C420 allows parallel programming of its internal flash memory compatible with standard flash or EPROM programmers. In parallel programming mode, a mass-erase command is used to erase all memory locations in the 16kB program memory, the security block, and the memory bank select. Erasing the memory bank select sets it to the default state; the memory bank select cannot be altered otherwise. If lock bit LB2 has not been programmed, the program code can be read back for verification. The state of the lock bits can also be verified directly in the parallel programming mode. One instruction is used to read signature information (at addresses 30, 31, and 60h). Separate instructions are used for the option control register.

The following sequence can be used to program the flash memory in the parallel programming mode:

1) The DS89C420 is powered up and running at a clock speed between 4MHz and 6MHz.
2) Set RST = $\overline{EA}$ = 1 and $\overline{PSEN}$ = 0.
3) Apply the appropriate logic combination to pins P2.6, P2.7, P3.6, and P3.7 to select one of the flash instructions shown in Table 7.
   For program operation, apply the desired address to pins P1.7:0 and P2.5:0. Data is written to port 0.
   For verify operation, apply the desired address to pins P1.7:0 and P2.5:0. Data is read at port 0.
4) Pulse ALE/$\overline{PROG}$ once to perform an erase/program operation.
5) Repeat steps 3 and 4 as necessary.

ON-CHIP MOVX DATA MEMORY

On-chip data memory is provided by the 1kB SRAM and occupies addresses 0000h through 03FFh. The internal data memory is disabled after a power-on reset, and any MOVX instruction directs the data memory access to the external data memory. To enable the internal data memory, software must configure the data memory enable bits DME1 and DME0 (PMR.1-0). See “SFR Bit Descriptions” in the *Ultra-High-Speed Flash Microcontroller User’s Guide* for data memory configurations. Once enabled, MOVX instructions with addresses inside the 1k range access the on-chip data memory, and addresses exceeding the 1k range automatically access external data memory.

An internal data memory cycle spans only one system clock period to support fast internal execution.

Figure 9. Non-Page Mode, External Data-Memory Access (Stretch = 0, CD1:CD2 = 10)

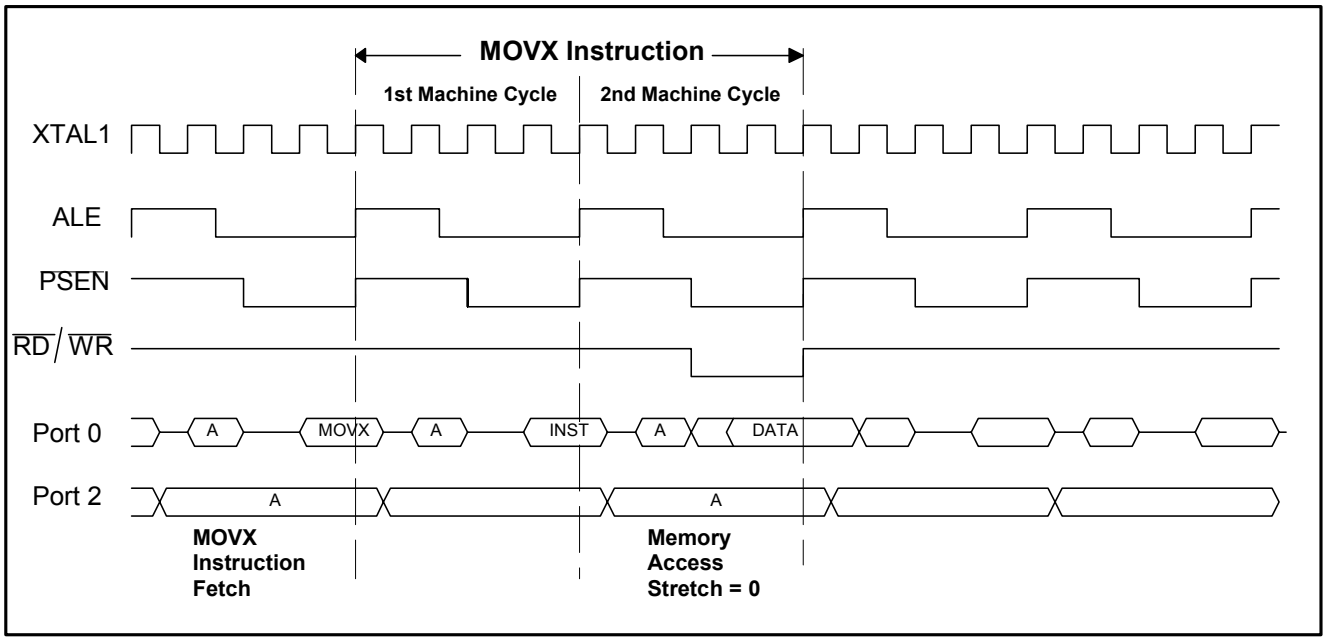
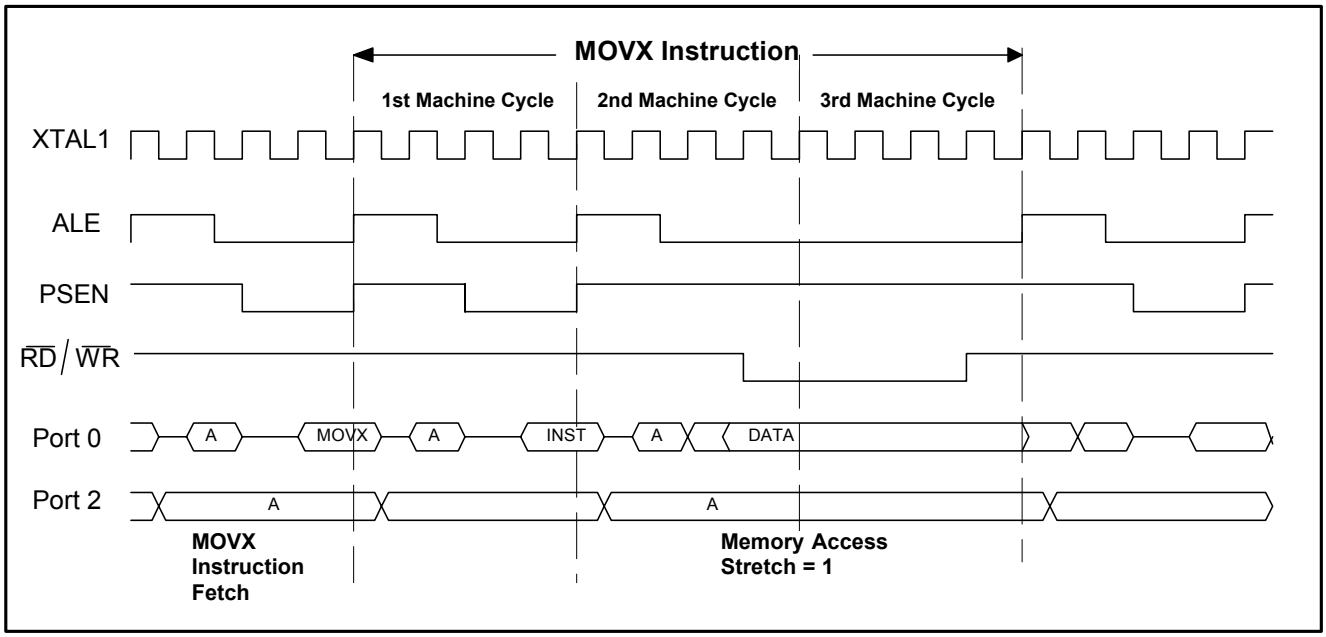


Figure 10. Non-Page Mode, External Data-Memory Access (Stretch = 1, CD1:CD2 = 10)



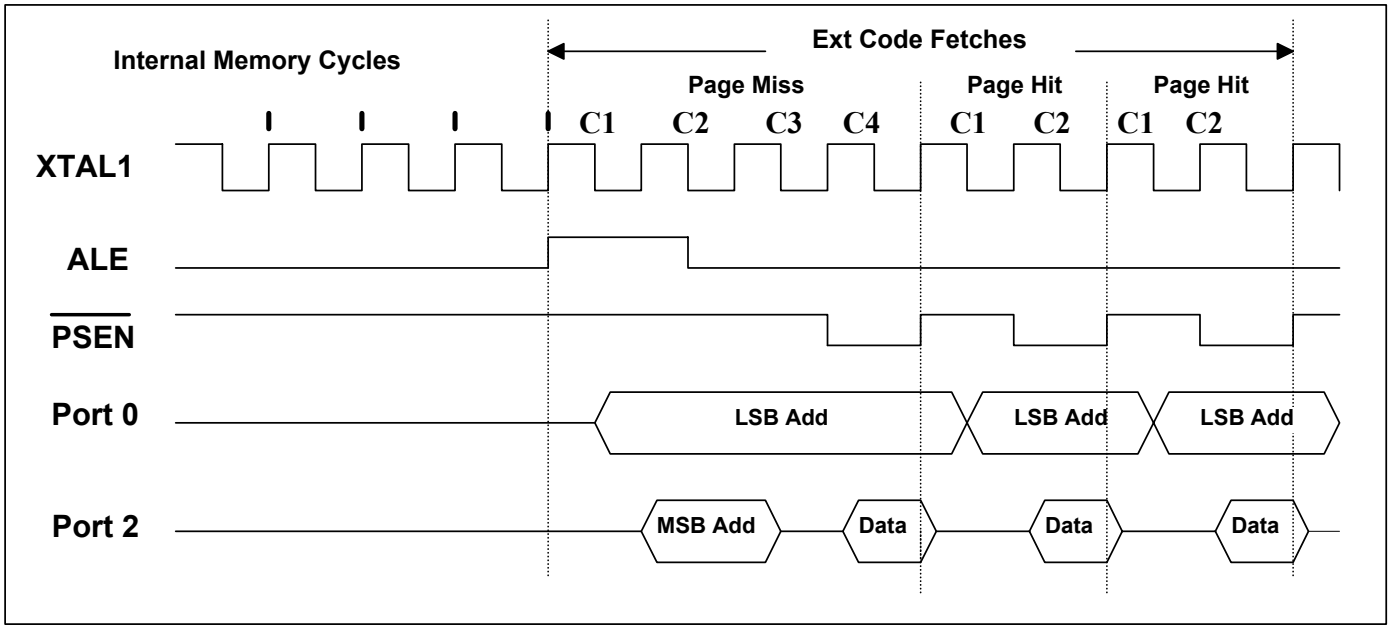
Note that there are a few exceptions for this mode of operation when PAGES1 and PAGES2 are set to 00b:

- $\overline{\text{PSEN}}$ is asserted for both page hit and page miss for a full clock cycle.
- The execution of external MOVX instruction causes a page miss.
- A page miss occurs when fetching the next external instruction following the execution of an external MOVX instruction.

Figure 11 shows the external memory cycle for this bus structure. The first case illustrates a back-to-back execution sequence for 1-cycle page mode (PAGES1 = PAGES0 = 0b). $\overline{\text{PSEN}}$ remains active during page-hit cycles, and page misses are forced during and after MOVX executions, independent of the most significant byte of the subsequent addresses. The second case illustrates a MOVX execution sequence for 2-cycle page mode (PAGES1 = 0 and PAGES0 = 1). $\overline{\text{PSEN}}$ is active for a full clock cycle in code fetches. Note that changing the MSB of the data address causes the page misses in this sequence. The third case illustrates a MOVX execution sequence for 4-cycle page mode (PAGES1 = 1 and PAGES0 = 0). There is no page miss in this execution cycle because the most significant byte of the data address is assumed to match the last program address.

The second page mode (page mode 2) external bus structure multiplexes the most significant address byte with data on P2, and uses P0 for the least significant address byte. This bus structure is used to speed up external code fetches only. External data-memory access cycles are identical to the non-page mode except for the different signals on P0 and P2. Figure 12 illustrates the memory cycle for external code fetches.

Figure 12. Page Mode 2, External Code Fetch Cycle (CD1:CD0 = 10)



STRETCH EXTERNAL DATA MEMORY CYCLE IN PAGE MODE

The DS89C420 allows software to adjust the speed of external data memory access by stretching the memory bus cycle in page mode operation just like non-page mode operation. The following tables summarize the stretch values and their effects on the external MOVX-memory bus cycle and the control signals' pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks, independent of the logic value of the page mode select bits.

Table 7. Page Mode 1, Data Memory Cycle Stretch Values (Pages1:Pages0 = 00)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 8. Page Mode 1, Data Memory Cycle Stretch Values (Pages1:Pages0 = 01)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

regardless of the individual interrupt enable settings. The power-fail interrupt is controlled by its individual enable only.

The interrupt enables and priorities are functionally identical to those of the 80C52, except that the DS89C420 supports five levels of interrupt priorities instead of the original two.

INTERRUPT PRIORITY

There are five levels of interrupt priority: level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power-Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1)**	EX0 (IE.0)	LPX0 (IP0.0) MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5)*	ET0 (IE.1)	LPT0 (IP0.1) MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3)**	EX1 (IE.2)	LPX1 (IP0.2) MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7)*	ET1 (IE.3)	LPT1 (IP0.3) MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4) MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7) EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5) MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0) TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6) MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0) MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1) MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2) MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3) MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4) MPWDI (EIP1.4)

**Cleared automatically by hardware when the service routine is vectored to.*
***If the interrupt is edge triggered, cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.*

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

TIMER/COUNTERS

Three 16-bit timers are incorporated in the DS89C420. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that count oscillator cycles. Table 12 summarizes the timer functions.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with auto-reload. Timer 0 has a fourth operating mode as two 8-bit

Before these bits can be altered, the processor must execute the timed access sequence. This sequence consists of writing an AAh to the timed access (TA, C7h) register, followed by writing a 55h to the same register within three machine cycles. This timed sequence of steps then allows any of the timed-access-protected SFR bits to be altered during the three machine cycles, following the writing of the 55h. Writing to a timed access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address-, data-, and time-dependent. A processor running out of control and not executing system software cannot statistically perform this timed sequence of steps, and as such, will not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. It is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

POWER MANAGEMENT AND CLOCK-DIVIDE CONTROL

The DS89C420 incorporates power management features that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h), and power control (PCON, 87h) registers.

SYSTEM CLOCK-DIVIDE CONTROL

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and also to slow the system clocks providing lower power operation when required. An on-chip crystal multiplier allows the DS89C420 to operate at two or four times the crystal frequency by setting the 4X/$\overline{2X}$ bit and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide-by-1024. When used with a 7.372MHz crystal, for example, the processor executes machine cycle in times ranging from 33.9ns (divide-by-0.25) to 138.9µs (multiply-by-1024), and maintains a highly accurate serial port baud rate while allowing the use of more cost-effective, lower-frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features have been provided to enhance the use of these clock controls to guarantee proper serial port operation, and also to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved, and has the same effect as the 10b setting, which forces the system clock into a divide by 1 mode. The DS89C420 defaults to divide-by-1 clock mode on all forms of reset.

When programmed to the divide-by-1024 mode, and the switchback bit (PMR.5:SWB) is also set, the system forces the clock-divide control bits to reset automatically to the divide-by-1 mode whenever the system has detected externally enabled interrupts.

The oscillator divide ratios of 0.25, 0.5, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH, TxM = 00b, x = 1, 2, or 3) to the timers.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled during divide-by-1024 mode, and all other clock modes are unaffected by interrupts and serial port activity. See *Power Management Mode* for more details.

Use of the divide-by-0.25 or 0.5 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the 4X/$\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The 4X/$\overline{2X}$ bit can only be altered when the CTM bit is cleared to logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled through the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to logic 0 on all resets. Figure 15 gives a

WATCHDOG TIMER

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. When the clock divider is set to 10b, the interrupt timeout has a default divide ratio of 2^{17} of the crystal oscillator clock, with the watchdog reset set to timeout 512 system clock cycles later. This results in a 33MHz crystal oscillator producing an interrupt timeout every 3.9718ms, followed 15.5µs later by a watchdog reset. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the clock control (CKCON.6 and 7) register, other divide ratios can be selected for longer watchdog interrupt periods. Table 13 summarizes the watchdog bit settings and the timeout values.

Note: All watchdog-timer reset timeouts follow the programmed interrupt timeouts by 512 system clock cycles, which equates to varying numbers of oscillator cycles depending on the clock-divide (CD1:0) and crystal multiplier settings.

Table 13. Watchdog Timeout Value (in Number of Oscillator Clocks)

4X/$\overline{2X}$	CD1:0	WATCHDOG INTERRUPT TIMEOUT				WATCHDOG RESET TIMEOUT			
		WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11	WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15} + 128	2^{18} + 128	2^{21} + 128	2^{24} + 128
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16} + 256	2^{19} + 256	2^{22} + 256	2^{25} + 256
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	11	2^{27}	2^{30}	2^{33}	2^{36}	2^{27} + 524,288	2^{30} + 524,288	2^{33}+ 524,288	2^{36} + 524,288

A watchdog control (WDCON) SFR is used for programming the functions. EWT (WDCON.1) is the enable for the watchdog-timer reset function and RWT (WDCON.0) is the bit used to restart the watchdog timer. Setting the RWT bit restarts the timer for another full interval. If the watchdog timer reset function is masked by the EWT bit and no resets are issued to the timer through the RWT bit, the watchdog timer generates interrupt timeouts at a rate determined by the programmed divide ratio. WDIF (WDCON.3) is the interrupt flag set at timer termination and WTRF (WDCON.2) is the reset flag set following a watchdog-reset timeout. The watchdog interrupt is enabled by the EWDI bit (EIE.4) when it is set to 1. The watchdog timer reset and interrupt timeouts are measured by counting system clock cycles.

An independent watchdog timer functions as the crystal startup counter to count 65,536 crystal clock cycles before allowing the crystal oscillator to function as the system clock. This warmup time is verified by the watchdog timer following each power-up as well as each time the crystal is restarted following a stop mode. The watchdog is also used to establish a startup time whenever the CTM in the PMR register is set to enable the crystal multiplier (4X/$\overline{2X}$).

One of the applications of the watchdog timer is for the watchdog to wake up the system from idle mode. The watchdog interrupt can be programmed to allow a system to wake up periodically to sample the external world.

EXTERNAL RESET

If the RST input is taken to a logic 1, the device is forced into a reset state. An external reset is accomplished by holding the RST pin high for at least 3 clock cycles while the oscillator is running. Once the reset state is invoked, it is maintained as long as RST is pulled to logic 1. When the RST is removed, the processor exits the reset state within 4 clock cycles and begins execution at address 0000h. If a RST is applied while the processor is in stop mode, the RST causes the oscillator to begin running and forces the program counter to 0000h. There is a reset delay of 65,536 clock cycles to allow the oscillator to stabilize.

The RST pin is a bidirectional I/O. If a reset is caused by a power-fail reset, a watchdog timer reset, or an internal system reset, an output-reset pulse is also generated at the RST pin. This reset pulse is asserted as long as an internal reset is asserted and may not be able to drive the reset signal out if the RST pin is connected to an RC circuit. Connecting the RST pin to a capacitor does not affect the internal reset condition.

Table 14. Effect of Clock Mode on Timer Operation (in Number of Oscillator Clocks)

4X/2X, CD1, CD0	OSC. CYCLES PER MACHINE CYCLE	OSC. CYCLES PER TIMERS (0, 1, 2) CLOCK			OSC. CYCLES PER TIMER 2 CLOCK	OSC. CYCLES PER SERIAL PORT CLOCK MODE 0		OSC. CYCLES PER SERIAL PORT CLOCK MODE 2	
		TxMH, TxM =			BAUD RATE GENERATOR T2MH, T2M = xx				
		00	01	1x		SM2 = 0	SM2 = 1	SMOD = 0	SMOD = 1
100	0.25	12	1	0.25	2	3	1	64	32
000	0.5	12	2	0.5	2	6	2	64	32
x01	1 (reserved)	—			—	—		—	
x10	1 (default)	12	4	1	2	12	4	64	32
x11	1,024	12,288	4,096	1,024	2,048	12,288	4,096	65,536	32,768

x = don't care

RING OSCILLATOR

A ring oscillator, which typically runs at 10MHz, allows the processor to recover instantly from the stop mode.

When the system is in stop mode the crystal is disabled. When stop mode is removed, the crystal requires a period of time to start up and stabilize. To allow the system to begin immediate execution of software following the removal of the stop mode, the ring oscillator is used to supply a system clock until the crystal startup time is satisfied. Once this time has passed, the ring oscillator is switched off and the system clock is switched over to the crystal oscillator. This function is programmable and is enabled by setting the RGSL bit (EXIF.1) to logic 1. When it is logic 0, the processor delays software execution until after the 65,536 crystal clock periods. To allow the processor to know whether it is being clocked by the ring or the crystal oscillator, an additional bit, termed the RGMD bit, indicates which clock source is being used. When the processor is running from the ring, the clock-divide control bits (CD1 and CD0 in the PMR register) are locked into the divide-by-1 mode (CD1:CD0 = 10b). The clock-divide control bits cannot be changed from this state until after the system clock transitions to the crystal oscillator (RGMD = 0).

Note: The watchdog is permanently connected to the crystal oscillator and continues to run at the external clock rate. The ring oscillator does not drive it.

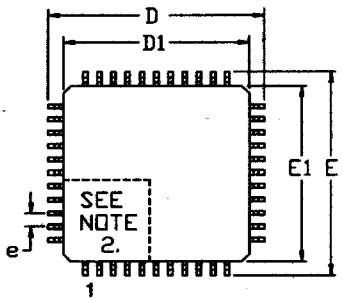
IDLE MODE

Idle mode suspends the processor by holding the program counter in a static state. No instructions are fetched and no processing occurs. Setting the IDLE bit (PCON.0) to logic 1 invokes idle mode. The instruction that executes this step is the last instruction prior to freezing the program counter. Once in Idle mode, all resources are preserved but all peripheral clocks remain active, and the timers, watchdog, serial ports, and power monitor functions continue to operate, so that the processor can exit the idle mode using any interrupt sources that are enabled. The oscillator-detect circuit also continues to function when enabled. The IDLE bit is cleared automatically once idle mode is exited. On returning from the interrupt vector using the RETI instruction, the next address is the one that immediately follows the instruction that invoked the idle mode. Any processor resets also remove the idle mode.

STOP MODE

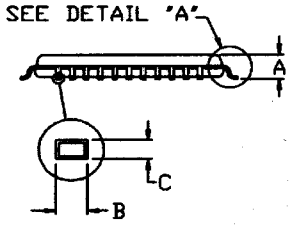
The stop mode disables all circuits within the processor. All on-chip clocks, timers, and serial port communication are stopped, and no processing is possible.

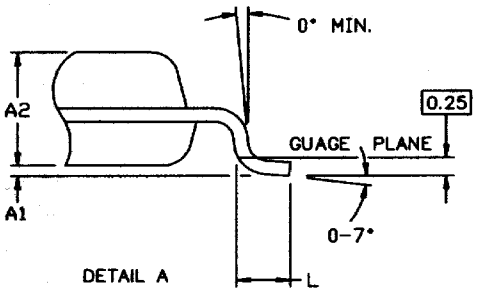
Stop mode is invoked by setting the STOP bit (PCON.1) to logic 1. The processor enters the stop mode on the instruction that sets the bit. The processor can exit stop mode by using any of the six external interrupts that are enabled.



NOTES:

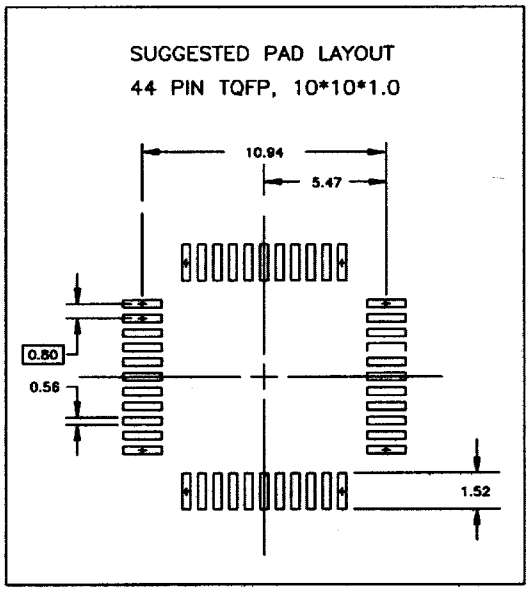
1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.





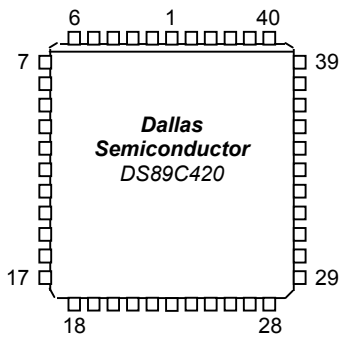
PKG	44-PIN	
DIM	MIN	MAX
A	–	1.20
A1	0.05	0.15
A2	0.95	1.05
D	11.80	12.20
D1	10.00 BSC	
E	11.80	12.20
E1	10.00 BSC	
L	0.45	0.75
e	0.80 BSC	
B	0.30	0.45
C	0.09	0.20

56-G4012-001



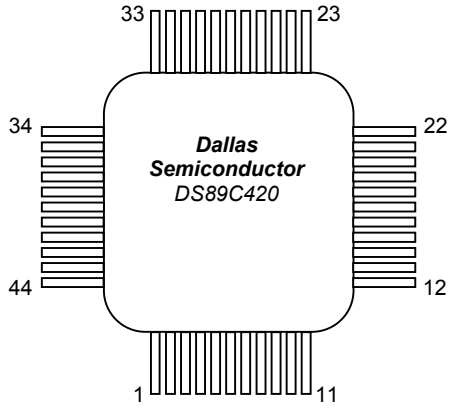
PIN CONFIGURATIONS

TOP VIEW



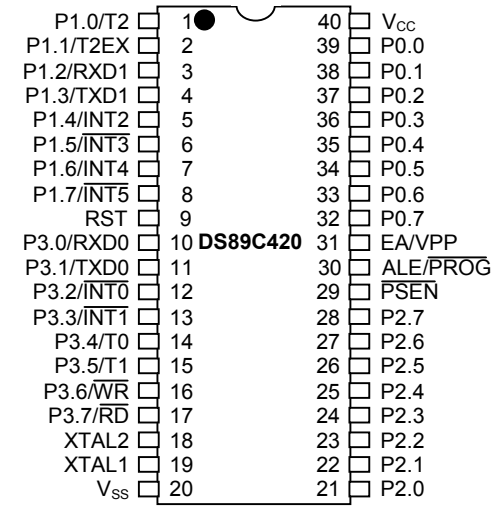
PLCC

TOP VIEW



TQFP

TOP VIEW



DIP