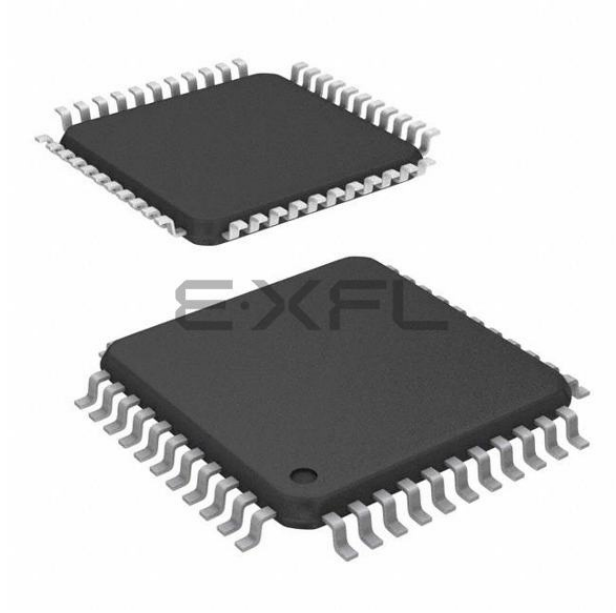
Analog Devices Inc./Maxim Integrated - DS89C420-ENG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c420-eng

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Notes 2, 13)	4.5	5.0	5.5	V
Power-Fail Warning	V_{PFW}	(Notes 2, 12)	4.2	4.375	4.6	V
Reset Trip Point	V_{RST}	(Notes 2, 12, 13)	3.95	4.125	4.35	V
Supply Current Active Mode (Note 3)	I_{CC}	33MHz		100	150	mA
		25MHz		75	125	
Supply Current Idle Mode (Note 4)	I_{IDLE}	33MHz		40	50	mA
		25MHz		40	50	
Supply Current Stop Mode, Bandgap Disabled	I_{STOP}	(Note 5)			40	mA
Supply Current Stop Mode, Bandgap Enabled	I_{SPBG}	(Note 5)			40	mA
Input Low Level	V_{IL}	(Note 2)	-0.3		+0.8	V
Input High Level	V_{IH}	(Note 2)	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST	V_{IH2}	(Note 2)	3.5		V_{CC} + 0.3	V
Output Low Voltage; Port 1 and 3 at I_{OL} = 1.6mA	V_{OL1}	(Note 2)		0.15	0.45	V
Output Low Voltage; Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}	(Note 2)		0.15	0.45	V
Output High Voltage; Port 1, 2, and 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	(Notes 2, 7)	2.4			V
Output High Voltage; Port 1, 2, and 3 at I_{OH} = -1.5mA	V_{OH2}	(Notes 2, 8)	2.4			V
Output High Voltage; Port 0 and 2 in Bus Mode at I_{OH} = -8mA	V_{OH3}	(Notes 2, 6)	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA	V_{OH4}	(Notes 2, 14)	2.4			V
Input Low Current; Port 1, 2, and 3 at 0.4V	I_{IL}		-55			µA
Transition Current from 1 to 0; Port 1, 2, and 3 at 2V	I_{TL}	(Note 9)	-650			µA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$	I_L	(Note 11)	-10		+10	µA
Input Leakage Current, Port 0 in Bus Mode	I_L	(Note 10)	-300		+300	µA
RST Pulldown Resistance	R_{RST}	(Note 11)	50		170	kΩ

PARAMETER	SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		t_{CLCL} - 18		t_{CLCL} - 18		$2t_{CLCL}$ - 18		t_{CLCL} - 18		$2t_{CLCL}$ - 18	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		0		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}								$1.5t_{CLCL}$ - 20		$3t_{CLCL}$ - 20	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}		t_{CLCL} - 18		$1.5t_{CLCL}$ - 18		$2.5t_{CLCL}$ - 18		$3t_{CLCL}$ - 20		$3.5t_{CLCL}$ - 20	ns
$\overline{PSEN}$ Low to Port 0 Address Float	t_{PLAZ}								0		0	ns
$\overline{RD}$ Pulse Width (P3.7) (Note 2)	t_{RLRH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{WR}$ Pulse Width (P3.6) (Note 2)	t_{WLWH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{RD}$ (P3.7) Low to Valid Data In (Note 2)	t_{RLDV}		t_{CLCL} - 15 + t_{STC1}		t_{CLCL} - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}		$2t_{CLCL}$ - 15 + t_{STC1}	ns
Data Hold After $\overline{RD}$ (P3.7)	t_{RHDX}	0		0		0		0		0		ns
Data Float After $\overline{RD}$ (P3.7)	t_{RHDZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
MOVX ALE Low to Input Data Valid (Note 2)	t_{LLDV}								$2.5t_{CLCL}$ - 20 + t_{STC1}		$2.5t_{CLCL}$ - 20 + t_{STC1}	ns
Port 0 Address to Valid Data In (Note 2)	t_{AVDV0}								$3t_{CLCL}$ - 20 + t_{STC1}		$3t_{CLCL}$ - 20 + t_{STC1}	ns

PARAMETER	SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Port 2 Address to Valid Data In (Note 2)	t_{AVDV2}		t_{CLCL} - 16 + t_{STC1}		1.5t_{CLCL} - 16 + t_{STC1}		3.5t_{CLCL} - 16 + t_{STC1}		3.0t_{CLCL} - 16 + t_{STC1}		3.5t_{CLCL} - 20 + t_{STC1}	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (Note 2)	t_{LLRL} (t_{LLWL})	0.5t_{CLCL} - 8 + t_{STC2}	0.5t_{CLCL} + 1 + t_{STC2}	2t_{CLCL} - 8 + t_{STC2}	2t_{CLCL} + 8 + t_{STC2}	4t_{CLCL} - 8 + t_{STC2}	4t_{CLCL} + 8 + t_{STC2}	0.5t_{CLCL} - 8 + t_{STC2}	0.5t_{CLCL} + 4 + t_{STC2}	0.5t_{CLCL} - 8 + t_{STC2}	0.5t_{CLCL} + 4 + t_{STC2}	ns
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 2)	t_{AVRL0} (t_{AVWL0})							1.5t_{CLCL} - 5 + t_{STC2}		t_{CLCL} - 5 + t_{STC2}		ns
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 2)	t_{AVRL2} (t_{AVWL2})	0 + t_{STC5} - 5		0.5t_{CLCL} - 5 + t_{STC5}		1.5t_{CLCL} - 5 + t_{STC5}		t_{CLCL} - 5 + t_{STC5}		1.5t_{CLCL} - 5 + t_{STC5}		ns
Data Out Valid to $\overline{WR}$ Transition (Note 1)	t_{QVWX}	-5		-5		-5		-5		-5		ns
Data Hold After $\overline{WR}$ (Note 1)	t_{WHQX}	20		20		20		20		20		ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High (Note 1)	t_{RHLH} (t_{WHLH})	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	t_{STC2} - 2	t_{STC2} + 6	ns

**Specifications to -40°C are guaranteed by design and not production tested.*

Note 1: The system clock frequency is dependent on the oscillator frequency and the setting of the clock-divide control bits (CD1 and CD0) and the crystal multiplier control bits (4X/$\overline{2X}$ and CTM) in the PMR register. The term "1 / t_{CLCL}" used in the variable timing table is calculated through the use of the table given below.

4X/$\overline{2X}$	CD1	CD0	NUMBER OF OSCILLATOR CYCLES PER SYSTEM CLOCK (1 / t_{CLCL})
1	0	0	4 Oscillator Cycles
0	0	0	2 Oscillator Cycles
X	0	1	Reserved
X	1	0	1 Oscillator Cycle
X	1	1	1 / 1024 Oscillator Cycle

Note 2: External MOVX instruction times are dependent on the setting of the MD2, MD1, and MD0 bits in the clock control register. The terms "t_{STC1}, t_{STC2}, t_{STC3}" used in the variable timing table are calculated through the use of the table given below.

MD2	MD1	MD0	MOVX INSTRUCTION TIME (MACHINE CYCLES)	t_{STC1} (t_{CLCL})	t_{STC2} (t_{CLCL})	t_{STC3} (t_{CLCL})	t_{STC4} (t_{CLCL})	t_{STC5} (t_{CLCL})
0	0	0	2	0	0	0	0	0
0	0	1	3	2	1	0	0	1
0	1	0	4	6	1	0	0	1
0	1	1	5	10	1	0	0	1
1	0	0	9	14	5	4	1	1
1	0	1	10	18	5	4	1	1
1	1	0	11	22	5	4	1	1
1	1	1	12	26	5	4	1	1

Note 3: Maximum load capacitance (to meet the above timing) for Port 0, ALE, $\overline{PSEN}$, $\overline{WR}$, and $\overline{RD}$ is limited to 60pF. XTAL1 and XTAL2 load capacitance is dependent on the frequency of the selected crystal.

Figure 1. Non-Page Mode Timing

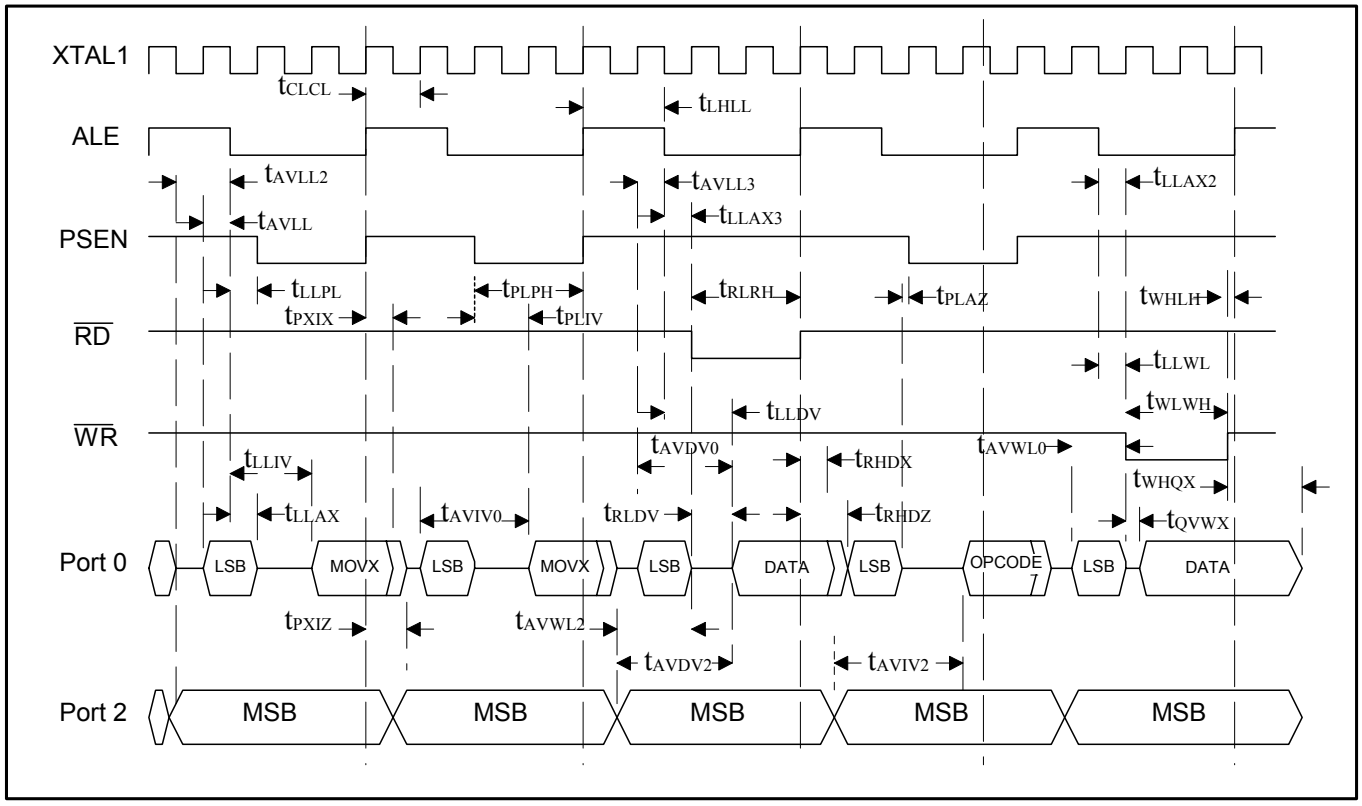


Figure 2. Page-Mode 1 Timing

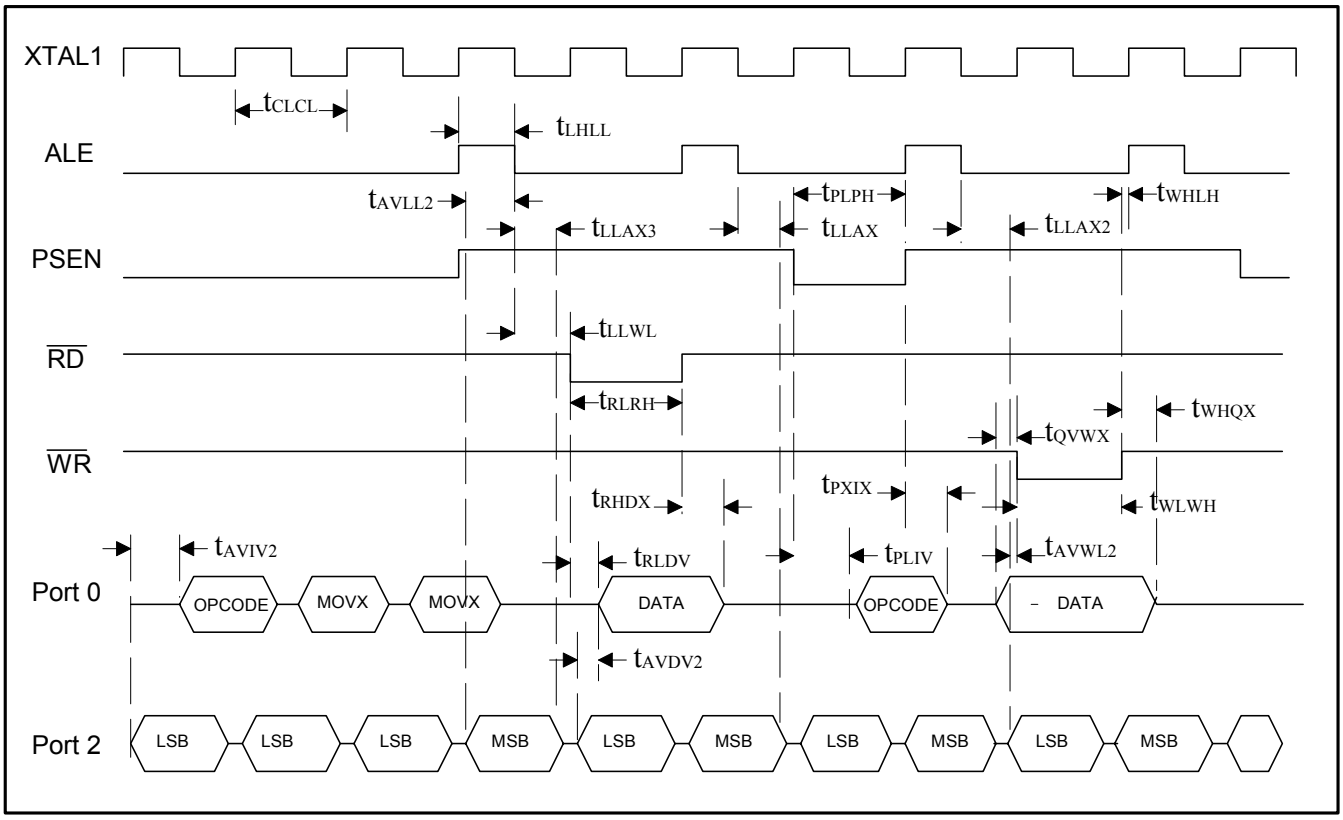
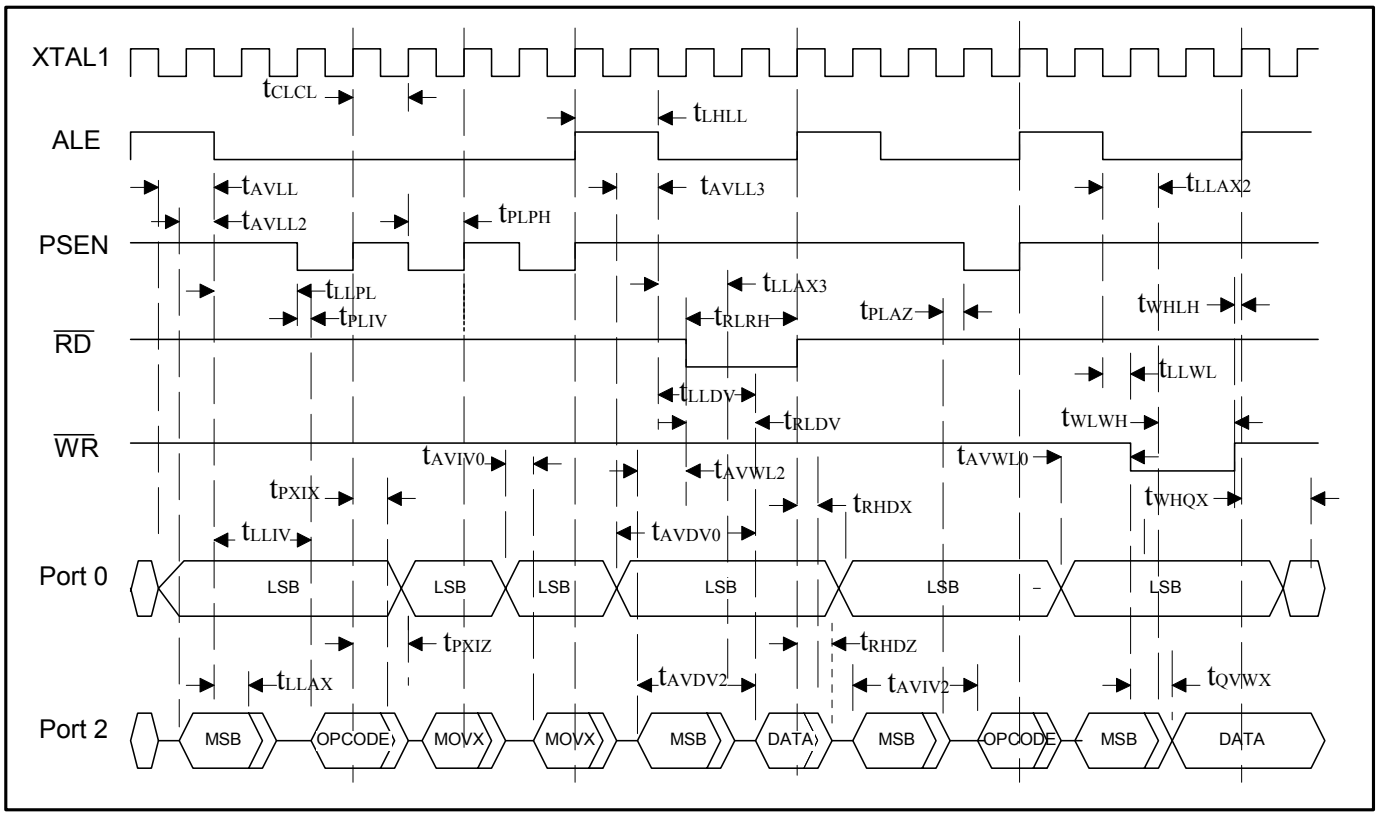


Figure 3. Page-Mode 2 Timing



EXTERNAL CLOCK CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)*

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

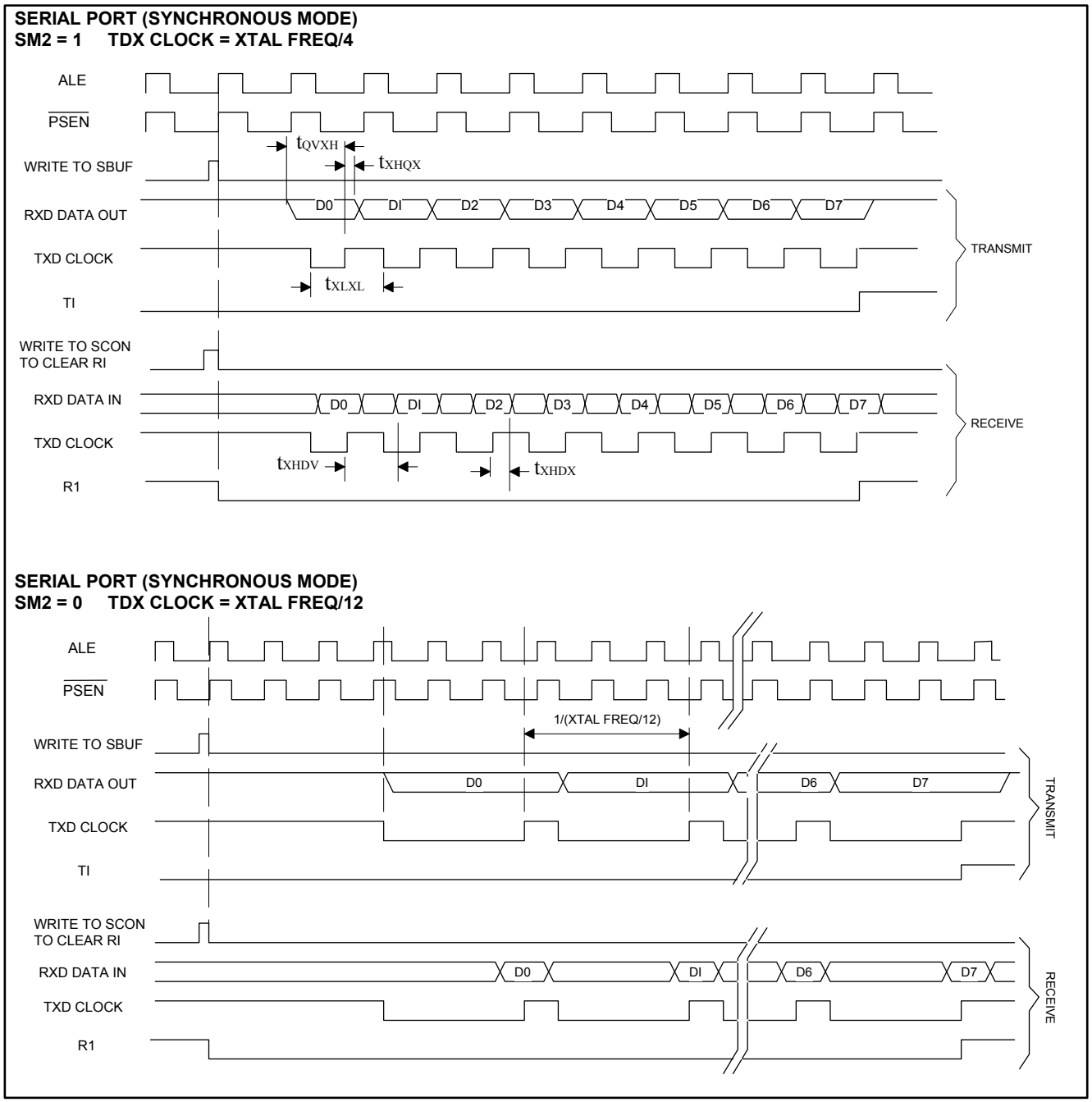
(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)* (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	

Note: SM2 is the serial port 0, mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial-port clock cycle.

**Specifications to -40°C are guaranteed by design and not production tested.*

Figure 4. Serial Port Timing



PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th colspan="3">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>PDIP</th><th></th><th></th><th></th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td colspan="3" rowspan="8">Port 2 (A8–15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus; in page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2 (A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3 (A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4 (A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5 (A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6 (A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7 (A15)</td></tr>
<tr><td rowspan="2">10–17</td><td rowspan="2">11, 13–19</td><td rowspan="2">5, 7–13</td><td rowspan="2">P3.0–P3.7</td><td colspan="3">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.</td></tr>
<tr><td>PORT</td><td>ALTERNATE</td><td>FUNCTION</td></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Receive</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Transmit</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td colspan="3">External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C420 to use an external memory-program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

COMPATIBILITY

The DS89C420 is a fully static CMOS 8051-compatible microcontroller similar to the DS87C520 in functional features, but with much higher performance. In most cases the DS89C420 can drop into an existing socket for the 8xC51 family to improve the operation significantly. While remaining familiar to 8051 family users, it has many new features. The DS89C420 runs the standard 8051 family instruction set and is pin compatible with DIP, PLCC, and TQFP packages. In general, software written for existing 8051-based systems works without DS89C420 modification, with the exception of critical timing routines, since the DS89C420 performs its instructions much faster than the original for any given crystal selection.

The DS89C420 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to a 12 clock-per-cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 1 clock-per-cycle if desired. The DS89C420 provides several new hardware features implemented by new SFRs.

PERFORMANCE OVERVIEW

The DS89C420 features a completely redesigned high-speed 8051-compatible core and allows operation at a higher clock frequency, but the updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS89C420, the same machine cycle takes 1 clock. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement reduces when using external memory access modes that require more than 1 clock per cycle.

Improvement of individual programs depends on the actual instructions used. Speed-sensitive applications make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architecture improvements produce instruction cycle times as low as 30ns (33MIPs). The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is also identical. However, the timing of each instruction is different in both absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using information in the “Instruction Set” table of the *Ultra-High-Speed Flash Microcontroller User’s Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at lower numbers of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C420, the MOVX instruction takes as little as two machine cycles or two oscillator cycles but the “MOV direct, direct” uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C420 usually uses one machine cycle for each instruction byte and requires one cycle for execution. The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes.

SPECIAL FUNCTION REGISTERS (SFRS)

All peripherals and operations that are not explicit instructions in the DS89C420 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers (DPTRs), stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function’s status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs whose addresses end in 0h or 8h are bit-addressable.

All standard SFR locations from the 8051 are duplicated in the DS89C420 and several SFRs have been added for the unique features of the DS89C420. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map. This allows for increased functionality while maintaining complete instruction set compatibility. Table 1 summarizes the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

DATA POINTERS

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip), or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user selects the active pointer through a dedicated SFR bit (Sel = DPS.0), or activates an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

STACK POINTER

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O PORTS

The DS89C420 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location, and can be written or read. The I/O port has a latch that contains the value written by software.

COUNTER/TIMERS

Three 16-bit timer/counters are available in the DS89C420. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs described in the “SFR Bit Description” section of the *Ultra-High-Speed Flash Microcontroller User’s Guide*.

SERIAL PORTS

The DS89C420 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the UART. The same address is used for read and write operations, which are distinguished by the instruction. Its own SFR control register controls each UART.

4kB (1000h) boundary or above the 16kB (3FFFh) boundary so that it is unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

For non-page mode operations, off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip program memory access also occurs if the $\overline{EA}$ pin is logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when port 0 and port 2 fetch from external program memory.

The $\overline{RD}$ and $\overline{WR}$ signals are used to control the external data memory device. Data memory is accessed by MOVX instructions. The MOVX@Ri instruction uses the value in the designated working register to provide the LSB of the address, while port 2 supplies the address MSB. The MOVX@DPTR instruction uses one of the two data pointers to move data over the entire 64kB external data memory space. Software selects the data pointer to be used by writing to the SEL bit (DPS.0).

The DS89C420 also provides a user option for high-speed external memory access by reconfiguring the external memory interface into page mode operation.

Note: When using the original 8051 expanded bus structure, the throughput is reduced by 75% compared with that of internal operations. This is due to the CPU being stalled for three out of four clocks waiting for the data fetch, which takes four clocks. Page Mode 1 is the only external addressing mode where the CPU does not require stalls for external memory access, but page misses result in reduced external access performance.

ON-CHIP PROGRAM MEMORY

The processor can fetch the full on-chip program memory range automatically. The reset routines and all interrupt vectors are located in the lower 128 bytes of the on-chip program memory area.

On-chip program memory is logically divided into two 8kB flash memory banks and is designed to be programmed with the standard 5V V_{CC} supply by using a built-in program memory loader. It can also be programmed in standard flash or EPROM programmers. The DS89C420 incorporates a memory management unit (MMU) and other hardware to support any of the two programming methods. The MMU controls program and data memory access, and provides sequencing and timing controls for programming the on-chip program memory. There is also a separate security flash block that is used to support a standard three-level lock, a 64-byte encryption array, and other flash options.

SECURITY FEATURES

The DS89C420 incorporates a 64-byte encryption array, allowing the user to verify program codes while viewing the data in encrypted form. The encryption array is implemented in a security flash memory block that has the same electrical and timing characteristics as the on-chip program memory. Once the encryption array is programmed to non-FFh, the data presented in the verify mode is encrypted. Each byte of data is XNORed with a byte in the encryption array during verification.

A three-level lock restricts viewing of the internal program and data memory contents. By programming the three lock bits, the user can select a level of security as specified in Table 3. Once a security level is selected and programmed, the setting of the lock bits remains. Only a mass erase can erase these bits to allow reprogramming the security level to a less restricted protection.

Table 3. Flash Memory Lock Bits

LEVEL	LB1	LB2	LB3	PROTECTION
1	1	1	1	No program lock. Encrypted verify if encryption array is programmed.
2	0	1	1	Prevent MOVC in external memory from reading program code in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further parallel or program memory loader programming.
3	X	0	1	Level 2 plus no verify operation. Also prevent MOVX in external memory from reading internal SRAM.
4	X	X	0	Level 3 plus no external execution.

The DS89C420 provides user-selectable options that must be set before beginning software execution. The option control register uses flash bits rather than SFRs, and is individually erasable and programmable as a byte-wide register. Bit 3 of this register is defined as the watchdog POR default. Setting this bit to 1 disables the watchdog-reset function on power-up, and clearing this bit to 0 enables the watchdog-reset function automatically. Other bits of this register are undefined and are at logic 1 when read. The value of this register can be read at address FCh in parallel programming mode or when executing a verify-option control-register instruction in ROM loader mode.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information about manufacturer, part, and extension as follows:

ADDRESS VALUE	FUNCTION
30h DAh	Manufacturer ID
31h 42h	DS89C420 Device ID
60h 01h	Device Extension

ROM LOADER

The full 16kB of on-chip flash program-memory space, security flash block, and external SRAM can be programmed in-system from an external source through serial port 0 under the control of a built-in ROM loader. The ROM loader also has an auto-baud feature that determines which baud rate frequencies are being used for communication and sets up the baud rate generator for communication at that frequency.

When the DS89C420 is powered up and has entered its user operating mode, the ROM loader mode can be invoked at any time by forcing RST = 1, $\overline{EA}$ = 0, and $\overline{PSEN}$ = 0. It remains in effect until power-down or when the condition (RST = 1 and $\overline{PSEN}$ = $\overline{EA}$ = 0) is removed. Entering the ROM loader mode forces the processor to start fetching from the 2kB internal ROM for program memory initialization and other loader functions.

The read/write accessibility is determined by the state of the lock bits, which can be verified directly by the ROM loader. In the ROM loader mode, a mass-erase operation also erases the memory bank select and sets it to the default state. Otherwise, the memory bank select cannot be altered in the ROM loader mode.

Flash programming is executed by a series of internal flash commands that are derived (by the built-in ROM loader) from data transmitted over the serial interface from a host PC. PC-based software tools that configure and load the microcontrollers are available at www.maxim-ic.com/micros/ftpinfo.html.

Full details of the ROM loader software and its implementation are given in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

Table 4. Parallel Programming Instruction Set

INSTRUCTION	P2.5:0, P1.7:0	P0.7:0	$\overline{PROG}$	P2.6	P2.7	P3.6	P3.7	OPERATION
Mass Erase	Don't care	Don't care	PL[1]	H	L	L	L	Mass erase the 16k x 8 program memory, the security block and the bank select. The contents of every memory location is returned to FFh.
Write Program Memory	ADDR	DIN	PL[3]	L	H	H	H	Program the 16k program memory.
Read Program Memory	ADDR	DOUT	H[4]	L	L	H	H	Verify the 16k program memory.
Write Encryption Array	ADDR	DIN	PL[3]	L	H	L	H	Program the 64 byte encryption array.
Write LB1	Don't care	Don't care	PL[3]	H	H	H	H	Program LB1 to logic 0.
Write LB2	Don't care	Don't care	PL[3]	H	H	L	L	Program LB2 and LB1 to 00b.
Write LB3	Don't care	Don't care	PL[3]	H	L	H	L	Program LB3, LB2, and LB1 to 000b.
Read Lock Bits	Don't care	DOUT	H[4]	L	L	L	H	Verify the lock bits. The lock bits are at address 40h and the three LSBs of the DOUT are the logic value of the lock bits LB3, LB2, and LB1, respectively.
Write Option Control Register	Don't care	DIN	PL[3]	L	H	L	L	Program the option control register. Bit 3 of the DIN represents the watchdog POR default setting.
Erase Option Control Register	Don't care	Don't care	PL[2]	H	L	L	H	Erase the option control register. This operation disables the watch-dog reset function on power-up.
Read Address 30, 31, 60, FC	ADDR	DOUT	H[4]	L	L	L	L	30h = Manufacturer ID 31h = Device ID 60h = Device extension FCh = Verify the option control register. Bit 3 of the DOUT is the logic value of the watchdog POR.

[1] Mass erase requires an active-low $\overline{PROG}$ pulse width of 828ms.
[2] Erase option control register requires an active-low $\overline{PROG}$ pulse width of 828ms.
[3] Byte program requires an active-low $\overline{PROG}$ pulse width of 100µs max.
[4] $\overline{PROG}$ is weakly pulled to a high internally.

Note 1: P3.2 is pulled low during programming to indicate Busy. P3.2 is pulled high again when programming is completed to indicate Ready.
Note 2: P3.0 is pulled high during programming to indicate an error.

DATA POINTER INCREMENT/DECREMENT AND OPTIONS

The DS89C420 incorporates a hardware feature to assist applications that require data pointer increment/decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	Increment DPTR	Increment DPTR1
0	1	Decrement DPTR	Increment DPTR1
1	0	Increment DPTR	Decrement DPTR1
1	1	Decrement DPTR	Decrement DPTR1

PAGE MODE, EXTERNAL MEMORY CYCLE

Page mode retains the basic circuitry requirement for original 8051 external memory interface, but alters the configuration of P0 and P2 for the purposes of address output and data I/O during external memory cycles. Additionally, the functions of ALE and $\overline{PSEN}$ are altered to support this mode of operation.

Setting the PAGEE (ACON.7) bit to logic 1 enables page mode. Clearing the PAGEE bit to a logic 0 disables the page mode and the external bus structure defaults to the original 8051 expanded bus configuration (non-page mode). The DS89C420 supports page mode in two external bus structures. The logic value of the page mode select bits in the ACON register determines the external bus structure and the basic memory cycle in the number of system clocks. Table 6 summarizes this option. The first three selections use the same bus structure but with a different memory cycle time. Setting the select bits to 11b selects another bus structure. Write access to the ACON register requires a timed access.

Table 6. Page Mode Select

PAGES1:PAGES0	CLOCKS PER MEMORY CYCLE		EXTERNAL BUS STRUCTURE
	PAGE HIT	PAGE MISS	
00	1	2	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of the address.
01	2	4	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of the address.
10	4	8	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of the address.
11	2	4	P0: Lower address byte. P2: The upper address byte is multiplexed with the data byte. **Note:** This setting affects external code fetches only; accessing the external data memory requires 4 clock cycles, regardless of page hit or miss.

The first page mode (page mode 1) external bus structure uses P2 as the primary address bus, (multiplexing both the most significant byte (MSB) and least significant byte (LSB) of the address for each external memory cycle) and P0 is used as the primary data bus. During external code fetches, P0 is held in a high-impedance state by the processor. Op codes are driven by the external memory onto P0 and latched at the end of the external fetch cycle at the rising edge of $\overline{PSEN}$. During external data read/write operations, P0 functions as the data I/O bus. It is held in a high-impedance state for external reads from data memory, and driven with data during external writes to data memory.

- A page miss occurs when the MSB of the subsequent address is different from the last address. The external memory machine cycle can be 2, 4, or 8 system clocks in length for a page miss.
- A page hit occurs when the MSB of the subsequent address does not change from the last address. The external memory machine cycle can be 1, 2, or 4 system clocks in length for a page hit.

During a page hit, P2 drives Addr0–7 of the 16-bit address while the most significant address byte is held in the external address latches. $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ strobe accordingly for the appropriate operation on the P0 data bus. There is no ALE assertion for page hits.

During a page miss, P2 drives the Addr [8:15] of the 16-bit address and holds it for the duration of the first half of the memory cycle to allow the external address latches to latch the new most significant address byte. ALE is asserted to strobe the external address latches. During this operation, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ are held in inactive states and P0 is in a high-impedance state. The second half of the memory cycle is executed as a page-hit cycle and the appropriate operation takes place.

A page miss can occur at set intervals or during external operations that require a memory access into a page of memory that has not been accessed during the last external cycle. Generally, the first external memory access causes a page miss. The new page address is stored internally, and is used to detect a page miss for the current external memory cycle.

Figure 11. Page Mode 1, External Memory Cycle (CD1:CD0 = 10)

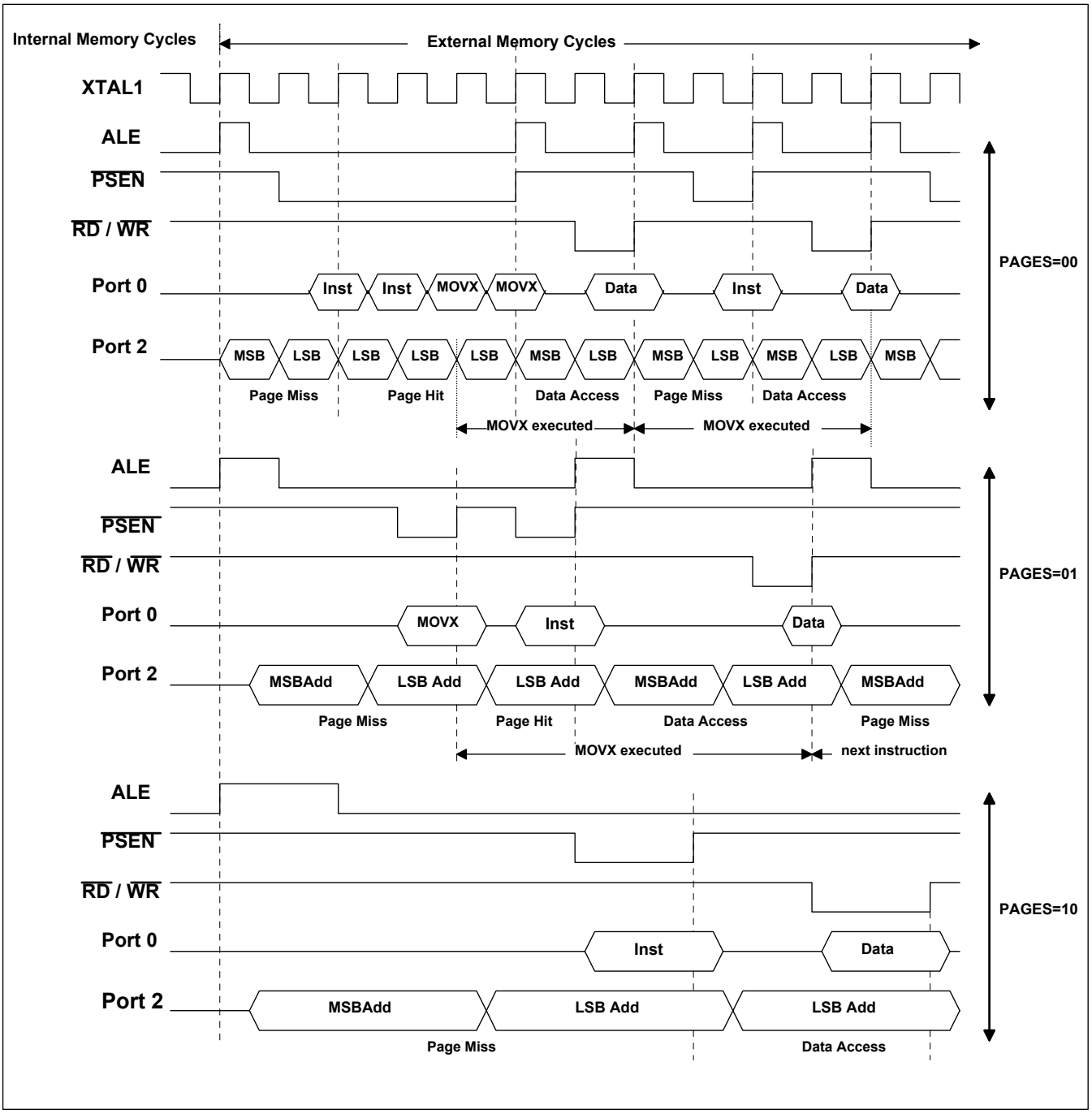


Table 9. Page Mode 1, Data Memory Cycle Stretch Values (Pages1:Pages0 = 10)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

Table 10. Page Mode 2, Data Memory Cycle Stretch Values (Pages1:Pages0 = 11)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

As shown in the previous tables, the stretch feature supports eight stretched external data-memory access cycles that can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data-memory access and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch memory cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the control signals. This is because the first stretch uses one system clock to create additional address setup and data bus float time, and one system clock to create additional address and data hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, two stretch cycles are used to create additional setup (the ALE pulse width is also stretched by one stretch cycle for page miss) and one stretch cycle is used to create additional hold time. The following timing diagrams illustrate the external data-memory access at divide-by-1 system clock mode (CD1:CD0 = 10b).

timer/counters without auto-reload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The timer mode (TMOD) register controls the operation mode. Each timer consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. The timer control (TCON) register enables Timers 0 and 1.

Table 12. Timer Functions

FUNCTIONS	TIMER 0	TIMER 1	TIMER 2
Timer/Counter	13/16/8*/2 x 8 bit	13/16/8* bit	16 bit
Timer with Capture	No	No	Yes
External Control-Pulse Counter	Yes	Yes	No
Up/Down Auto-Reload Timer/Counter	No	No	Yes
Baud Rate Generator	No	Yes	Yes
Timer-Output Clock Generator	No	No	Yes

**8-bit timer/counter includes auto-reload feature; 2- x 8-bit mode does not.*

Timer 2 is a true 16-bit timer/counter that, with a 16-bit capture (RCAP2L and RCAP2H) register, is able to provide some unique functions like up/down auto-reload timer/counter and timer-output clock generation. Timer 2 (registers TL2 and TH2) is enabled by the T2CON register, and its mode of operation is selected by the T2MOD register.

Each timer has a selectable time base (Table 14). Following a reset, the timers default to divide-by-12 to maintain drop-in compatible with the 8051. If Timer 2 is used as a baud rate generator or clock output, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

For details of operation, refer to “Programmable Timers” in the *Ultra-High-Speed Flash Microcontroller User’s Guide*.

TIMED ACCESS

The timed access function provides control verification to system functions. The timed access function prevents an errant CPU from making accidental changes to certain SFR bits that are considered vital to proper system operation. This is achieved by using software control when accessing the following SFR control bits:

WDCON.0	RWT	Reset Watchdog Timer
WDCON.1	EWT	Watchdog Reset Enable
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.6	POR	Power-On Reset Flag
EXIF.0	BGS	Bandgap Select
ACON.5	PAGES0	Page Mode Select Bit 0
ACON.6	PAGES1	Page Mode Select Bit 1
ACON.7	PAGEE	Page Mode Enable
ROMSIZE.0	RMS0	Program Memory Size Select Bit 0
ROMSIZE.1	RMS1	Program Memory Size Select Bit 1
ROMSIZE.2	RMS2	Program Memory Size Select Bit 2
ROMSIZE.3	PRAME	Program RAM Enable
FCNTL.0	FC0	Flash Command Bit 0
FCNTL.1	FC1	Flash Command Bit 1
FCNTL.2	FC2	Flash Command Bit 2
FCNTL.3	FC3	Flash Command Bit 3

Before these bits can be altered, the processor must execute the timed access sequence. This sequence consists of writing an AAh to the timed access (TA, C7h) register, followed by writing a 55h to the same register within three machine cycles. This timed sequence of steps then allows any of the timed-access-protected SFR bits to be altered during the three machine cycles, following the writing of the 55h. Writing to a timed access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address-, data-, and time-dependent. A processor running out of control and not executing system software cannot statistically perform this timed sequence of steps, and as such, will not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. It is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

POWER MANAGEMENT AND CLOCK-DIVIDE CONTROL

The DS89C420 incorporates power management features that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h), and power control (PCON, 87h) registers.

SYSTEM CLOCK-DIVIDE CONTROL

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and also to slow the system clocks providing lower power operation when required. An on-chip crystal multiplier allows the DS89C420 to operate at two or four times the crystal frequency by setting the 4X/$\overline{2X}$ bit and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide-by-1024. When used with a 7.372MHz crystal, for example, the processor executes machine cycle in times ranging from 33.9ns (divide-by-0.25) to 138.9µs (multiply-by-1024), and maintains a highly accurate serial port baud rate while allowing the use of more cost-effective, lower-frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features have been provided to enhance the use of these clock controls to guarantee proper serial port operation, and also to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved, and has the same effect as the 10b setting, which forces the system clock into a divide by 1 mode. The DS89C420 defaults to divide-by-1 clock mode on all forms of reset.

When programmed to the divide-by-1024 mode, and the switchback bit (PMR.5:SWB) is also set, the system forces the clock-divide control bits to reset automatically to the divide-by-1 mode whenever the system has detected externally enabled interrupts.

The oscillator divide ratios of 0.25, 0.5, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH, TxM = 00b, x = 1, 2, or 3) to the timers.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled during divide-by-1024 mode, and all other clock modes are unaffected by interrupts and serial port activity. See *Power Management Mode* for more details.

Use of the divide-by-0.25 or 0.5 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the 4X/$\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The 4X/$\overline{2X}$ bit can only be altered when the CTM bit is cleared to logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled through the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to logic 0 on all resets. Figure 15 gives a

OSCILLATOR-FAIL DETECT

The DS89C420 incorporates an oscillator fail-detect circuit that, when enabled, causes a reset if the crystal oscillator frequency falls below 20kHz and holds the chip in reset with the ring oscillator operating. Setting the OFDE (PCON.4) bit to logic 1 enables the circuit. The OFDE bit is only cleared from logic 1 to logic 0 by a power-fail reset or by software. A reset caused by an oscillator failure also sets the OFDF (PCON.5) to logic 1. This flag is cleared by software or power-on reset. Note that this circuit does not force a reset when the oscillator is stopped by the software-enabled stop mode.

POWER MANAGEMENT MODE

Power management mode offers a software-controllable power-saving scheme by providing a reduced instruction cycle speed, which allows the DS89C420 to continue to operate while using an internally divided version of the clock source to save power. Power management mode is invoked by software setting the clock-divide control bits CD1 and CD0 (PMR.7-6) bits to 11b, which sets an operating rate of 1024 oscillator cycles for 1 machine cycle. On all forms of reset, the clock-divide control bits default to 10b, which selects 1 oscillator cycle per machine cycle.

Since the clock speed choice affects all functional logic including timers, the DS89C420 implements several hardware switchback features that allow the clock speed to automatically return to the divide-by-1 mode from a reduced cycle rate. Setting the SWB (PMR.5) bit to a 1 in software enables this switchback function.

When CD1 and CD0 are programmed to the divide-by-1024 mode and the SWB bit is also enabled, the system forces the clock-divide control bits to automatically reset to the divide-by-1 mode whenever the system detects an externally enabled (and allowed through nesting priorities) interrupt. The switchback occurs whenever one of the two conditions occur. The first switchback condition is initiated by the detection of a low on either $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ or $\overline{\text{INT5}}$, or a high on INT2 or INT4 when the respective pin has been programmed and allowed (through nesting priorities) to issue an interrupt. The second switchback condition occurs when either serial port is enabled to receive data and is found to have an active-low transition on the respective receive input pin. Serial port transmit activity also forces a switchback if the SWB is set. Note that the serial port activity, as related to the switchback, is independent of the serial port interrupt relationship. Any attempt to change the clock divider to the divide-by-1024 mode while the serial port is either transmitting or receiving has no effect, leaving the clock control in the divide-by-1 mode. Note also that the switchback interrupt relationship requires that the respective external interrupt source is allowed to actually generate an interrupt as defined by the priority of the interrupt and the state of the nested interrupts, before the switchback can actually occur. An interrupt by the serial port is not required, nor is the setting of serial port enable. Disabling external interrupts and serial port receive/transmission mode disable the automatic switchback mode. Clearing the SWB bit also disables the switchback, and all interrupt and serial port controls of the clock divider are disabled. All other clock modes ignore the switchback relationship and are unaffected by interrupts and serial port activity.

The basic divide-by-12 mode for the timers (TxMH, TxM = 00b), as well as the divide-by-32 and 64 for mode 2 on the serial ports, are maintained when running the processor with the oscillator divide ratio of 0.25, 0.5, and 1. Serial ports and timers track the oscillator cycles per machine cycle when the higher divide ratio of 1024 is selected, and require the switchback function to automatically return to the divide-by-1 mode for proper operation when a qualified event occurs. Table 14 summarizes the effect of clock mode on timer operation.

It is possible to enable a receive function on a serial port when incoming data is not present and then change to the higher divide ratio. An inactive serial port receive/transmit mode requires the receive input pin to remain high and all outgoing transmissions to be completed. During this inactive receive mode it is possible to change the clock-divide control bits from a divide-by-1 to a 1024 divide ratio. In the case when the serial port is being used to receive or transmit data it is very important to validate an attempted change in the clock-divide control bits (read CD1 and CD0 to verify write was allowed) before proceeding with low-power program functions.

REVISION HISTORY

REVISION	DESCRIPTION
092200	Initial release
122601	Added errata (See www.maxim-ic.com/errata for details.)
042702	Official product introduction release
051302	Inserted AC Characteristics table
103102	Removed (Min Operating Voltage) from *DC Electrical Characteristics*; inserted diagram of ROM loader interface circuit
032003	Added 25MHz variant information
102203	Modified Figure 7 to support programmer-only operation.

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