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What is "Embedded - Microcontrollers"?

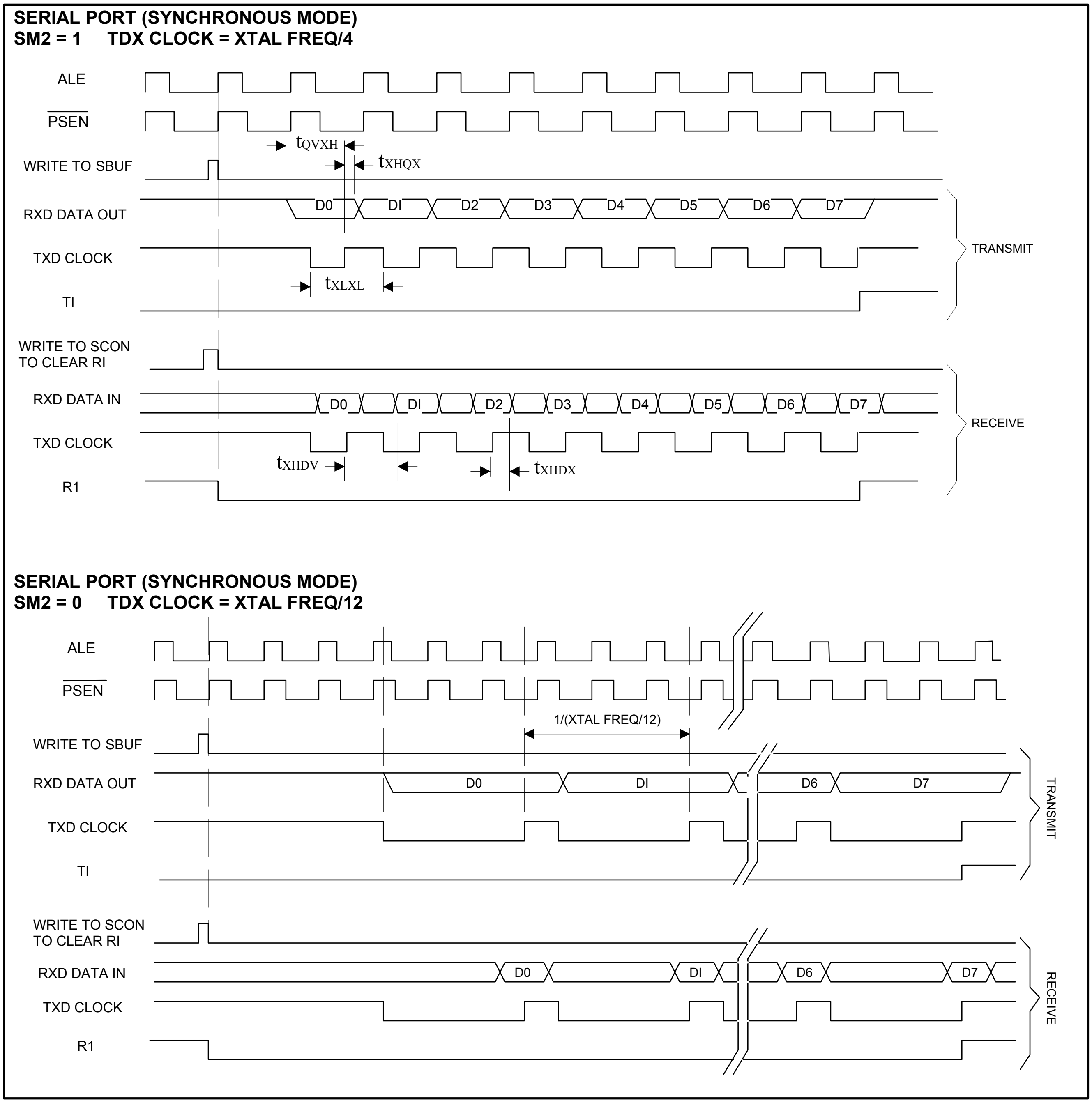
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c420-mnl

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: Active current is measured with a 25MHz/33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins disconnected.
Note 4: Idle mode current measured with a 25MHz/33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins disconnected.
Note 5: Stop mode measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins disconnected.
Note 6: When addressing external memory.
Note 7: RST = 5.5V. This condition mimics the operation of pins in I/O mode.
Note 8: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.
Note 9: Ports 1, 2, and 3 source transition current when being pulled down externally. The current reaches its maximum at approximately 2V.
Note 10: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.
Note 11: RST = 5.5V. Port 0 floating during reset and when in the logic-high state during I/O mode.
Note 12: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it such that this is not possible. Within the ranges given, there is a guaranteed separation between these two voltages.
Note 13: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.
Note 14: Guaranteed by design.

Figure 4. Serial Port Timing



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	12, 44	6, 38	V_{CC}	V_{CC} - +5V
20	1, 22, 23, 34	16, 17, 28, 39	GND	Logic Ground
9	10	4	RST	External Reset. The RST input pin is bidirectional and contains a Schmitt trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, since the device provides this function internally.
19	21	15	XTAL1	XTAL1, XTAL2. The crystal oscillator pins XTAL1 and XTAL2 provide support for fundamental mode parallel resonant, AT cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{\text{PSEN}}$	Program Store Enable. This signal is commonly connected to optional external program memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In 1-cycle page mode 1, $\overline{\text{PSEN}}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{\text{PROG}}$	Address Latch Enable. Functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{\text{PROG}}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	Port 0 (AD0–7), I/O. Port 0 is an open-drain 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of Port 0 is three-state. Pullup resistors are required when using Port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	
1–8	2–9	40–44, 1–3	P1.0–P1.7	Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of Port 1 are outlined below.

DIP	PLCC	TQFP	PORT	ALTERNATE	FUNCTION
1	2	40	P1.0	T2	External I/O for Timer/Counter 2
2	3	41	P1.1	T2EX	Timer 2 Capture/Reload Trigger
3	4	42	P1.2	RXD1	Serial Port 1 Receive
4	5	43	P1.3	TXD1	Serial Port 1 Transmit
5	6	44	P1.4	INT2	External Interrupt 2 (Positive Edge Detect)
6	7	1	P1.5	$\overline{\text{INT3}}$	External Interrupt 3 (Negative Edge Detect)
7	8	2	P1.6	INT4	External Interrupt 4 (Positive Edge Detect)
8	9	3	P1.7	$\overline{\text{INT5}}$	External Interrupt 5 (Negative Edge Detect)

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th colspan="3" rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>PDIP</th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td colspan="3" rowspan="8">Port 2 (A8–15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus; in page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2 (A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3 (A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4 (A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5 (A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6 (A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7 (A15)</td></tr>
<tr><td rowspan="2">10–17</td><td rowspan="2">11, 13–19</td><td rowspan="2">5, 7–13</td><td rowspan="2">P3.0–P3.7</td><td colspan="3">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.</td></tr>
<tr><th>PORT</th><th>ALTERNATE</th><th>FUNCTION</th></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Receive</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Transmit</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td colspan="3">External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C420 to use an external memory-program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

Table 1. Special Function Registers

REGISTER	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h	—	—	—	—	—	—	—	—
DPL	82h	—	—	—	—	—	—	—	—
DPH	83h	—	—	—	—	—	—	—	—
DPL1	84h	—	—	—	—	—	—	—	—
DPH1	85h	—	—	—	—	—	—	—	—
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah	—	—	—	—	—	—	—	—
TL1	8Bh	—	—	—	—	—	—	—	—
TH0	8Ch	—	—	—	—	—	—	—	—
TH1	8Dh	—	—	—	—	—	—	—	—
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{\text{INT5}}$	P1.6/INT4	P1.5/$\overline{\text{INT3}}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h	—	—	T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h	—	—	—	—	—	—	—	—
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h	—	—	—	—	—	—	—	—
SADDR1	AAh	—	—	—	—	—	—	—	—
P3	B0h	P3.7/$\overline{\text{RD}}$	P3.6/$\overline{\text{WR}}$	P3.5/T1	P3.4/T0	P3.3/$\overline{\text{INT1}}$	P3.2/$\overline{\text{INT0}}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h	—	—	—	—	—	—	—	—
SADEN1	BAh	—	—	—	—	—	—	—	—
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h	—	—	—	—	—	—	—	—
ROMSIZE	C2h	—	—	—	—	PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{\text{2X}}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h	—	—	—	—	—	—	—	—
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{\text{T2}}$	CP/$\overline{\text{RL2}}$
T2MOD	C9h	—	—	—	—	—	—	T2OE	DCEN
RCAP2L	CAh	—	—	—	—	—	—	—	—
RCAP2H	CBh	—	—	—	—	—	—	—	—
TL2	CCh	—	—	—	—	—	—	—	—
TH2	CDh	—	—	—	—	—	—	—	—
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{\text{FBUSY}}$	FERR	—	—	FC3	FC2	FC1	FC0
FDATA	D6h	—	—	—	—	—	—	—	—
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h	—	—	—	—	—	—	—	—
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h	—	—	—	—	—	—	—	—
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Table 2. SFR Reset Value

REGISTER	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

MEMORY ORGANIZATION

There are three distinct memory areas in the DS89C420: scratchpad registers, program memory, and data memory. All registers are located on-chip but the program and data memory spaces can either be on-chip, off-chip, or both. There are 16kB of on-chip program memory implemented in flash memory and 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C420 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different ways. If the maximum address of on-chip program or data memory is exceeded, the DS89C420 performs an external memory access using the expanded memory bus. The $\overline{\text{PSEN}}$ signal goes active-low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal for external MOVX data memory access. The lower 128 bytes of on-chip flash memory store reset and interrupt vectors. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C420 to act as a bootloader for an external flash or NV SRAM. It also enables the use of the overlapping external program spaces. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

REGISTER SPACE

Registers are located in the 256 bytes of on-chip RAM, which can be divided into two subareas of 128 bytes each as illustrated in Figure 6. Separate classes of instructions are used to access the registers and the program/data memory. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. Indirect addressing accesses the upper 128 bytes of scratchpad RAM, and direct addressing accesses the SFR area. Direct or indirect addressing can access the lower 128 bytes.

There are four banks of eight individual working registers in the lower 128 bytes of scratchpad RAM. The working registers are general-purpose RAM locations that can be addressed within the selected bank by any instructions that use R0–R7. The register bank selection is controlled through the program status register in the SFR area. The contents of the working registers can be used for indirectly addressing the upper 128 bytes of scratchpad RAM.

To support the Boolean operations, there are individually addressable bits in both the RAM and SFR areas. In the scratchpad RAM area, registers 20h–2Fh are bit-addressable by software using Boolean operation instructions.

Another use of the scratchpad RAM area is for the stack. The stack pointer in the SFRs is used to select storage locations for program variables and for return addresses of control operations.

MEMORY CONFIGURATION

As illustrated in Figure 6, the DS89C420 incorporates two 8kB flash memories for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of “alternate” program memory space. The DS89C420 uses an address scheme that separates program memory from data memory, such that the 16-bit address bus can address each memory area up to 64kB.

PROGRAM MEMORY ACCESS

On-chip program memory begins at address 0000h and is contiguous through 3FFFh (16kB). Exceeding the maximum address of on-chip program memory causes the device to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS89C420 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory is used. The maximum memory size is dynamically variable. Thus, a portion of memory can be removed from the memory map to access off-chip memory, then be restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. Program memory addresses that are larger than the selected maximum are automatically fetched from outside the part through ports 0 and 2 (Figure 6).

The ROMSIZE register is used to select the maximum on-chip decoded address for program memory. Bits RMS2, RMS1, RMS0 have the following effect:

RMS2	RMS1	RMS0 ADDRESS	MAXIMUM ON-CHIP PROGRAM MEMORY
0	0	0	0k
0	0	1	1k/03FFh
0	1	0	2k/07FFh
0	1	1	4k/0FFFh
1	0	0	8k/1FFFh
1	0	1	16k (default)/3FFFh
1	1	0	Invalid–Reserved
1	1	1	Invalid–Reserved

Table 3. Flash Memory Lock Bits

LEVEL	LB1	LB2	LB3	PROTECTION
1	1	1	1	No program lock. Encrypted verify if encryption array is programmed.
2	0	1	1	Prevent MOVC in external memory from reading program code in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further parallel or program memory loader programming.
3	X	0	1	Level 2 plus no verify operation. Also prevent MOVX in external memory from reading internal SRAM.
4	X	X	0	Level 3 plus no external execution.

The DS89C420 provides user-selectable options that must be set before beginning software execution. The option control register uses flash bits rather than SFRs, and is individually erasable and programmable as a byte-wide register. Bit 3 of this register is defined as the watchdog POR default. Setting this bit to 1 disables the watchdog-reset function on power-up, and clearing this bit to 0 enables the watchdog-reset function automatically. Other bits of this register are undefined and are at logic 1 when read. The value of this register can be read at address FCh in parallel programming mode or when executing a verify-option control-register instruction in ROM loader mode.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information about manufacturer, part, and extension as follows:

ADDRESS VALUE	FUNCTION
30h DAh	Manufacturer ID
31h 42h	DS89C420 Device ID
60h 01h	Device Extension

ROM LOADER

The full 16kB of on-chip flash program-memory space, security flash block, and external SRAM can be programmed in-system from an external source through serial port 0 under the control of a built-in ROM loader. The ROM loader also has an auto-baud feature that determines which baud rate frequencies are being used for communication and sets up the baud rate generator for communication at that frequency.

When the DS89C420 is powered up and has entered its user operating mode, the ROM loader mode can be invoked at any time by forcing RST = 1, $\overline{EA}$ = 0, and $\overline{PSEN}$ = 0. It remains in effect until power-down or when the condition (RST = 1 and $\overline{PSEN}$ = $\overline{EA}$ = 0) is removed. Entering the ROM loader mode forces the processor to start fetching from the 2kB internal ROM for program memory initialization and other loader functions.

The read/write accessibility is determined by the state of the lock bits, which can be verified directly by the ROM loader. In the ROM loader mode, a mass-erase operation also erases the memory bank select and sets it to the default state. Otherwise, the memory bank select cannot be altered in the ROM loader mode.

Flash programming is executed by a series of internal flash commands that are derived (by the built-in ROM loader) from data transmitted over the serial interface from a host PC. PC-based software tools that configure and load the microcontrollers are available at www.maxim-ic.com/micros/ftpinfo.html.

Full details of the ROM loader software and its implementation are given in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

Table 4. Parallel Programming Instruction Set

INSTRUCTION	P2.5:0, P1.7:0	P0.7:0	$\overline{PROG}$	P2.6	P2.7	P3.6	P3.7	OPERATION
Mass Erase	Don't care	Don't care	PL[1]	H	L	L	L	Mass erase the 16k x 8 program memory, the security block and the bank select. The contents of every memory location is returned to FFh.
Write Program Memory	ADDR	DIN	PL[3]	L	H	H	H	Program the 16k program memory.
Read Program Memory	ADDR	DOUT	H[4]	L	L	H	H	Verify the 16k program memory.
Write Encryption Array	ADDR	DIN	PL[3]	L	H	L	H	Program the 64 byte encryption array.
Write LB1	Don't care	Don't care	PL[3]	H	H	H	H	Program LB1 to logic 0.
Write LB2	Don't care	Don't care	PL[3]	H	H	L	L	Program LB2 and LB1 to 00b.
Write LB3	Don't care	Don't care	PL[3]	H	L	H	L	Program LB3, LB2, and LB1 to 000b.
Read Lock Bits	Don't care	DOUT	H[4]	L	L	L	H	Verify the lock bits. The lock bits are at address 40h and the three LSBs of the DOUT are the logic value of the lock bits LB3, LB2, and LB1, respectively.
Write Option Control Register	Don't care	DIN	PL[3]	L	H	L	L	Program the option control register. Bit 3 of the DIN represents the watchdog POR default setting.
Erase Option Control Register	Don't care	Don't care	PL[2]	H	L	L	H	Erase the option control register. This operation disables the watch-dog reset function on power-up.
Read Address 30, 31, 60, FC	ADDR	DOUT	H[4]	L	L	L	L	30h = Manufacturer ID 31h = Device ID 60h = Device extension FCh = Verify the option control register. Bit 3 of the DOUT is the logic value of the watchdog POR.

1) Mass erase requires an active-low $\overline{PROG}$ pulse width of 828ms.
2) Erase option control register requires an active-low $\overline{PROG}$ pulse width of 828ms.
3) Byte program requires an active-low $\overline{PROG}$ pulse width of 100µs max.
4) $\overline{PROG}$ is weakly pulled to a high internally.

Note 1: P3.2 is pulled low during programming to indicate Busy. P3.2 is pulled high again when programming is completed to indicate Ready.
Note 2: P3.0 is pulled high during programming to indicate an error.

DATA POINTER INCREMENT/DECREMENT AND OPTIONS

The DS89C420 incorporates a hardware feature to assist applications that require data pointer increment/decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	Increment DPTR	Increment DPTR1
0	1	Decrement DPTR	Increment DPTR1
1	0	Increment DPTR	Decrement DPTR1
1	1	Decrement DPTR	Decrement DPTR1

The SEL (DPS.0) bit always selects the active data pointer. The DS89C420 offers a programmable option that allows any instructions related to data pointer to toggle the SEL bit automatically. This option is enabled by setting the toggle-select-enable bit (TSL-DPS.5) to logic 1. Once enabled, the SEL bit is automatically toggled after the execution of one of the following five DPTR-related instructions:

```
INC DPTR
MOV DPTR #data16
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

The DS89C420 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 after the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent upon the setting of the ID1 and ID0 bits. This option is enabled by setting the automatic increment/decrement enable (AID-DPS.4) to a logic 1 and is affected by one of the following three instructions:

```
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

EXTERNAL MEMORY

The DS89C420 executes external memory cycles for code fetches and read/writes of external program and data memory. A non-page external memory cycle is four times slower than the internal memory cycles (i.e., an external memory cycle contains four system clocks). For this reason, although a DS89C420 can be substituted for a ROM-less 8051 device (DS80C310, C320, etc.), there is no increase in execution speed.

However, a page mode external memory cycle can be completed in 1, 2, or 4 system clocks for a page hit and 2, 4, or 8 system clocks for a page miss, depending on user selection. The DS89C420 also supports a second page mode operation with a different external bus structure that provides for fast external code fetches but uses 4 system clock cycles for data memory access.

EXTERNAL PROGRAM MEMORY INTERFACE (NON-PAGE MODE)

Figure 8 shows the timing relationship for internal and external code fetches when CD1 and CD0 are set to 10b, assuming the microcontroller is in non-page mode for external fetches. Note that an external program fetch takes 4 system clocks, and an internal program fetch requires only 1 system clock.

As illustrated in Figure 8, ALE is deasserted when executing an internal memory fetch. The DS89C420 provides a programmable user option to turn on ALE during internal program memory operation. ALE is automatically enabled for code fetch externally, independent of the setting of this option.

$\overline{\text{PSEN}}$ is only asserted for external code fetches, and is inactive during internal execution.

EXTERNAL DATA MEMORY INTERFACE IN NON-PAGE MODE OPERATION

Just like the program memory cycle, the external data memory cycle is four times slower than the internal data memory cycle in non-page mode. A basic internal memory cycle contains one system clock and a basic external memory cycle contains four system clocks for non-page mode operation.

The DS89C420 allows software to adjust the speed of external data memory access by stretching the memory bus cycle. CKCON (8Eh) provides an application-selectable stretch value for this purpose. Software can change the stretch value dynamically by changing the setting of CKCON.2–CKCON.0. Table 5 shows the data memory cycle stretch values and their effects on the external MOVX-memory bus cycle and the control signal pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks.

Figure 11. Page Mode 1, External Memory Cycle (CD1:CD0 = 10)

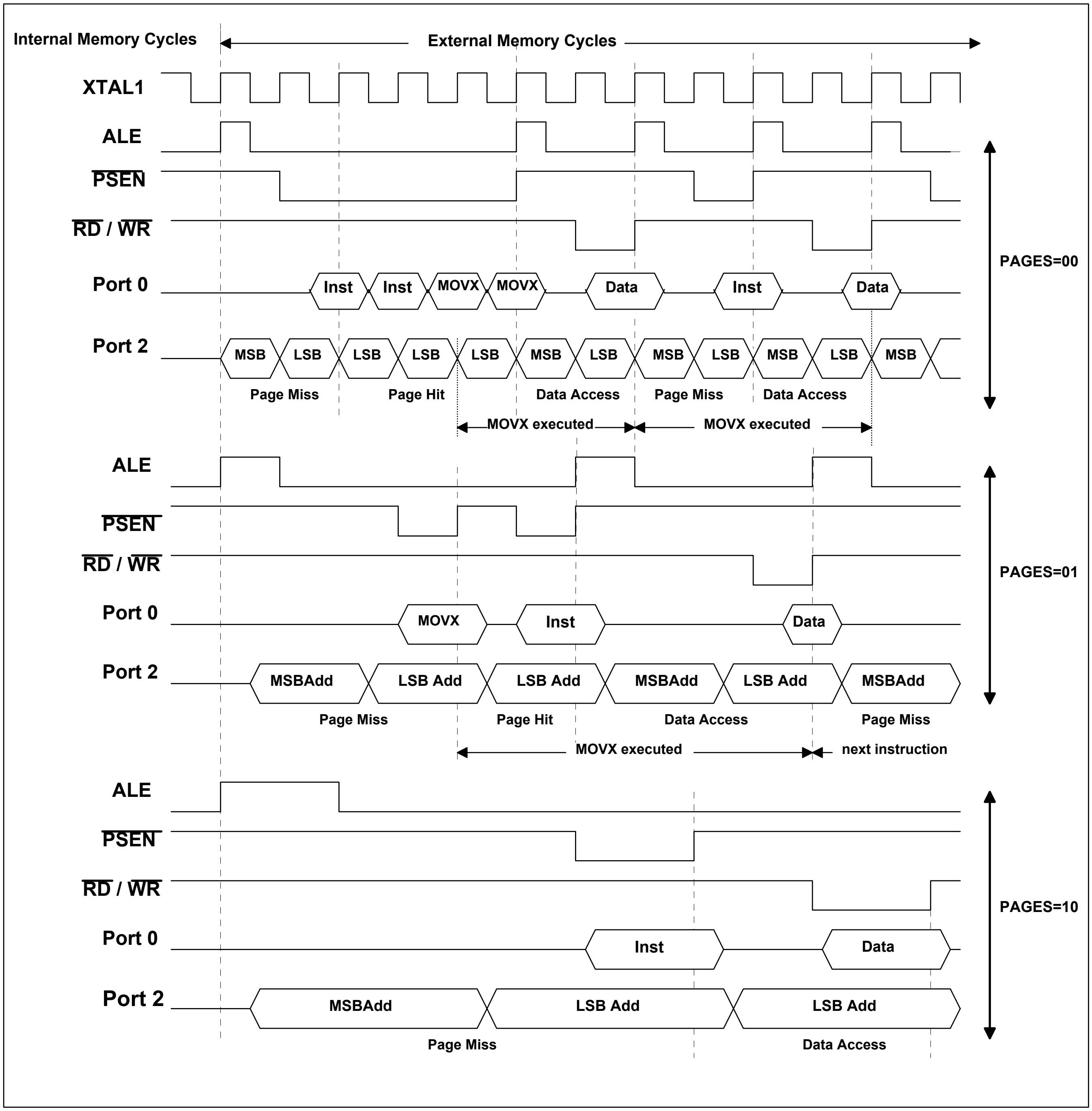


Figure 13. Page Mode 1, External Data Memory Access (Pages = 01, Stretch = 1, CD = 10)

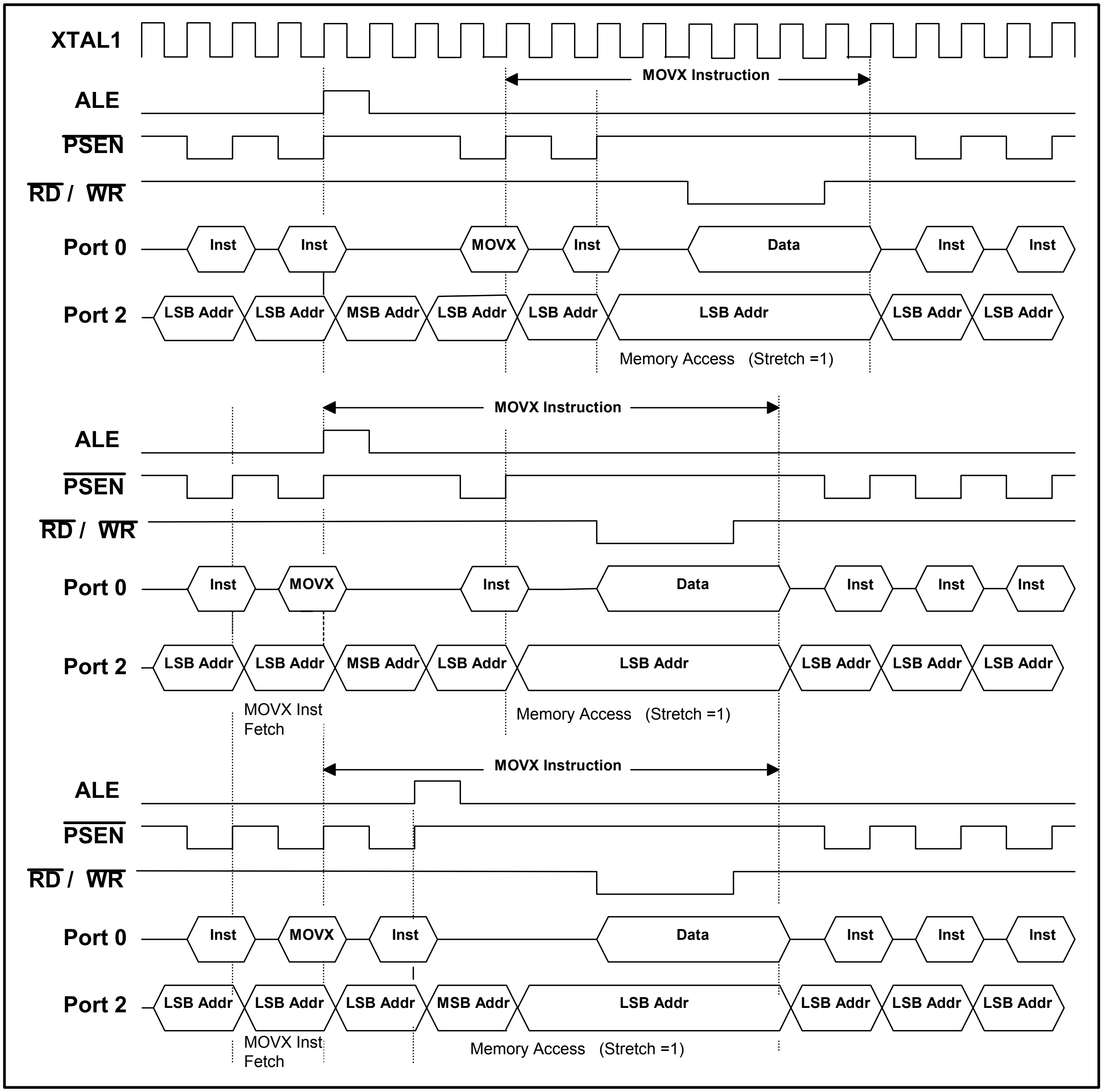


Figure 13 illustrates the external data-memory stretch cycle timing relationship when PAGEE = 1 and PAGES1:PAGES0 = 01. The stretch cycle shown is for a stretch value of 1 and is coincident with a page miss. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup and one system clock to create additional hold time.

Figure 14. Page Mode 1, External Data Memory Access (Pages = 01, Stretch = 4, CD = 10)

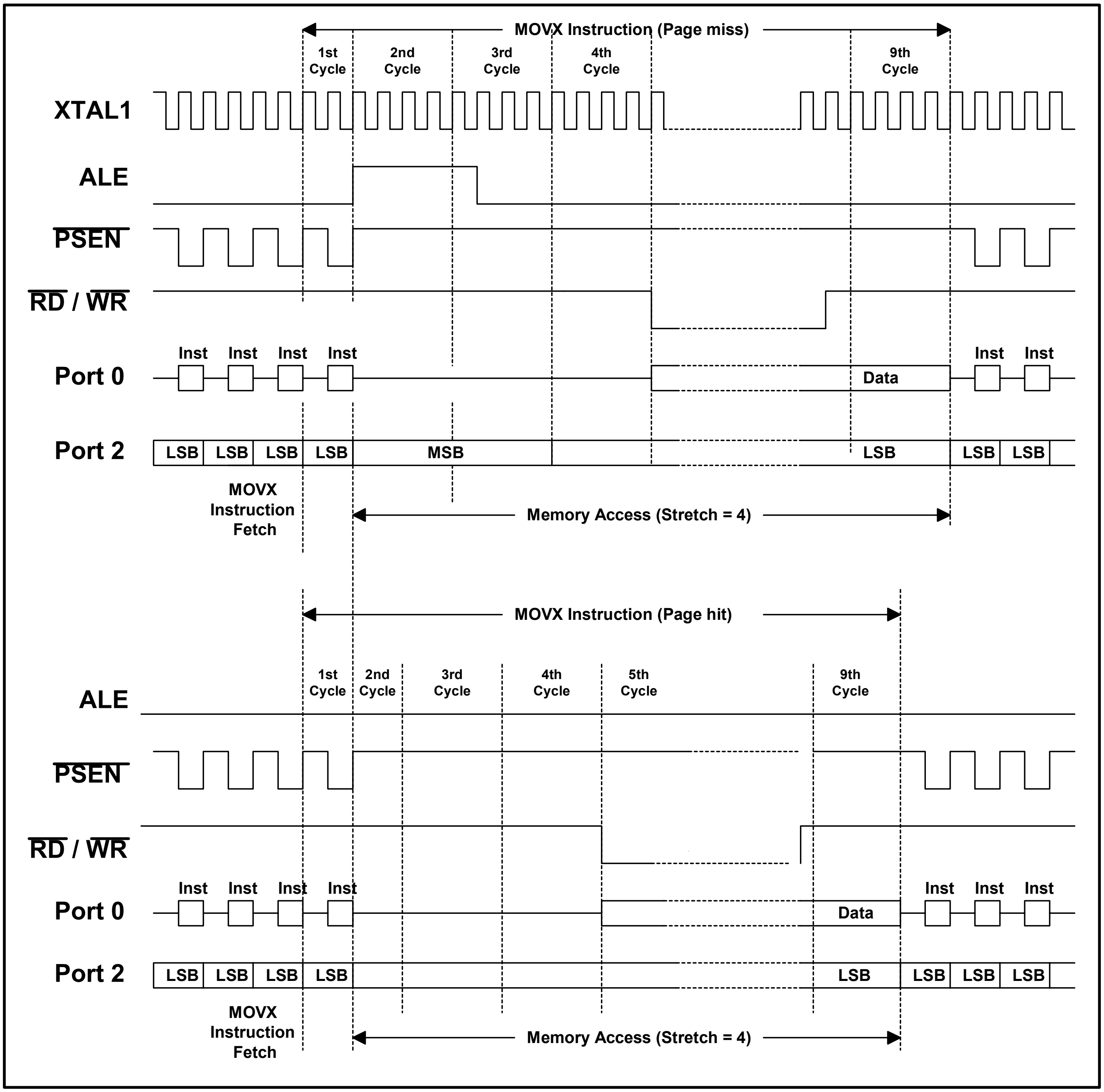


Figure 14 shows the timing relationship for a slow peripheral interface (stretch value = 4). Note that a page hit data-memory cycle is shorter than a page miss data-memory cycle. The ALE pulse width is also stretched by a stretch cycle in the case of page miss.

The stretched data-memory bus-cycle timing relationship for PAGES = 11 is identical to non-page mode operation since the basic data-memory cycle always contains four system clocks in this page mode operation.

INTERRUPTS

The DS89C420 provides 13 interrupt vector sources. All interrupts, with the exception of the power-fail, are controlled by a series combination of individual enable bits and a global enable (EA) in the interrupt enable register (IE.7). Setting $\overline{EA}$ to logic 1 allows individual interrupts to be enabled. Setting EA to a logic 0 disables all interrupts regardless of the individual interrupt enable settings. The power-fail interrupt is controlled by its individual enable only.

The interrupt enables and priorities are functionally identical to those of the 80C52, except that the DS89C420 supports five levels of interrupt priorities instead of the original two.

INTERRUPT PRIORITY

There are five levels of interrupt priority: level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power-Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1)**	EX0 (IE.0)	LPX0 (IP0.0) MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5)*	ET0 (IE.1)	LPT0 (IP0.1) MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3)**	EX1 (IE.2)	LPX1 (IP0.2) MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7)*	ET1 (IE.3)	LPT1 (IP0.3) MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4) MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7) EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5) MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0) TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6) MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0) MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1) MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2) MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3) MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4) MPWDI (EIP1.4)

**Cleared automatically by hardware when the service routine is vectored to.*
***If the interrupt is edge triggered, cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.*

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

TIMER/COUNTERS

Three 16-bit timers are incorporated in the DS89C420. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that count oscillator cycles. Table 12 summarizes the timer functions.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with auto-reload. Timer 0 has a fourth operating mode as two 8-bit timer/counters without auto-reload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The timer mode (TMOD) register controls the operation mode. Each timer consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. The timer control (TCON) register enables Timers 0 and 1.

Table 12. Timer Functions

FUNCTIONS	TIMER 0	TIMER 1	TIMER 2
Timer/Counter	13/16/8*/2 x 8 bit	13/16/8* bit	16 bit
Timer with Capture	No	No	Yes
External Control-Pulse Counter	Yes	Yes	No
Up/Down Auto-Reload Timer/Counter	No	No	Yes
Baud Rate Generator	No	Yes	Yes
Timer-Output Clock Generator	No	No	Yes

**8-bit timer/counter includes auto-reload feature; 2- x 8-bit mode does not.*

Timer 2 is a true 16-bit timer/counter that, with a 16-bit capture (RCAP2L and RCAP2H) register, is able to provide some unique functions like up/down auto-reload timer/counter and timer-output clock generation. Timer 2 (registers TL2 and TH2) is enabled by the T2CON register, and its mode of operation is selected by the T2MOD register.

Each timer has a selectable time base (Table 14). Following a reset, the timers default to divide-by-12 to maintain drop-in compatible with the 8051. If Timer 2 is used as a baud rate generator or clock output, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

For details of operation, refer to "Programmable Timers" in the *Ultra-High-Speed Flash Microcontroller User's Guide*.

TIMED ACCESS

The timed access function provides control verification to system functions. The timed access function prevents an errant CPU from making accidental changes to certain SFR bits that are considered vital to proper system operation. This is achieved by using software control when accessing the following SFR control bits:

WDCON.0	RWT	Reset Watchdog Timer
WDCON.1	EWT	Watchdog Reset Enable
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.6	POR	Power-On Reset Flag
EXIF.0	BGS	Bandgap Select
ACON.5	PAGES0	Page Mode Select Bit 0
ACON.6	PAGES1	Page Mode Select Bit 1
ACON.7	PAGEE	Page Mode Enable
ROMSIZE.0	RMS0	Program Memory Size Select Bit 0
ROMSIZE.1	RMS1	Program Memory Size Select Bit 1
ROMSIZE.2	RMS2	Program Memory Size Select Bit 2
ROMSIZE.3	PRAME	Program RAM Enable
FCNTL.0	FC0	Flash Command Bit 0
FCNTL.1	FC1	Flash Command Bit 1
FCNTL.2	FC2	Flash Command Bit 2
FCNTL.3	FC3	Flash Command Bit 3

Before these bits can be altered, the processor must execute the timed access sequence. This sequence consists of writing an AAh to the timed access (TA, C7h) register, followed by writing a 55h to the same register within three machine cycles. This timed sequence of steps then allows any of the timed-access-protected SFR bits to be altered during the three machine cycles, following the writing of the 55h. Writing to a timed access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address-, data-, and time-dependent. A processor running out of control and not executing system software cannot statistically perform this timed sequence of steps, and as such, will not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. It is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

POWER MANAGEMENT AND CLOCK-DIVIDE CONTROL

The DS89C420 incorporates power management features that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h), and power control (PCON, 87h) registers.

SYSTEM CLOCK-DIVIDE CONTROL

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and also to slow the system clocks providing lower power operation when required. An on-chip crystal multiplier allows the DS89C420 to operate at two or four times the crystal frequency by setting the $4X/\overline{2X}$ bit and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide-by-1024. When used with a 7.372MHz crystal, for example, the processor executes machine cycle in times ranging from 33.9ns (divide-by-0.25) to 138.9μs (multiply-by-1024), and maintains a highly accurate serial port baud rate while allowing the use of more cost-effective, lower-frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features have been provided to enhance the use of these clock controls to guarantee proper serial port operation, and also to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved, and has the same effect as the 10b setting, which forces the system clock into a divide by 1 mode. The DS89C420 defaults to divide-by-1 clock mode on all forms of reset.

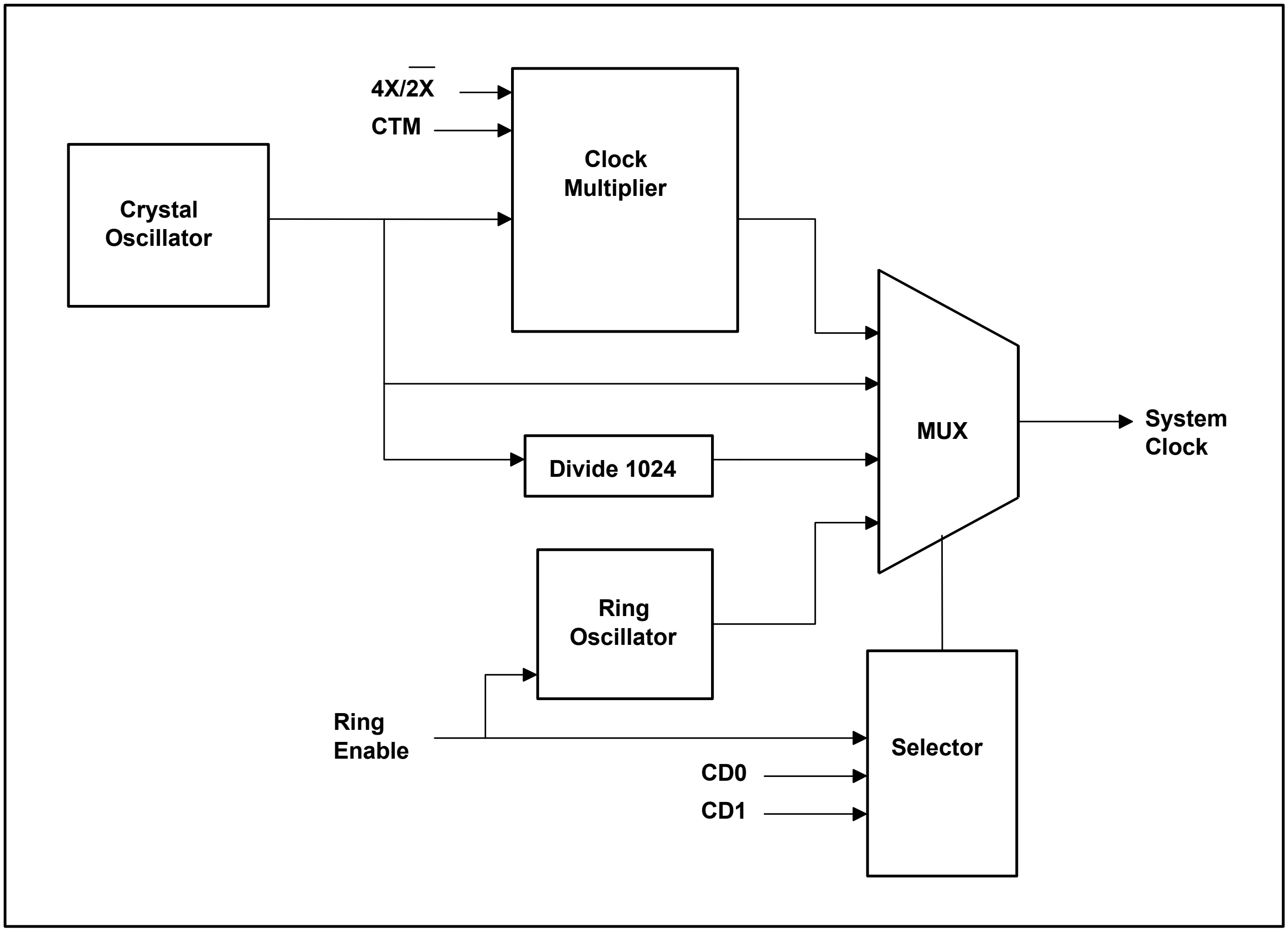
When programmed to the divide-by-1024 mode, and the switchback bit (PMR.5:SWB) is also set, the system forces the clock-divide control bits to reset automatically to the divide-by-1 mode whenever the system has detected externally enabled interrupts.

The oscillator divide ratios of 0.25, 0.5, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH, TxM = 00b, x = 1, 2, or 3) to the timers.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled during divide-by-1024 mode, and all other clock modes are unaffected by interrupts and serial port activity. See *Power Management Mode* for more details.

Use of the divide-by-0.25 or 0.5 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the $4X/\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The $4X/\overline{2X}$ bit can only be altered when the CTM bit is cleared to logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled through the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to logic 0 on all resets. Figure 15 gives a simplified diagram of the generation of the system clocks. Specifics of hardware restrictions associated with the use of the 4X/$\overline{2X}$ CTM, CKRY, CD1, and CD0 bits are outlined in the SFR description.

Figure 15. System Clock Sources



BANDGAP-MONITORED INTERRUPT AND RESET GENERATION

The power monitor in the DS89C420 monitors the V_{CC} pin in relation to the on-chip bandgap voltage reference. Whenever V_{CC} falls below V_{PFW}, an interrupt is generated if the corresponding power-fail interrupt-enable bit EPFI (WDCON.5) is set, causing the device to vector to address 33h. The power-fail interrupt-status bit PFI (WDCON.4) is set anytime V_{CC} transitions below V_{PFW}, and can only be cleared by software once set. Similarly, as V_{CC} falls below V_{RST}, a reset is issued internally to halt program execution. Following power-up, a power-on reset initiates a power-on reset timeout before starting program execution. When V_{CC} is first applied to the DS89C420, the processor is held in reset until $V_{CC} > V_{RST}$ and a delay of 65,536 oscillator cycles has elapsed, to ensure that power is within tolerance and the clock source has had time to stabilize. Once the reset timeout period has elapsed, the reset condition is removed automatically and software execution begins at the reset vector location of 0000h. The power-on reset flag POR (WDCON.6) is set to logic 1 to indicate a power-on reset has occurred, and can only be cleared by software.

When the DS89C420 enters stop mode, the bandgap, reset comparator, and power-fail interrupt comparator are automatically disabled to conserve power, if the BGS (EXIF.0) bit is set to a logic 0. This is the lowest power mode. If BGS is set to logic 1, the bandgap reference, reset comparator, and the power-fail comparator are powered up, although in a reduced fashion, while in stop mode.

OSCILLATOR-FAIL DETECT

The DS89C420 incorporates an oscillator fail-detect circuit that, when enabled, causes a reset if the crystal oscillator frequency falls below 20kHz and holds the chip in reset with the ring oscillator operating. Setting the OFDE (PCON.4) bit to logic 1 enables the circuit. The OFDE bit is only cleared from logic 1 to logic 0 by a power-fail reset or by software. A reset caused by an oscillator failure also sets the OFDF (PCON.5) to logic 1. This flag is cleared by software or power-on reset. Note that this circuit does not force a reset when the oscillator is stopped by the software-enabled stop mode.

POWER MANAGEMENT MODE

Power management mode offers a software-controllable power-saving scheme by providing a reduced instruction cycle speed, which allows the DS89C420 to continue to operate while using an internally divided version of the clock source to save power. Power management mode is invoked by software setting the clock-divide control bits CD1 and CD0 (PMR.7-6) bits to 11b, which sets an operating rate of 1024 oscillator cycles for 1 machine cycle. On all forms of reset, the clock-divide control bits default to 10b, which selects 1 oscillator cycle per machine cycle.

Since the clock speed choice affects all functional logic including timers, the DS89C420 implements several hardware switchback features that allow the clock speed to automatically return to the divide-by-1 mode from a reduced cycle rate. Setting the SWB (PMR.5) bit to a 1 in software enables this switchback function.

When CD1 and CD0 are programmed to the divide-by-1024 mode and the SWB bit is also enabled, the system forces the clock-divide control bits to automatically reset to the divide-by-1 mode whenever the system detects an externally enabled (and allowed through nesting priorities) interrupt. The switchback occurs whenever one of the two conditions occur. The first switchback condition is initiated by the detection of a low on either $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ or $\overline{\text{INT5}}$, or a high on INT2 or INT4 when the respective pin has been programmed and allowed (through nesting priorities) to issue an interrupt. The second switchback condition occurs when either serial port is enabled to receive data and is found to have an active-low transition on the respective receive input pin. Serial port transmit activity also forces a switchback if the SWB is set. Note that the serial port activity, as related to the switchback, is independent of the serial port interrupt relationship. Any attempt to change the clock divider to the divide-by-1024 mode while the serial port is either transmitting or receiving has no effect, leaving the clock control in the divide-by-1 mode. Note also that the switchback interrupt relationship requires that the respective external interrupt source is allowed to actually generate an interrupt as defined by the priority of the interrupt and the state of the nested interrupts, before the switchback can actually occur. An interrupt by the serial port is not required, nor is the setting of serial port enable. Disabling external interrupts and serial port receive/transmission mode disable the automatic switchback mode. Clearing the SWB bit also disables the switchback, and all interrupt and serial port controls of the clock divider are disabled. All other clock modes ignore the switchback relationship and are unaffected by interrupts and serial port activity.

The basic divide-by-12 mode for the timers (TxMH, TxM = 00b), as well as the divide-by-32 and 64 for mode 2 on the serial ports, are maintained when running the processor with the oscillator divide ratio of 0.25, 0.5, and 1. Serial ports and timers track the oscillator cycles per machine cycle when the higher divide ratio of 1024 is selected, and require the switchback function to automatically return to the divide-by-1 mode for proper operation when a qualified event occurs. Table 14 summarizes the effect of clock mode on timer operation.

It is possible to enable a receive function on a serial port when incoming data is not present and then change to the higher divide ratio. An inactive serial port receive/transmit mode requires the receive input pin to remain high and all outgoing transmissions to be completed. During this inactive receive mode it is possible to change the clock-divide control bits from a divide-by-1 to a 1024 divide ratio. In the case when the serial port is being used to receive or transmit data it is very important to validate an attempted change in the clock-divide control bits (read CD1 and CD0 to verify write was allowed) before proceeding with low-power program functions.

Table 14. Effect of Clock Mode on Timer Operation (in Number of Oscillator Clocks)

4X/2X, CD1, CD0	OSC. CYCLES PER MACHINE CYCLE	OSC. CYCLES PER TIMERS (0, 1, 2) CLOCK			OSC. CYCLES PER TIMER 2 CLOCK	OSC. CYCLES PER SERIAL PORT CLOCK MODE 0		OSC. CYCLES PER SERIAL PORT CLOCK MODE 2	
		TxMH, TxM = 00	01	1x	BAUD RATE GENERATOR T2MH, T2M = xx	SM2 = 0	SM2 = 1	SMOD = 0	SMOD = 1
100	0.25	12	1	0.25	2	3	1	64	32
000	0.5	12	2	0.5	2	6	2	64	32
x01	1 (reserved)	—			—	—		—	
x10	1 (default)	12	4	1	2	12	4	64	32
x11	1,024	12,288	4,096	1,024	2,048	12,288	4,096	65,536	32,768

x = don't care

RING OSCILLATOR

A ring oscillator, which typically runs at 10MHz, allows the processor to recover instantly from the stop mode.

When the system is in stop mode the crystal is disabled. When stop mode is removed, the crystal requires a period of time to start up and stabilize. To allow the system to begin immediate execution of software following the removal of the stop mode, the ring oscillator is used to supply a system clock until the crystal startup time is satisfied. Once this time has passed, the ring oscillator is switched off and the system clock is switched over to the crystal oscillator. This function is programmable and is enabled by setting the RGSL bit (EXIF.1) to logic 1. When it is logic 0, the processor delays software execution until after the 65,536 crystal clock periods. To allow the processor to know whether it is being clocked by the ring or the crystal oscillator, an additional bit, termed the RGMD bit, indicates which clock source is being used. When the processor is running from the ring, the clock-divide control bits (CD1 and CD0 in the PMR register) are locked into the divide-by-1 mode (CD1:CD0 = 10b). The clock-divide control bits cannot be changed from this state until after the system clock transitions to the crystal oscillator (RGMD = 0).

Note: The watchdog is permanently connected to the crystal oscillator and continues to run at the external clock rate. The ring oscillator does not drive it.

IDLE MODE

Idle mode suspends the processor by holding the program counter in a static state. No instructions are fetched and no processing occurs. Setting the IDLE bit (PCON.0) to logic 1 invokes idle mode. The instruction that executes this step is the last instruction prior to freezing the program counter. Once in Idle mode, all resources are preserved but all peripheral clocks remain active, and the timers, watchdog, serial ports, and power monitor functions continue to operate, so that the processor can exit the idle mode using any interrupt sources that are enabled. The oscillator-detect circuit also continues to function when enabled. The IDLE bit is cleared automatically once idle mode is exited. On returning from the interrupt vector using the RETI instruction, the next address is the one that immediately follows the instruction that invoked the idle mode. Any processor resets also remove the idle mode.

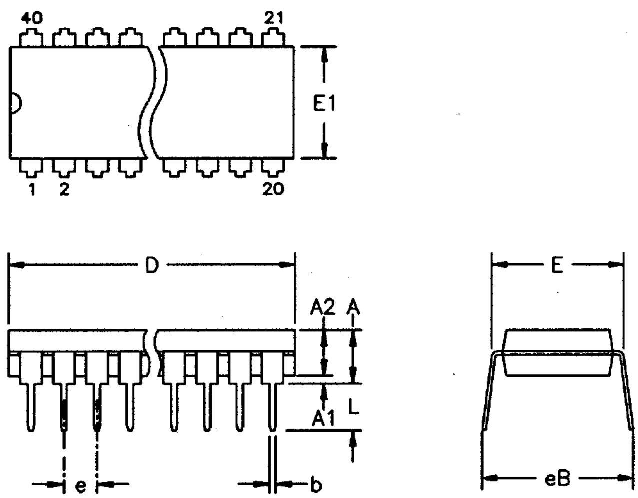
STOP MODE

The stop mode disables all circuits within the processor. All on-chip clocks, timers, and serial port communication are stopped, and no processing is possible.

Stop mode is invoked by setting the STOP bit (PCON.1) to logic 1. The processor enters the stop mode on the instruction that sets the bit. The processor can exit stop mode by using any of the six external interrupts that are enabled.

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



PKG	40-PIN	
DIM	**MIN**	**MAX**
A	—	0.200
A1	0.015	—
A2	0.140	0.160
b	0.014	0.022
c	0.008	0.012
D	1.980	2.085
E	0.600	0.625
E1	0.530	0.555
e	0.090	0.110
L	0.115	0.145
eB	0.600	0.700

56–G5000–000
Dimensions are in inches (in).