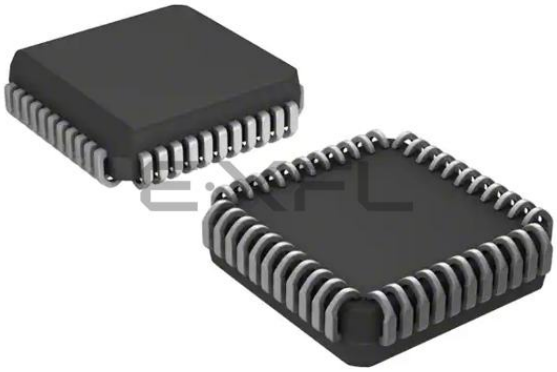

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c420-qng

Note 1: Specifications to -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: Active current is measured with a 25MHz/33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins disconnected.
Note 4: Idle mode current measured with a 25MHz/33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins disconnected.
Note 5: Stop mode measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins disconnected.
Note 6: When addressing external memory.
Note 7: RST = 5.5V. This condition mimics the operation of pins in I/O mode.
Note 8: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.
Note 9: Ports 1, 2, and 3 source transition current when being pulled down externally. The current reaches its maximum at approximately 2V.
Note 10: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.
Note 11: RST = 5.5V. Port 0 floating during reset and when in the logic-high state during I/O mode.
Note 12: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it such that this is not possible. Within the ranges given, there is a guaranteed separation between these two voltages.
Note 13: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.
Note 14: Guaranteed by design.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C)* (Figure 1, Figure 2, and Figure 3)

PARAMETER		SYMBOL	1 CYCLE PAGE MODE 1		2 CYCLE PAGE MODE 1		4 CYCLE PAGE MODE 1		PAGE MODE 2		NON-PAGE MODE		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
System Clock (Note 1)	External Oscillator (25MHz, 33MHz)	1 / t_{CLCL}	0	25	0	25	0	25	0	25	0	25	MHz
			0	33	0	33	0	33	0	33	0	33	
	External Crystal (25MHz, 33MHz)		1	25	1	25	1	25	1	25	1	25	
			1	33	1	33	1	33	1	33	1	33	
ALE Pulse Width (Note 2)		t_{LHLL}	$0.5t_{CLCL}$ - 2 + t_{STC3}		t_{CLCL} - 2 + t_{STC3}		$2t_{CLCL}$ - 4 + t_{STC3}		$1.5t_{CLCL}$ - 5 + t_{STC3}		$1.5t_{CLCL}$ - 5 + t_{STC3}		ns
Port 0 Instruction Address Valid to ALE Low		t_{AVLL}							t_{CLCL} - 2		$0.5t_{CLCL}$ - 2		ns
Port 2 Instruction Address Valid to ALE Low		t_{AVLL2}	$0.5t_{CLCL}$ - 4		$0.5t_{CLCL}$ - 4		$1.5t_{CLCL}$ - 5		$0.5t_{CLCL}$ - 2		t_{CLCL} - 2		ns
Port 0 Data AddressValid to ALE Low		t_{AVLL3}							t_{CLCL} - 2 + t_{STC3}		$0.5t_{CLCL}$ - 2 + t_{STC3}		ns
Program Address Hold After ALE Low		t_{LLAX}	$0.5t_{CLCL}$ - 8		$1.5t_{CLCL}$ - 8		$2.5t_{CLCL}$ - 8		$0.5t_{CLCL}$ - 8		$0.5t_{CLCL}$ - 8		ns
Address Hold After ALE Low MOVX Write		t_{LLAX2}	$0.5t_{CLCL}$ - 8 + t_{STC4}		$1.5t_{CLCL}$ - 8 + t_{STC4}		$2.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		ns
Address Hold After ALE Low MOVX Read		t_{LLAX3}	$0.5t_{CLCL}$ - 8 + t_{STC4}		$1.5t_{CLCL}$ - 8 + t_{STC4}		$2.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		$0.5t_{CLCL}$ - 8 + t_{STC4}		ns
ALE Low to Valid Instruction In		t_{LLIV}								$2.5t_{CLCL}$ - 20		$2.5t_{CLCL}$ - 20	ns
ALE Low to $\overline{PSEN}$ Low		t_{LLPL}							$1.5t_{CLCL}$ - 6		$0.5t_{CLCL}$ - 6		ns
$\overline{PSEN}$ Pulse Width for Program Fetch		t_{PLPH}	t_{CLCL} - 5		t_{CLCL} - 5		$2t_{CLCL}$ - 5		t_{CLCL} - 5		$2t_{CLCL}$ - 5		ns

EXTERNAL CLOCK CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)*

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V; T_A = -40°C to +85°C.)* (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	

Note: SM2 is the serial port 0, mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial-port clock cycle.

**Specifications to -40°C are guaranteed by design and not production tested.*

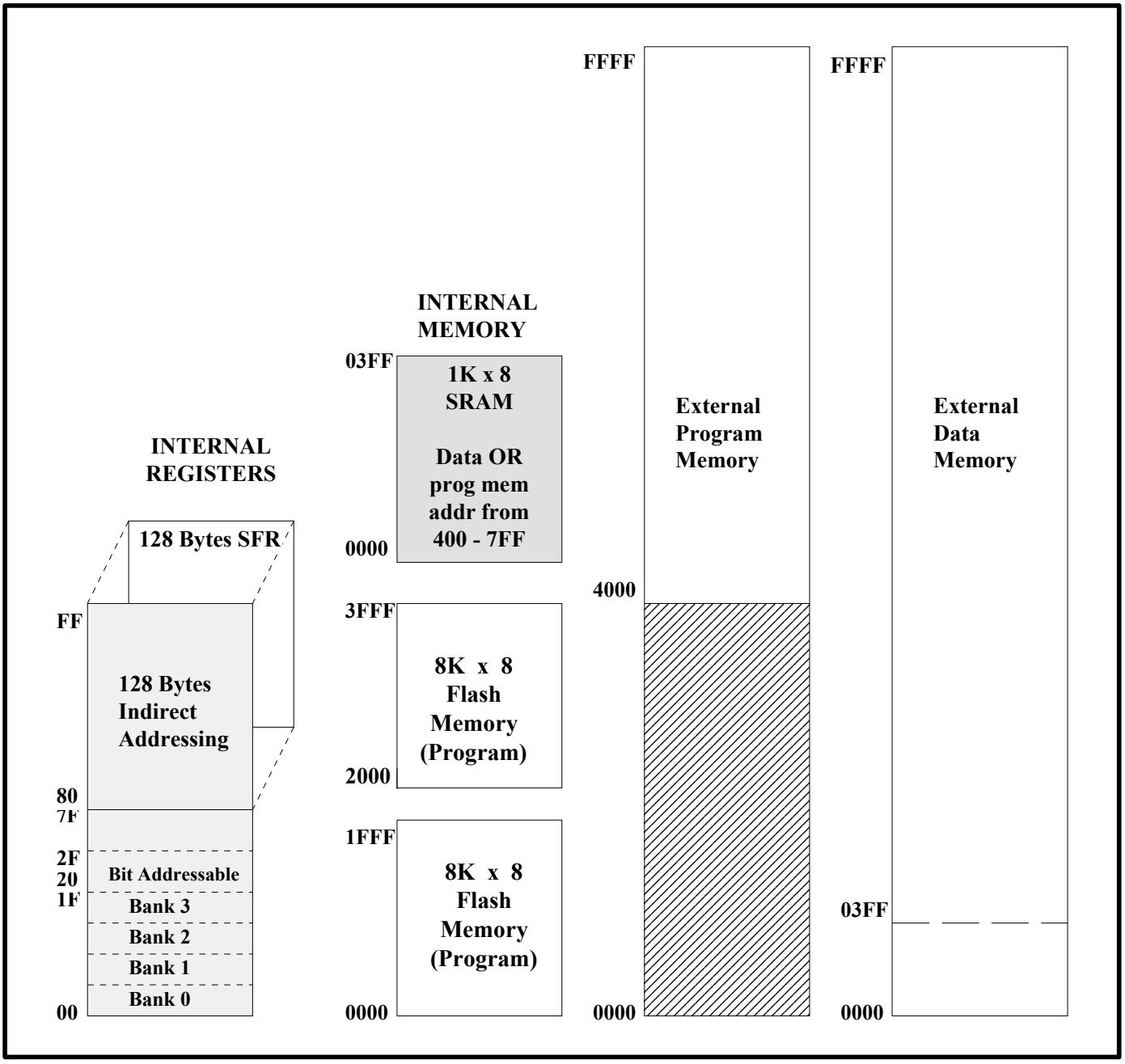
PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th colspan="3">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>PDIP</th><th></th><th></th><th></th></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td colspan="3" rowspan="8">Port 2 (A8–15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus; in page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2 (A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3 (A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4 (A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5 (A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6 (A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7 (A15)</td></tr>
<tr><td rowspan="2">10–17</td><td rowspan="2">11, 13–19</td><td rowspan="2">5, 7–13</td><td rowspan="2">P3.0–P3.7</td><td colspan="3">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C420 activates a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below.</td></tr>
<tr><td>PORT</td><td>ALTERNATE</td><td>FUNCTION</td></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td>P3.0</td><td>RXD0</td><td>Serial Port 0 Receive</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td><td>P3.1</td><td>TXD0</td><td>Serial Port 0 Transmit</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td><td>P3.4</td><td>T0</td><td>Timer 0 External Input</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td><td>P3.5</td><td>T1</td><td>Timer 1 External Input</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write Strobe</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read Strobe</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td colspan="3">External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C420 to use an external memory-program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

Table 1. Special Function Registers

REGISTER	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h	—	—	—	—	—	—	—	—
DPL	82h	—	—	—	—	—	—	—	—
DPH	83h	—	—	—	—	—	—	—	—
DPL1	84h	—	—	—	—	—	—	—	—
DPH1	85h	—	—	—	—	—	—	—	—
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah	—	—	—	—	—	—	—	—
TL1	8Bh	—	—	—	—	—	—	—	—
TH0	8Ch	—	—	—	—	—	—	—	—
TH1	8Dh	—	—	—	—	—	—	—	—
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{INT5}$	P1.6/INT4	P1.5/$\overline{INT3}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h	—	—	T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h	—	—	—	—	—	—	—	—
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h	—	—	—	—	—	—	—	—
SADDR1	AAh	—	—	—	—	—	—	—	—
P3	B0h	P3.7/$\overline{RD}$	P3.6/$\overline{WR}$	P3.5/T1	P3.4/T0	P3.3/$\overline{INT1}$	P3.2/$\overline{INT0}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h	—	—	—	—	—	—	—	—
SADEN1	BAh	—	—	—	—	—	—	—	—
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h	—	—	—	—	—	—	—	—
ROMSIZE	C2h	—	—	—	—	PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h	—	—	—	—	—	—	—	—
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h	—	—	—	—	—	—	T2OE	DCEN
RCAP2L	CAh	—	—	—	—	—	—	—	—
RCAP2H	CBh	—	—	—	—	—	—	—	—
TL2	CCh	—	—	—	—	—	—	—	—
TH2	CDh	—	—	—	—	—	—	—	—
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{FBUSY}$	FERR	—	—	FC3	FC2	FC1	FC0
FDATA	D6h	—	—	—	—	—	—	—	—
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h	—	—	—	—	—	—	—	—
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h	—	—	—	—	—	—	—	—
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

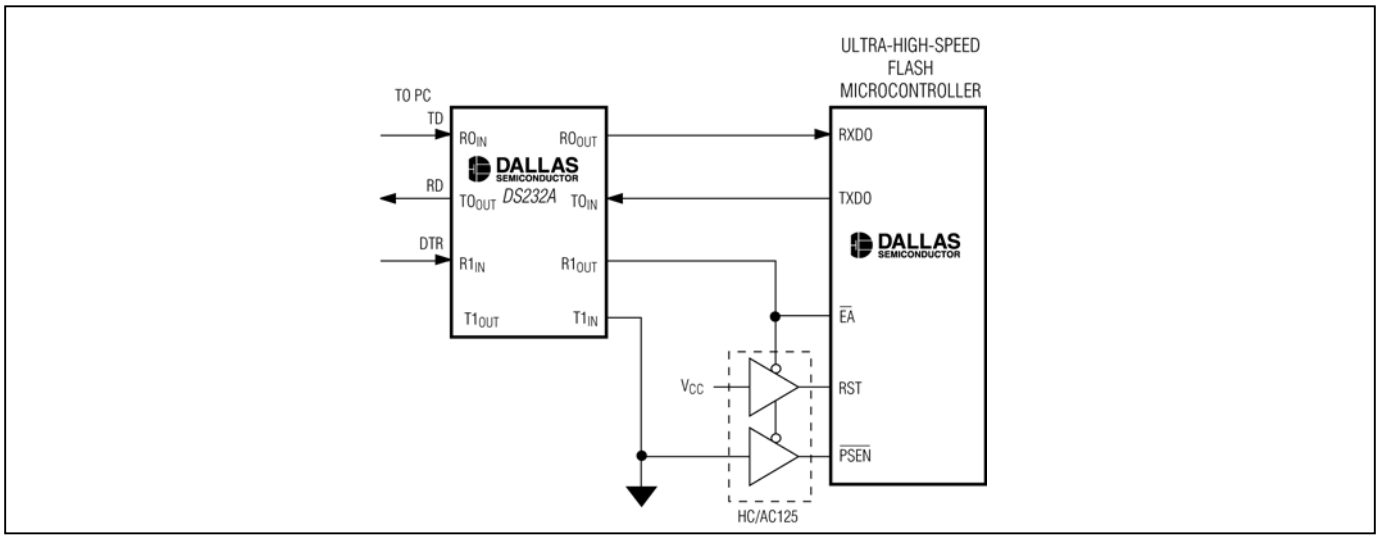
Figure 6. Memory Map



The reset default condition is a maximum on-chip program-memory address of 16kB. When accessing external program memory, the first 16kB would be inaccessible. To select a smaller effective program memory size, software must alter bits RMS2–RMS0. Altering these bits requires a timed access procedure as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that a DS89C420 is executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device immediately jumps to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that is internal (or external) both before and after the operation. In the above example, the instruction that modifies the ROMSIZE register should be located below the

Figure 7. Interfacing the Bootloader to a PC



PARALLEL PROGRAMMING

The DS89C420 allows parallel programming of its internal flash memory compatible with standard flash or EPROM programmers. In parallel programming mode, a mass-erase command is used to erase all memory locations in the 16kB program memory, the security block, and the memory bank select. Erasing the memory bank select sets it to the default state; the memory bank select cannot be altered otherwise. If lock bit LB2 has not been programmed, the program code can be read back for verification. The state of the lock bits can also be verified directly in the parallel programming mode. One instruction is used to read signature information (at addresses 30, 31, and 60h). Separate instructions are used for the option control register.

The following sequence can be used to program the flash memory in the parallel programming mode:

1) The DS89C420 is powered up and running at a clock speed between 4MHz and 6MHz.
2) Set RST = $\overline{EA}$ = 1 and $\overline{PSEN}$ = 0.
3) Apply the appropriate logic combination to pins P2.6, P2.7, P3.6, and P3.7 to select one of the flash instructions shown in Table 7.
   For program operation, apply the desired address to pins P1.7:0 and P2.5:0. Data is written to port 0.
   For verify operation, apply the desired address to pins P1.7:0 and P2.5:0. Data is read at port 0.
4) Pulse ALE/$\overline{PROG}$ once to perform an erase/program operation.
5) Repeat steps 3 and 4 as necessary.

ON-CHIP MOVX DATA MEMORY

On-chip data memory is provided by the 1kB SRAM and occupies addresses 0000h through 03FFh. The internal data memory is disabled after a power-on reset, and any MOVX instruction directs the data memory access to the external data memory. To enable the internal data memory, software must configure the data memory enable bits DME1 and DME0 (PMR.1-0). See “SFR Bit Descriptions” in the *Ultra-High-Speed Flash Microcontroller User’s Guide* for data memory configurations. Once enabled, MOVX instructions with addresses inside the 1k range access the on-chip data memory, and addresses exceeding the 1k range automatically access external data memory.

An internal data memory cycle spans only one system clock period to support fast internal execution.

Figure 8. External Program Memory Access (Non-Page Mode and CD1:CD0 = 10)

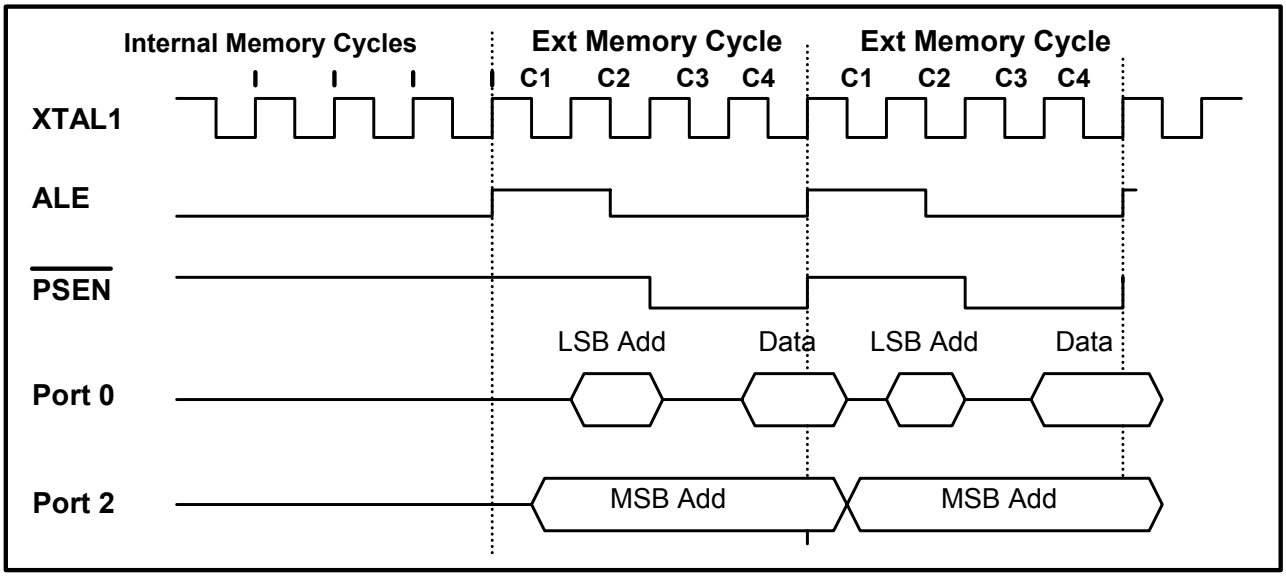


Table 5. Data Memory Cycle Stretch Values

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12288
100	7	4	8	16	16384
101	8	5	10	20	20480
110	9	6	12	24	24576
111	10	7	14	28	28672

As shown in Table 5, the stretch feature supports eight stretched external data-memory access cycles that can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data-memory access is extended by 1, 2, or 3 stretch machine cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup time and one system clock to create additional address hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, one stretch machine cycle (4 system clocks) is used to stretch the ALE pulse width, one stretch machine cycle is used to create additional setup, one stretch machine cycle is used to create additional hold time, and one stretch machine cycle is added to the $\overline{RD}$ or $\overline{WR}$ strobes.

Figure 9 and Figure 10 illustrate the timing relationship for external data-memory access in full speed (stretch value = 0), in the default stretch setting (stretch value = 1), and slow data-memory accessing (stretch value = 4) when the system clock is in divide by one mode (CD1:CD0 = 10b).

PAGE MODE, EXTERNAL MEMORY CYCLE

Page mode retains the basic circuitry requirement for original 8051 external memory interface, but alters the configuration of P0 and P2 for the purposes of address output and data I/O during external memory cycles. Additionally, the functions of ALE and $\overline{PSEN}$ are altered to support this mode of operation.

Setting the PAGEE (ACON.7) bit to logic 1 enables page mode. Clearing the PAGEE bit to a logic 0 disables the page mode and the external bus structure defaults to the original 8051 expanded bus configuration (non-page mode). The DS89C420 supports page mode in two external bus structures. The logic value of the page mode select bits in the ACON register determines the external bus structure and the basic memory cycle in the number of system clocks. Table 6 summarizes this option. The first three selections use the same bus structure but with a different memory cycle time. Setting the select bits to 11b selects another bus structure. Write access to the ACON register requires a timed access.

Table 6. Page Mode Select

PAGES1:PAGES0	CLOCKS PER MEMORY CYCLE		EXTERNAL BUS STRUCTURE
	PAGE HIT	PAGE MISS	
00	1	2	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of the address.
01	2	4	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of the address.
10	4	8	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of the address.
11	2	4	P0: Lower address byte. P2: The upper address byte is multiplexed with the data byte. **Note:** This setting affects external code fetches only; accessing the external data memory requires 4 clock cycles, regardless of page hit or miss.

The first page mode (page mode 1) external bus structure uses P2 as the primary address bus, (multiplexing both the most significant byte (MSB) and least significant byte (LSB) of the address for each external memory cycle) and P0 is used as the primary data bus. During external code fetches, P0 is held in a high-impedance state by the processor. Op codes are driven by the external memory onto P0 and latched at the end of the external fetch cycle at the rising edge of $\overline{PSEN}$. During external data read/write operations, P0 functions as the data I/O bus. It is held in a high-impedance state for external reads from data memory, and driven with data during external writes to data memory.

- A page miss occurs when the MSB of the subsequent address is different from the last address. The external memory machine cycle can be 2, 4, or 8 system clocks in length for a page miss.
- A page hit occurs when the MSB of the subsequent address does not change from the last address. The external memory machine cycle can be 1, 2, or 4 system clocks in length for a page hit.

During a page hit, P2 drives Addr0–7 of the 16-bit address while the most significant address byte is held in the external address latches. $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ strobe accordingly for the appropriate operation on the P0 data bus. There is no ALE assertion for page hits.

During a page miss, P2 drives the Addr [8:15] of the 16-bit address and holds it for the duration of the first half of the memory cycle to allow the external address latches to latch the new most significant address byte. ALE is asserted to strobe the external address latches. During this operation, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ are held in inactive states and P0 is in a high-impedance state. The second half of the memory cycle is executed as a page-hit cycle and the appropriate operation takes place.

A page miss can occur at set intervals or during external operations that require a memory access into a page of memory that has not been accessed during the last external cycle. Generally, the first external memory access causes a page miss. The new page address is stored internally, and is used to detect a page miss for the current external memory cycle.

Note that there are a few exceptions for this mode of operation when PAGES1 and PAGES2 are set to 00b:

- $\overline{\text{PSEN}}$ is asserted for both page hit and page miss for a full clock cycle.
- The execution of external MOVX instruction causes a page miss.
- A page miss occurs when fetching the next external instruction following the execution of an external MOVX instruction.

Figure 11 shows the external memory cycle for this bus structure. The first case illustrates a back-to-back execution sequence for 1-cycle page mode (PAGES1 = PAGES0 = 0b). $\overline{\text{PSEN}}$ remains active during page-hit cycles, and page misses are forced during and after MOVX executions, independent of the most significant byte of the subsequent addresses. The second case illustrates a MOVX execution sequence for 2-cycle page mode (PAGES1 = 0 and PAGES0 = 1). $\overline{\text{PSEN}}$ is active for a full clock cycle in code fetches. Note that changing the MSB of the data address causes the page misses in this sequence. The third case illustrates a MOVX execution sequence for 4-cycle page mode (PAGES1 = 1 and PAGES0 = 0). There is no page miss in this execution cycle because the most significant byte of the data address is assumed to match the last program address.

The second page mode (page mode 2) external bus structure multiplexes the most significant address byte with data on P2, and uses P0 for the least significant address byte. This bus structure is used to speed up external code fetches only. External data-memory access cycles are identical to the non-page mode except for the different signals on P0 and P2. Figure 12 illustrates the memory cycle for external code fetches.

Table 9. Page Mode 1, Data Memory Cycle Stretch Values (Pages1:Pages0 = 10)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

Table 10. Page Mode 2, Data Memory Cycle Stretch Values (Pages1:Pages0 = 11)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

As shown in the previous tables, the stretch feature supports eight stretched external data-memory access cycles that can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data-memory access and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch memory cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the control signals. This is because the first stretch uses one system clock to create additional address setup and data bus float time, and one system clock to create additional address and data hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, two stretch cycles are used to create additional setup (the ALE pulse width is also stretched by one stretch cycle for page miss) and one stretch cycle is used to create additional hold time. The following timing diagrams illustrate the external data-memory access at divide-by-1 system clock mode (CD1:CD0 = 10b).

Figure 13. Page Mode 1, External Data Memory Access (Pages = 01, Stretch = 1, CD = 10)

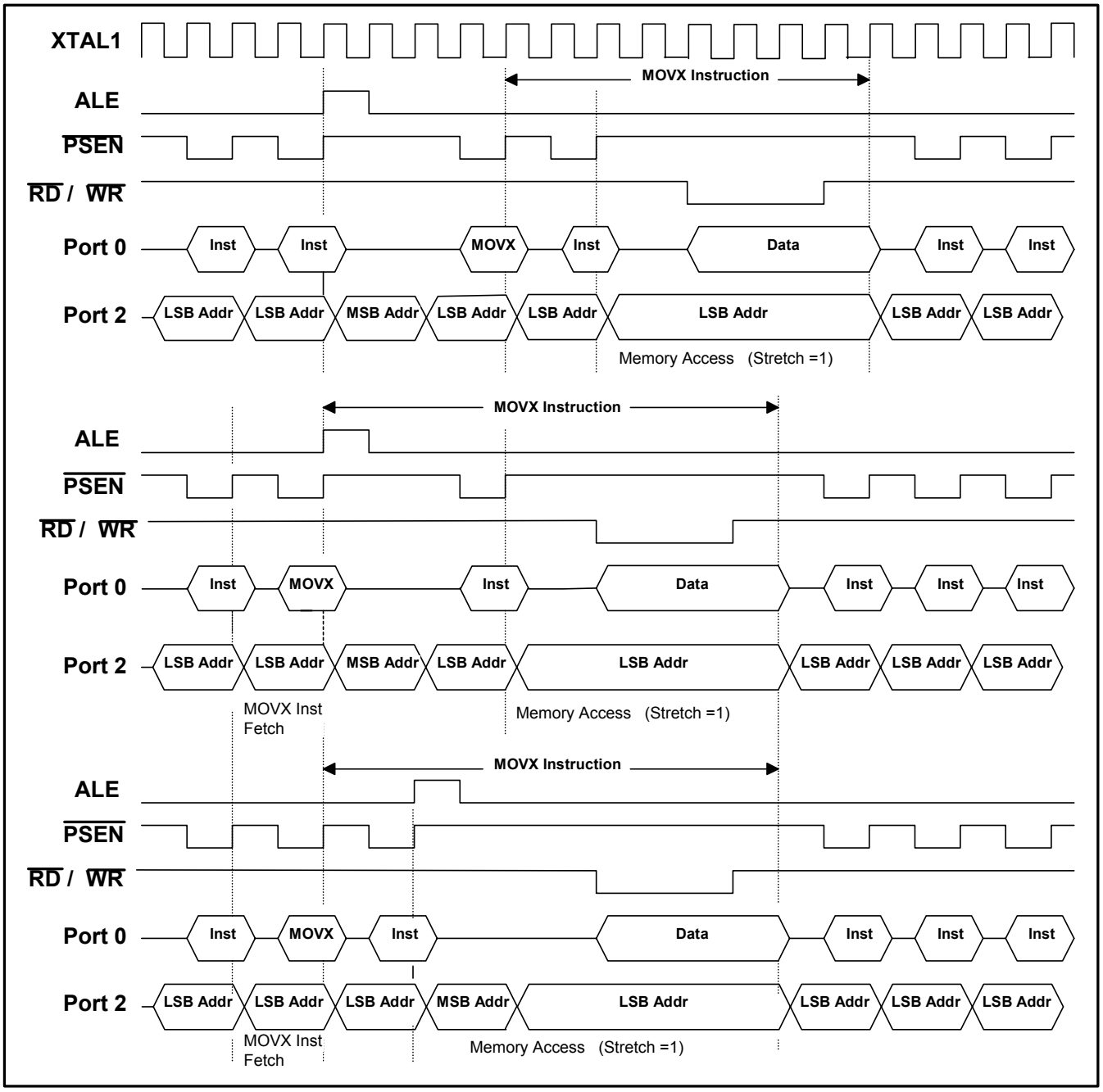


Figure 13 illustrates the external data-memory stretch cycle timing relationship when PAGEE = 1 and PAGES1:PAGES0 = 01. The stretch cycle shown is for a stretch value of 1 and is coincident with a page miss. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup and one system clock to create additional hold time.

regardless of the individual interrupt enable settings. The power-fail interrupt is controlled by its individual enable only.

The interrupt enables and priorities are functionally identical to those of the 80C52, except that the DS89C420 supports five levels of interrupt priorities instead of the original two.

INTERRUPT PRIORITY

There are five levels of interrupt priority: level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power-Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1)**	EX0 (IE.0)	LPX0 (IP0.0) MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5)*	ET0 (IE.1)	LPT0 (IP0.1) MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3)**	EX1 (IE.2)	LPX1 (IP0.2) MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7)*	ET1 (IE.3)	LPT1 (IP0.3) MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4) MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7) EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5) MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0) TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6) MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0) MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1) MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2) MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3) MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4) MPWDI (EIP1.4)

**Cleared automatically by hardware when the service routine is vectored to.*
***If the interrupt is edge triggered, cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.*

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

TIMER/COUNTERS

Three 16-bit timers are incorporated in the DS89C420. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that count oscillator cycles. Table 12 summarizes the timer functions.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with auto-reload. Timer 0 has a fourth operating mode as two 8-bit

timer/counters without auto-reload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The timer mode (TMOD) register controls the operation mode. Each timer consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. The timer control (TCON) register enables Timers 0 and 1.

Table 12. Timer Functions

FUNCTIONS	TIMER 0	TIMER 1	TIMER 2
Timer/Counter	13/16/8*/2 x 8 bit	13/16/8* bit	16 bit
Timer with Capture	No	No	Yes
External Control-Pulse Counter	Yes	Yes	No
Up/Down Auto-Reload Timer/Counter	No	No	Yes
Baud Rate Generator	No	Yes	Yes
Timer-Output Clock Generator	No	No	Yes

**8-bit timer/counter includes auto-reload feature; 2- x 8-bit mode does not.*

Timer 2 is a true 16-bit timer/counter that, with a 16-bit capture (RCAP2L and RCAP2H) register, is able to provide some unique functions like up/down auto-reload timer/counter and timer-output clock generation. Timer 2 (registers TL2 and TH2) is enabled by the T2CON register, and its mode of operation is selected by the T2MOD register.

Each timer has a selectable time base (Table 14). Following a reset, the timers default to divide-by-12 to maintain drop-in compatible with the 8051. If Timer 2 is used as a baud rate generator or clock output, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

For details of operation, refer to “Programmable Timers” in the *Ultra-High-Speed Flash Microcontroller User’s Guide*.

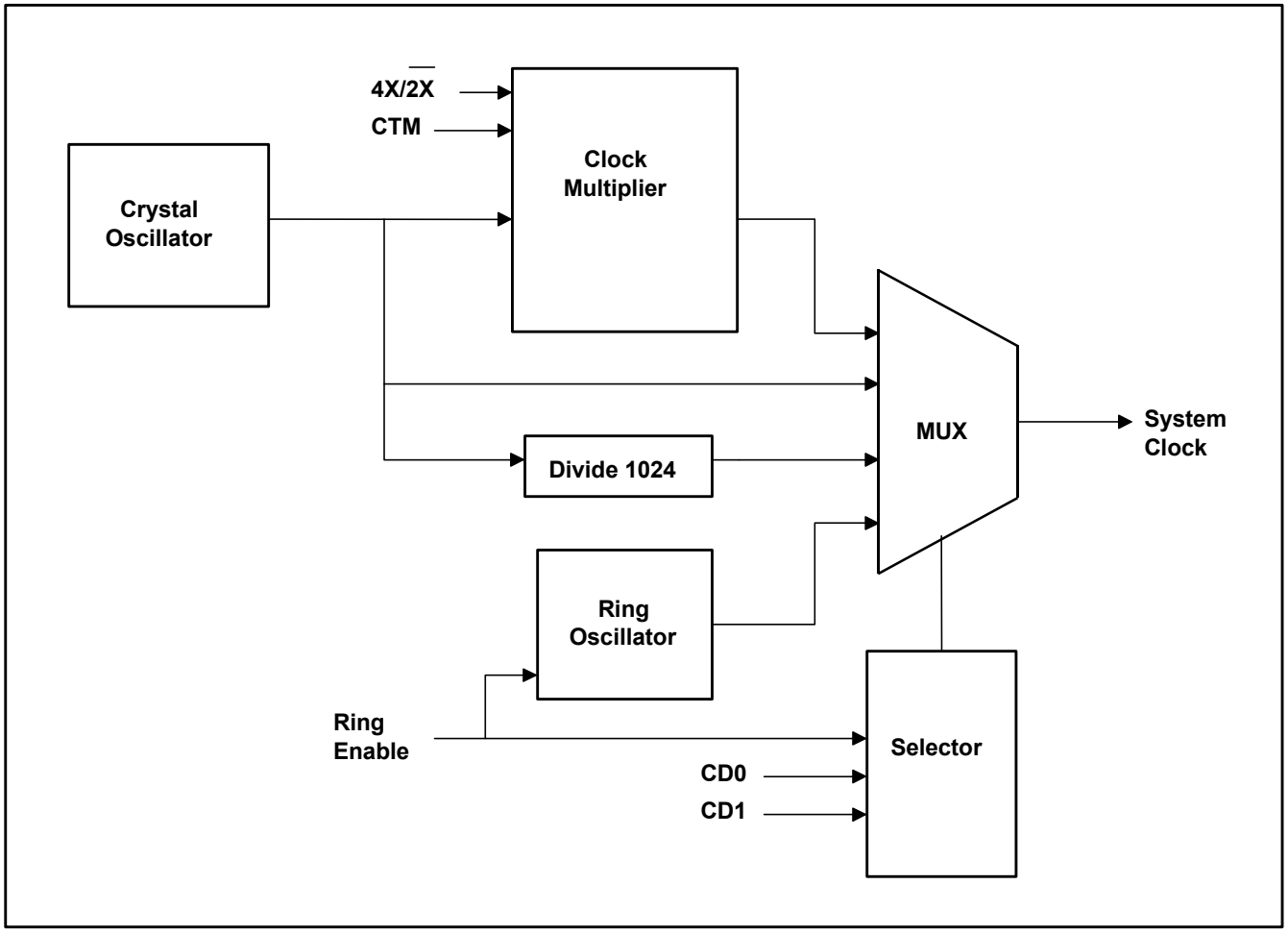
TIMED ACCESS

The timed access function provides control verification to system functions. The timed access function prevents an errant CPU from making accidental changes to certain SFR bits that are considered vital to proper system operation. This is achieved by using software control when accessing the following SFR control bits:

WDCON.0	RWT	Reset Watchdog Timer
WDCON.1	EWT	Watchdog Reset Enable
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.6	POR	Power-On Reset Flag
EXIF.0	BGS	Bandgap Select
ACON.5	PAGES0	Page Mode Select Bit 0
ACON.6	PAGES1	Page Mode Select Bit 1
ACON.7	PAGEE	Page Mode Enable
ROMSIZE.0	RMS0	Program Memory Size Select Bit 0
ROMSIZE.1	RMS1	Program Memory Size Select Bit 1
ROMSIZE.2	RMS2	Program Memory Size Select Bit 2
ROMSIZE.3	PRAME	Program RAM Enable
FCNTL.0	FC0	Flash Command Bit 0
FCNTL.1	FC1	Flash Command Bit 1
FCNTL.2	FC2	Flash Command Bit 2
FCNTL.3	FC3	Flash Command Bit 3

simplified diagram of the generation of the system clocks. Specifics of hardware restrictions associated with the use of the 4X/$\overline{2X}$ CTM, CKRY, CD1, and CD0 bits are outlined in the SFR description.

Figure 15. System Clock Sources



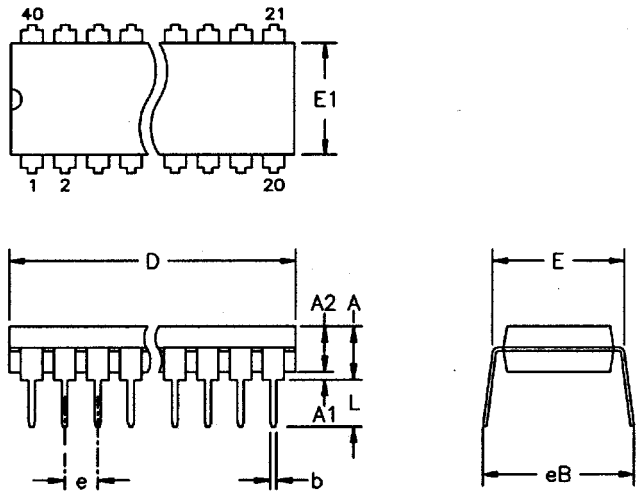
BANDGAP-MONITORED INTERRUPT AND RESET GENERATION

The power monitor in the DS89C420 monitors the V_{CC} pin in relation to the on-chip bandgap voltage reference. Whenever V_{CC} falls below V_{PFW}, an interrupt is generated if the corresponding power-fail interrupt-enable bit EPFI (WDCON.5) is set, causing the device to vector to address 33h. The power-fail interrupt-status bit PFI (WDCON.4) is set anytime V_{CC} transitions below V_{PFW}, and can only be cleared by software once set. Similarly, as V_{CC} falls below V_{RST}, a reset is issued internally to halt program execution. Following power-up, a power-on reset initiates a power-on reset timeout before starting program execution. When V_{CC} is first applied to the DS89C420, the processor is held in reset until $V_{CC} > V_{RST}$ and a delay of 65,536 oscillator cycles has elapsed, to ensure that power is within tolerance and the clock source has had time to stabilize. Once the reset timeout period has elapsed, the reset condition is removed automatically and software execution begins at the reset vector location of 0000h. The power-on reset flag POR (WDCON.6) is set to logic 1 to indicate a power-on reset has occurred, and can only be cleared by software.

When the DS89C420 enters stop mode, the bandgap, reset comparator, and power-fail interrupt comparator are automatically disabled to conserve power, if the BGS (EXIF.0) bit is set to a logic 0. This is the lowest power mode. If BGS is set to logic 1, the bandgap reference, reset comparator, and the power-fail comparator are powered up, although in a reduced fashion, while in stop mode.

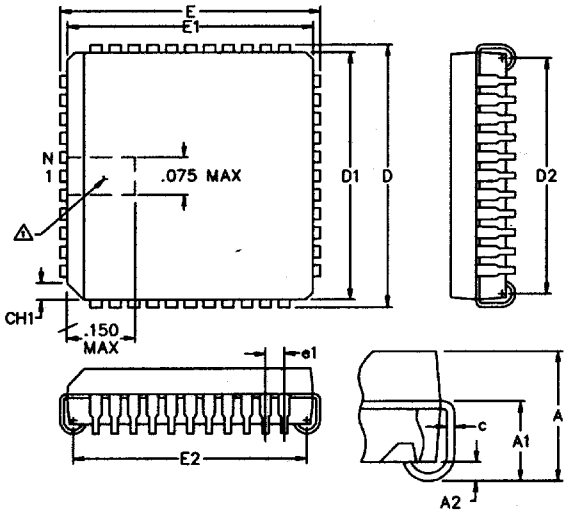
PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



PKG	40-PIN	
DIM	MIN	MAX
A	—	0.200
A1	0.015	—
A2	0.140	0.160
b	0.014	0.022
c	0.008	0.012
D	1.980	2.085
E	0.600	0.625
E1	0.530	0.555
e	0.090	0.110
L	0.115	0.145
eB	0.600	0.700

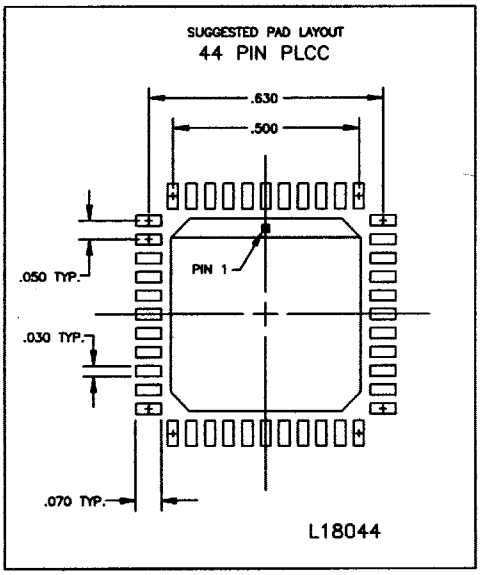
56–G5000–000
Dimensions are in inches (in).

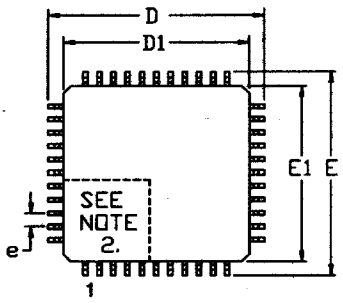


Note 1: Pin 1 identifier to be located in zone indicated.
Note 2: Controlling dimensions are in inches (in).

PKG	44–PIN	
DIM	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
c	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	–

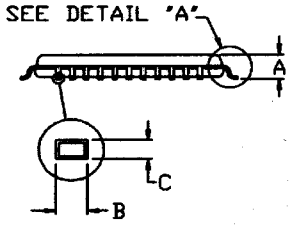
56–G4003–001

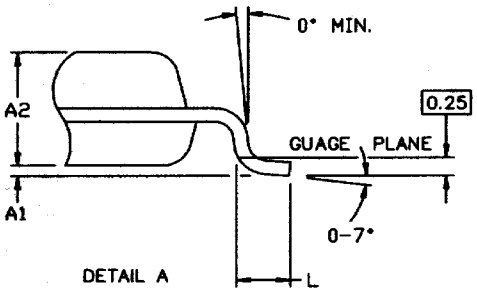




NOTES:

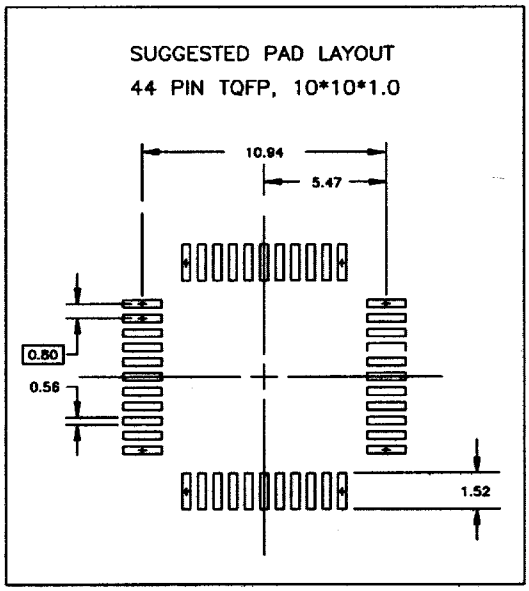
1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.





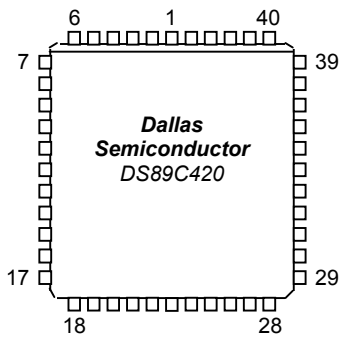
PKG	44-PIN	
DIM	MIN	MAX
A	–	1.20
A1	0.05	0.15
A2	0.95	1.05
D	11.80	12.20
D1	10.00 BSC	
E	11.80	12.20
E1	10.00 BSC	
L	0.45	0.75
e	0.80 BSC	
B	0.30	0.45
C	0.09	0.20

56-G4012-001



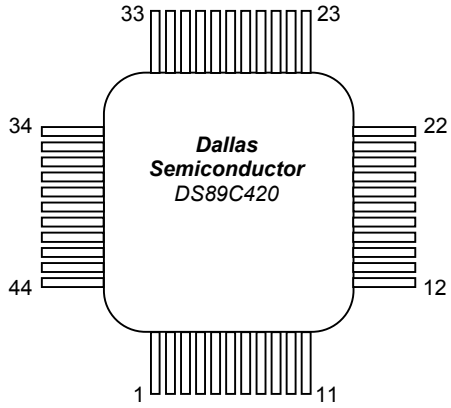
PIN CONFIGURATIONS

TOP VIEW



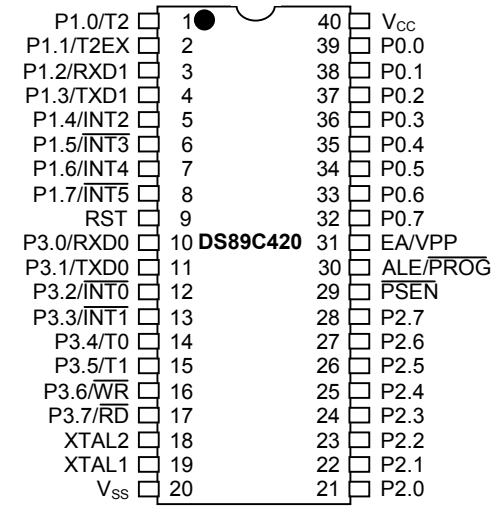
PLCC

TOP VIEW



TQFP

TOP VIEW



DIP

REVISION HISTORY

REVISION	DESCRIPTION
092200	Initial release
122601	Added errata (See www.maxim-ic.com/errata for details.)
042702	Official product introduction release
051302	Inserted AC Characteristics table
103102	Removed (Min Operating Voltage) from *DC Electrical Characteristics*; inserted diagram of ROM loader interface circuit
032003	Added 25MHz variant information
102203	Modified Figure 7 to support programmer-only operation.

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