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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3067rf20v

2.6 Instruction Set

2.6.1 Instruction Set Overview

The H8/300H CPU has 62 types of instructions, which are classified in table 2.1.

Table 2.1 Instruction Classification

Function	Instruction	Types
Data transfer	MOV, PUSH*1, POP*1, MOVTPE*2, MOVFPE*2	3
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, MULXS, DIVXU, DIVXS, CMP, NEG, EXTS, EXTU	18
Logic operations	AND, OR, XOR, NOT	4
Shift operations	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc*3, JMP, BSR, JSR, RTS	5
System control	TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	9
Block data transfer	EEPMOV	1
		Total 62 types

Notes: 1. POP.W Rn is identical to MOV.W @SP+, Rn.
PUSH.W Rn is identical to MOV.W Rn, @–SP.
POP.L ERn is identical to MOV.L @SP+, Rn.
PUSH.L ERn is identical to MOV.L Rn, @–SP.
2. Not available in the H8/3067 Group.
3. Bcc is a generic branching instruction.

Table 2.3 Data Transfer Instructions

Instruction	Size*	Function
MOV	B/W/L	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register.
MOVFPE	B	(EAs) → Rd Cannot be used in this LSI.
MOVTPE	B	Rs → (EAs) Cannot be used in this LSI.
POP	W/L	@SP+ → Rn Pops a general register from the stack. POP.W Rn is identical to MOV.W @SP+, Rn. Similarly, POP.L ERn is identical to MOV.L @SP+, ERn.
PUSH	W/L	Rn → @–SP Pushes a general register onto the stack. PUSH.W Rn is identical to MOV.W Rn, @–SP. Similarly, PUSH.L ERn is identical to MOV.L ERn, @–SP.

Note: * Size refers to the operand size.
B: Byte
W: Word
L: Longword

Table 2.4 Arithmetic Operation Instructions

Instruction	Size*	Function
ADD,SUB	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register. (Immediate byte data cannot be subtracted from data in a general register. Use the SUBX or ADD instruction.)
ADDX, SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry or borrow on data in two general registers, or on immediate data and data in a general register.
INC, DEC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
ADDS, SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA, DAS	B	Rd decimal adjust → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder
DIVXS	B/W	Rd ÷ Rs → Rd Performs signed division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder, or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder
CMP	B/W/L	Rd – Rs, Rd – #IMM Compares data in a general register with data in another general register or with immediate data, and sets CCR according to the result.
NEG	B/W/L	0 – Rd → Rd Takes the two's complement (arithmetic complement) of data in a general register.

4.6 Notes on Stack Usage

When accessing word data or longword data, the H8/3067 Group regards the lowest address bit as 0. The stack should always be accessed by word access or longword access, and the value of the stack pointer (SP, ER7) should always be kept even.

Use the following instructions to save registers:

PUSH.W Rn (or MOV.W Rn, @–SP)

PUSH.L ERn (or MOV.L ERn, @–SP)

Use the following instructions to restore registers:

POP.W Rn (or MOV.W @SP+, Rn)

POP.L ERn (or MOV.L @SP+, ERn)

Setting SP to an odd value may lead to a malfunction. Figure 4.7 shows an example of what happens when the SP value is odd.

6.2.6 Chip Select Control Register (CSCR)

CSCR is an 8-bit readable/writable register that enables or disables output of chip select signals ($\overline{CS}_7$ to $\overline{CS}_4$).

If output of a chip select signal is enabled by a setting in this register, the corresponding pin functions as a chip select signal ($\overline{CS}_7$ to $\overline{CS}_4$) output regardless of any other settings. CSCR cannot be modified in single-chip mode.

Bit	7	6	5	4	3	2	1	0
	CS7E	CS6E	CS5E	CS4E	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	—	—	—	—

Chip select 7 to 4 enable
These bits enable or disable chip select signal output

Reserved bits

CSCR is initialized to H'0F by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 4—Chip Select 7 to 4 Enable (CS7E to CS4E): These bits enable or disable output of the corresponding chip select signal.

Bit n CSnE	**Description**	
0	Output of chip select signal $\overline{CSn}$ is disabled	(Initial value)
1	Output of chip select signal $\overline{CSn}$ is enabled	

Note: n = 7 to 4

In byte access, whether the upper or lower data bus is used is determined by whether the address is even or odd. The upper data bus is used for an even address, and the lower data bus for an odd address.

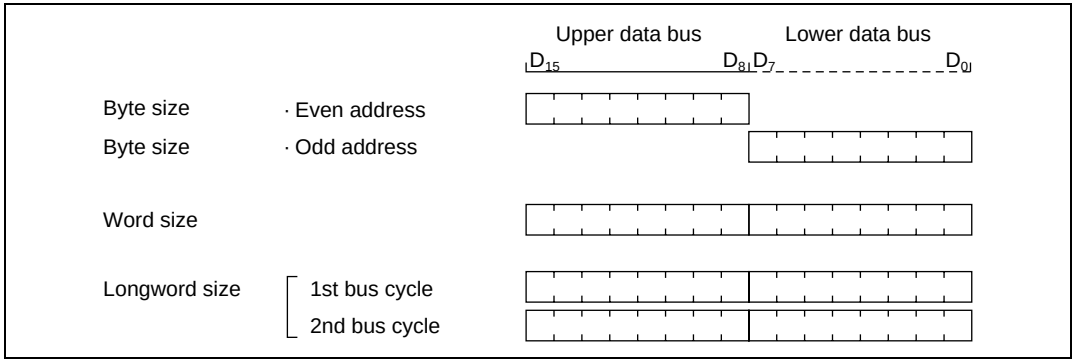


Figure 6.8 Access Sizes and Data Alignment Control (16-Bit Access Area)

6.4.3 Valid Strobes

Table 6.4 shows the data buses used, and the valid strobes, for the access spaces.

In a read, the $\overline{RD}$ signal is valid for both the upper and the lower half of the data bus.

In a write, the $\overline{HWR}$ signal is valid for the upper half of the data bus, and the $\overline{LWR}$ signal for the lower half.

If a DRAM read/write cycle is followed by an access cycle for an external area other than DRAM space when $\overline{HWR}$ and $\overline{LWR}$ are selected as the $\overline{UCAS}$ and $\overline{LCAS}$ output pins, an idle cycle (Ti) is inserted unconditionally immediately after the DRAM access cycle. See section 6.9, Idle Cycle, for details.

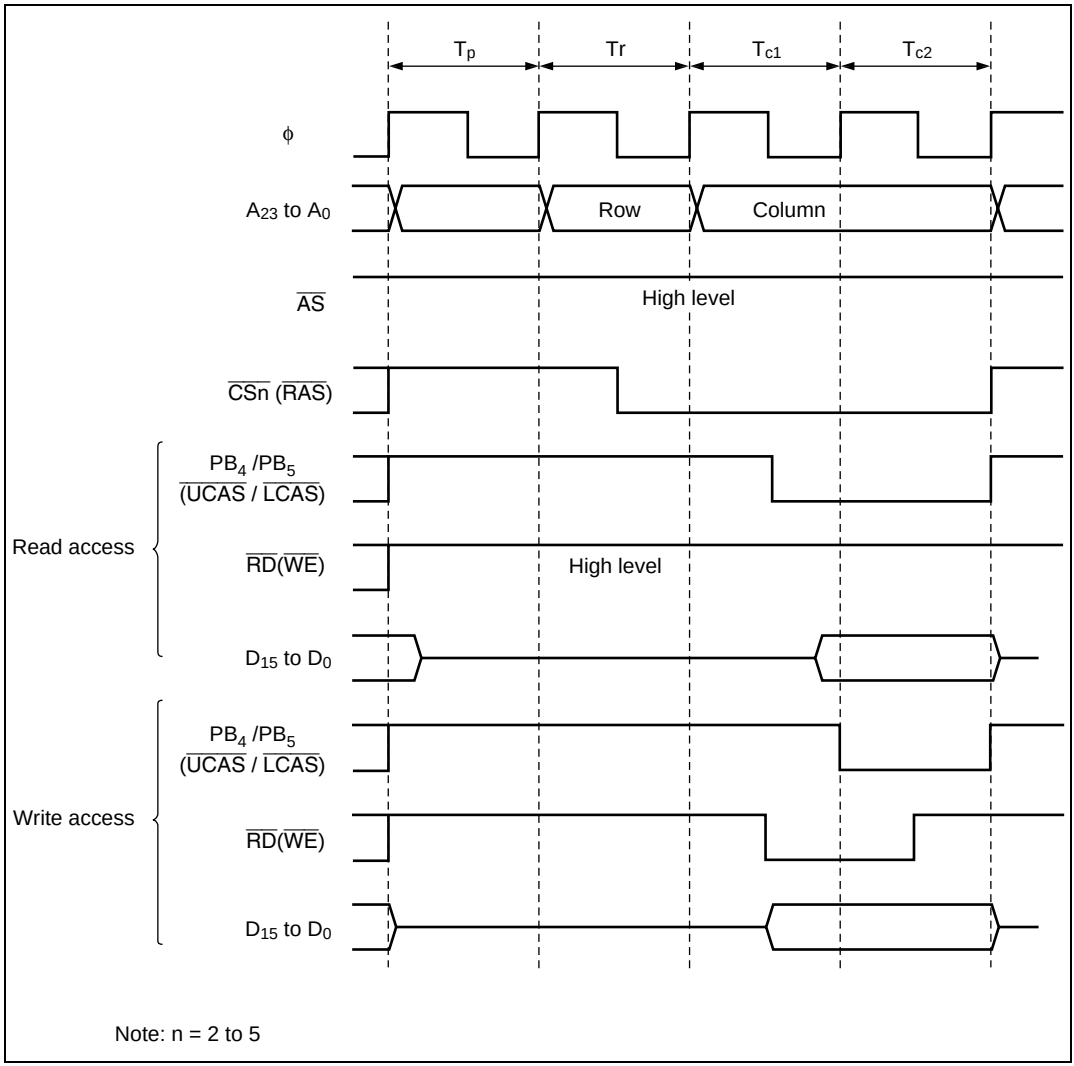


Figure 6.18 Basic Access Timing (CSEL = 0 in DRCRB)

Contention between RTCNT Write and Increment: If an increment pulse occurs in the T_3 state of an RTCNT write cycle, writing takes priority and RTCNT is not incremented. See Figure 6.40.

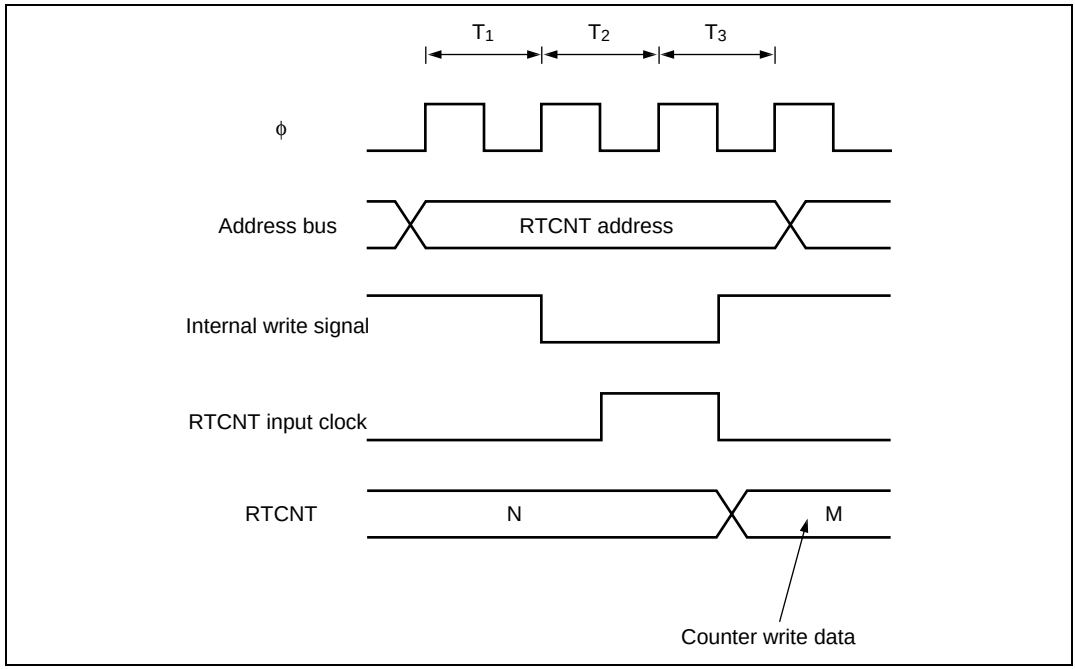
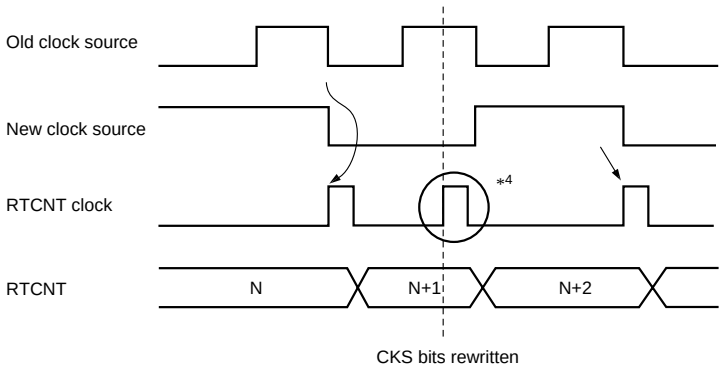
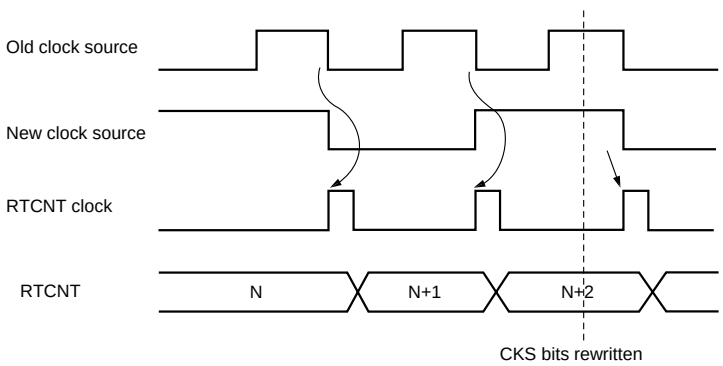


Figure 6.40 Contention between RTCNT Write and Increment

Table 6.10 Internal Clock Switchover and RTCNT Operation (2)

No.	CKS2 to CKS0 Write Timing	RTCNT Operation
3	"High" → "Low" switchover*3	
4	"High" → "High" switchover*4	

Notes: 3. Including switchover from a high clock source to the halted state.
4. The switchover is regarded as a falling edge, causing RTCNT to increment.

8.10.2 Register Descriptions

Table 8.16 summarizes the registers of port 9.

Table 8.16 Port 9 Registers

Address*	Name	Abbreviation	R/W	Initial Value
H'EE008	Port 9 data direction register	P9DDR	W	H'C0
H'FFFD8	Port 9 data register	P9DR	R/W	H'C0

Note: * Lower 20 bits of the address in advanced mode.

Port 9 Data Direction Register (P9DDR): P9DDR is an 8-bit write-only register that can select input or output for each pin in port 9.

Bits 7 and 6 are reserved. They are fixed at 1, and cannot be modified.

Bit	7	6	5	4	3	2	1	0
	—	—	$P9_5DDR$	$P9_4DDR$	$P9_3DDR$	$P9_2DDR$	$P9_1DDR$	$P9_0DDR$
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Reserved bits

Port 9 data direction 5 to 0
These bits select input or output for port 9 pins

When port 9 functions as an input/output port, a pin in port 9 becomes an output port if the corresponding P9DDR bit is set to 1, and an input port if this bit is cleared to 0. For the method of selecting the pin functions, see table 8.17.

P9DDR is a write-only register. Its value cannot be read. All bits return 1 when read.

P9DDR is initialized to H'C0 by a reset and in hardware standby mode. In software standby mode it retains its previous setting. Therefore, if a transition is made to software standby mode while port 9 is functioning as an input/output port and a P9DDR bit is set to 1, the corresponding pin maintains its output state.

Channel	Address*1	Name	Abbre-viation	R/W	Initial Value
2	H'FFF78	Timer control register 2	TCR2	R/W	H'80
	H'FFF79	Timer I/O control register 2	TIOR2	R/W	H'88
	H'FFF7A	Timer counter 2H	TCNT2H	R/W	H'00
	H'FFF7B	Timer counter 2L	TCNT2L	R/W	H'00
	H'FFF7C	General register A2H	GRA2H	R/W	H'FF
	H'FFF7D	General register A2L	GRA2L	R/W	H'FF
	H'FFF7E	General register B2H	GRB2H	R/W	H'FF
	H'FFF7F	General register B2L	GRB2L	R/W	H'FF

Notes: 1. The lower 20 bits of the address in advanced mode are indicated.
2. Only 0 can be written in bits 3 to 0, to clear the flags.

15.1.2 Block Diagram

Figure 15.1 shows a block diagram of the A/D converter.

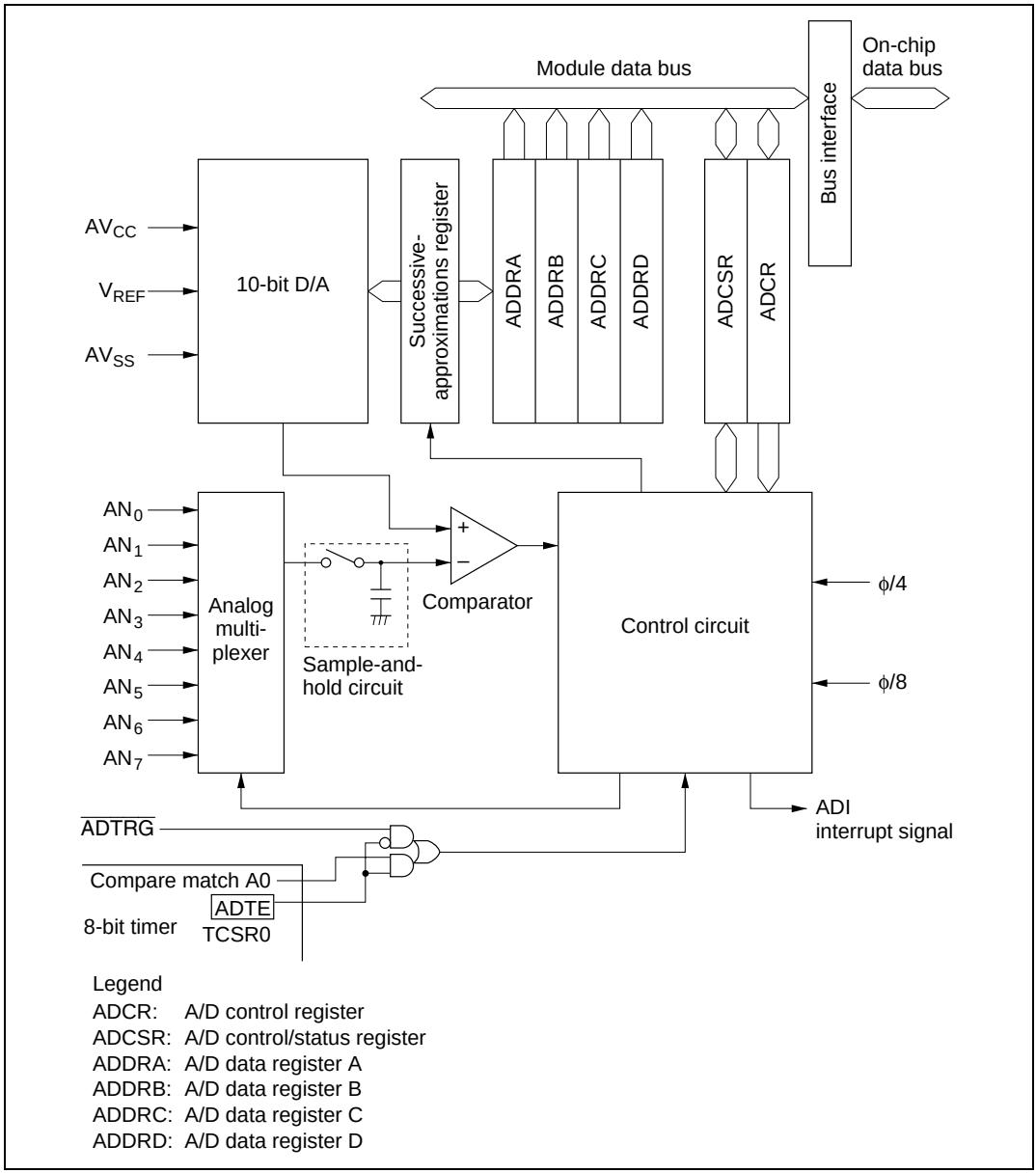


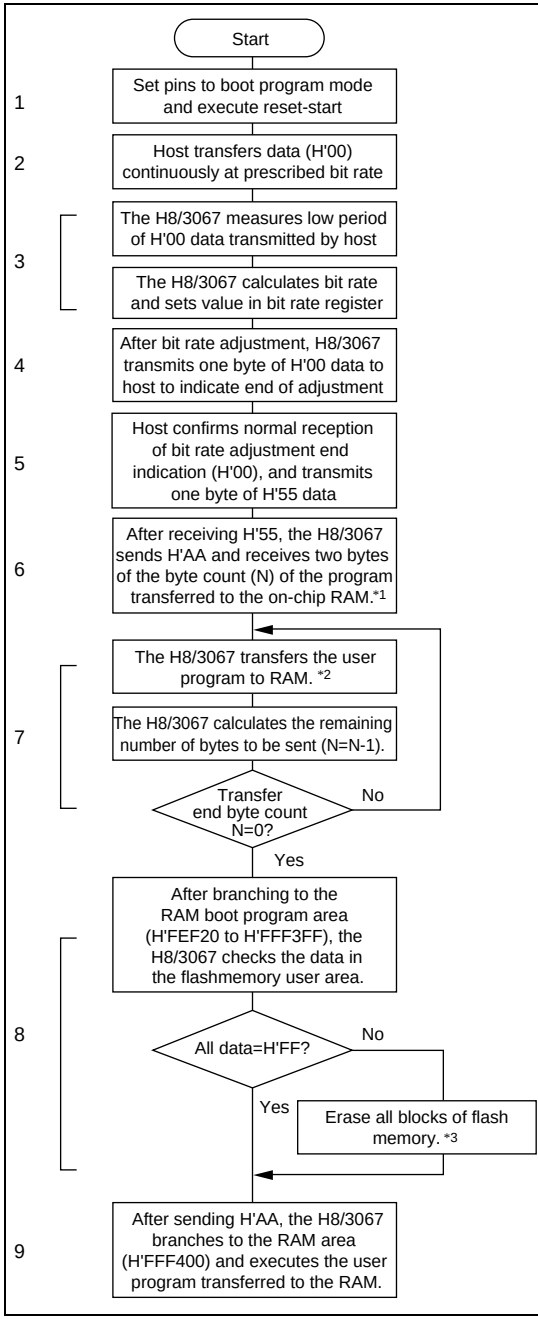
Figure 15.1 A/D Converter Block Diagram

Section 17 RAM

17.1 Overview

The H8/3067 and H8/3066 have 4 kbytes of high-speed static RAM on-chip. The H8/3065 has 2 kbytes. The RAM is connected to the CPU by a 16-bit data bus. The CPU accesses both byte data and word data in two states, making the RAM useful for rapid data transfer.

The on-chip RAM of the H8/3067 and H8/3066 is assigned to addresses H'FEF20 to H'FFF1F in modes 1, 2, and 7, and to addresses H'FFEF20 to H'FFFF1F in modes 3, 4, and 5,and to addresses H'EF20 to H'FF1F in mode 6. The on-chip RAM of the H8/3065 are assigned to addresses H'FF720 to H'FFF1F in modes 1, 2, and 7, and to addresses H'FFF720 to H'FFFF1F in modes 3, 4, and 5, and to addresses H'F720 to H'FF1F in mode 6. The RAM enable bit (RAME) in the system control register (SYSCR) can enable or disable the on-chip RAM.



1 Set the H8/3067 to the boot mode and reset starts the LSI.

2 Set the host to the prescribed bit rate (4800, 9600) and consecutively send H'00 data in 8-bit data, 1 stop bit format.

3 The H8/3067 repeatedly measures the RXD1 pin Low period and calculates the asynchronous communication bit rate at which the host performs transfer.

4 At the end of SCI bit rate adjustment, the H8/3067 sends one byte of H'00 data to signal the end of adjustment.

5 Check if the host normally received the one byte bit rate adjustment end signal sent from the H8/3067 and sent one byte of H'55 data.

6 After H'55 is sent, the host receives H'AA and sends the byte count of the user program that is transferred to the H8/3067.
Send the 2-byte count in upper byte and lower byte order. Then sequentially send the program set by the user.
The H8/3067 sequentially sends (echo back) each byte of the received byte count and user program to the host as verification data.

7 The H8/3067 sequentially writes the received user program to the on-chip RAM area (H'FFF400–H'FFFF1F).

8 Before executing the transferred user program, the H8/3067 checks if data was written to flash memory after control branched to the RAM boot program area (H'FEF20–H'FFF3F). If data was already written to flash memory, all the blocks are erased.

9 After sending H'AA, this LSI branches to the on-chip RAM area (H'FFF400) and executes the user program written to that area.

Notes: 1. The RAM area that can be used by the user is 2.8k Byte. Set the transfer byte count to within 2.8k Byte. Always send the 2-byte transfer byte count in upper byte and lower byte order. Transfer byte count example: For 256 bytes (H'0100), upper byte H'01, lower byte H'00.

2. Set the part that controls the user program flash memory at the program according to the flash memory programming/erase algorithms described later.

3. When a memory cell malfunctions and cannot be erased, the H8/3067 sends one H'FF byte as an erase error and stops the erase operation and subsequent operations.

Figure 18.6 Boot Mode Execution Procedure

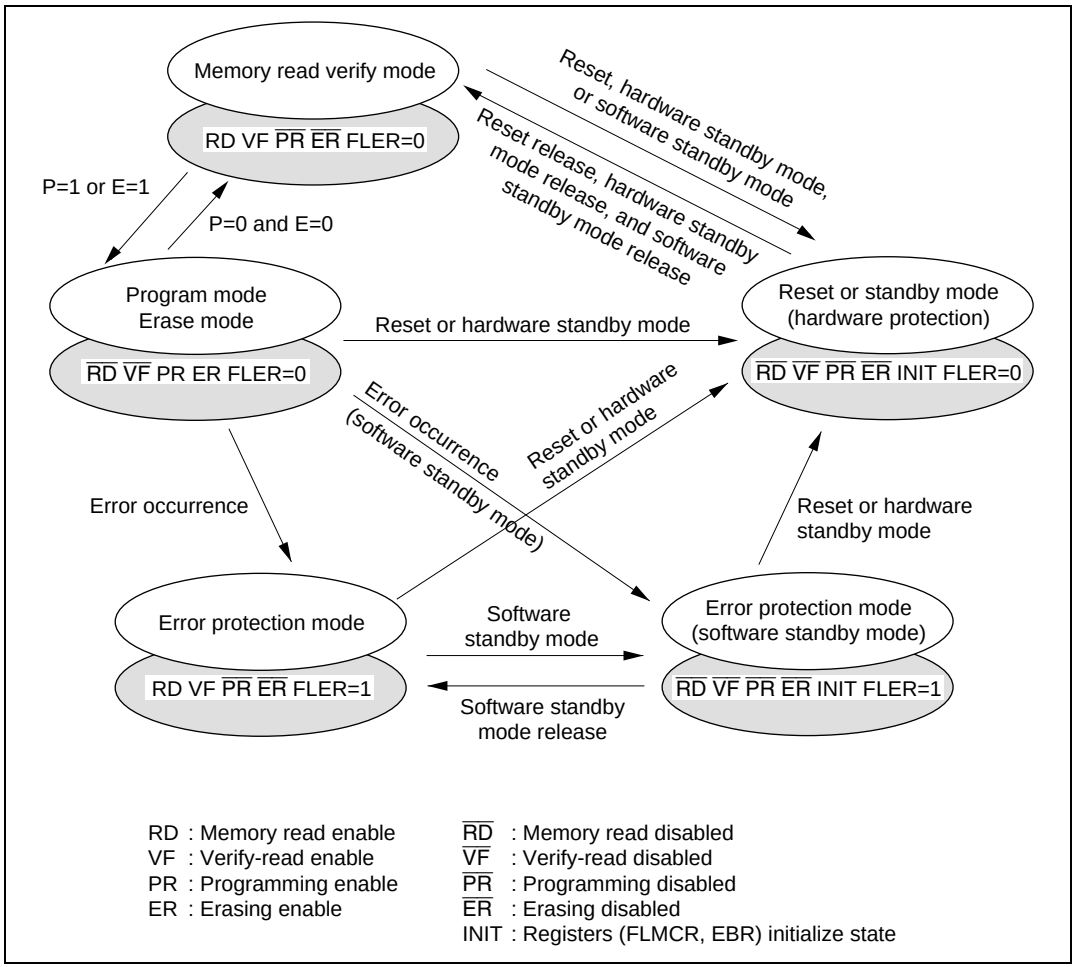


Figure 18.13 Flash Memory State Transitions
(When High level apply to FWE pin in modes 5 and 7 (on-chip ROM enabled))

The error protection function is disabled for errors other than the FLER bit set conditions. If considerable time elapses up to transit to this protection state, the flash memory may already be damaged. As a result, this function cannot completely protect the flash memory against damage.

Therefore, to prevent such erroneous operation, operation must be carried out correctly in according with the program/erase algorithms in the state that flash write enable (FWE) is set. In addition, the operation must be always carried out correctly by supervising microcomputer errors inside and outside the chip with the watchdog timer, etc. At transition to this protection mode, the flash memory may be erroneously programmed or erased, or its abort may result in incomplete

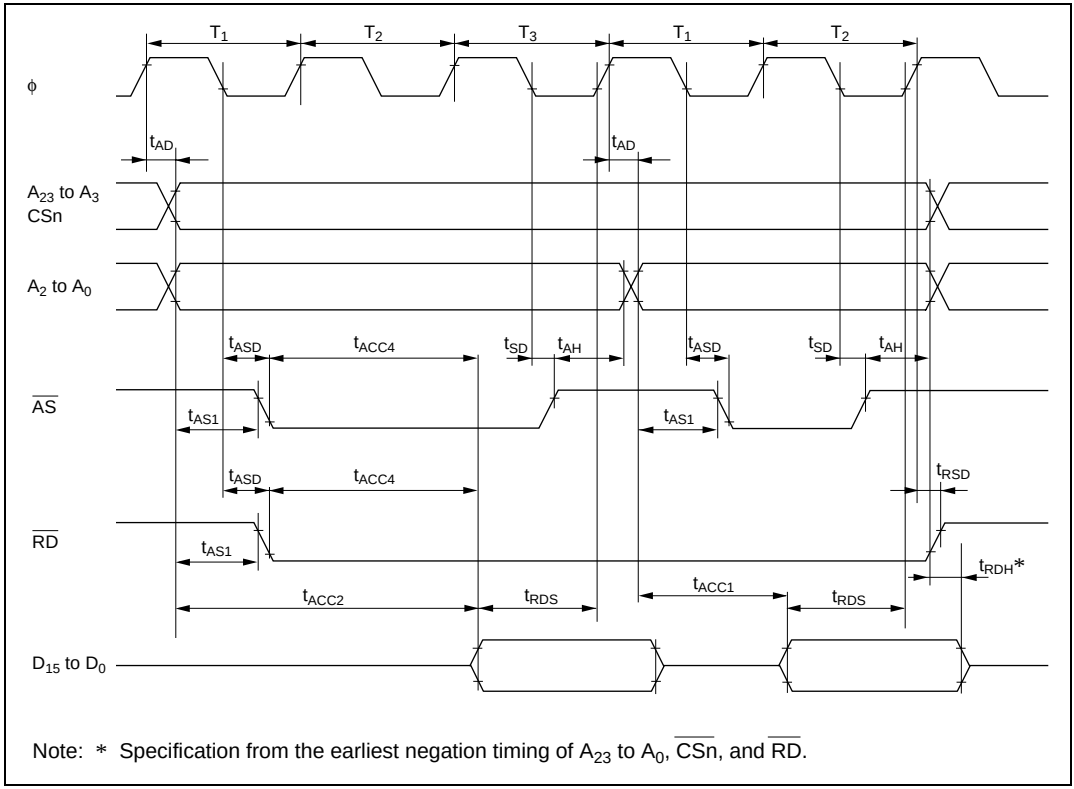
21.2.2 DC Characteristics

Tables 21.11 lists the DC characteristics. Table 21.12 lists the permissible output currents.

Table 21.11 DC Characteristics (1)

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC} *1,
V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)
[Programming/erasing conditions: T_a = 0°C to +75°C (regular specifications),
T_a = 0°C to +85°C (wide-range specifications)]

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0, FWE	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port 7		2.0	—	AV_{CC} + 0.3	V	
	Ports 1 to 6, $P8_3$, $P8_4$, $P9_0$ to $P9_5$, port B		2.0	—	V_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, FWE, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, ports 1 to 7, $P8_3$, $P8_4$, $P9_0$ to $P9_5$, port B		–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, 2, and 5		—	—	1.0	V	I_{OL} = 10 mA
Input leakage current	$\overline{STBY}$, $\overline{RES}$, NMI, FWE MD_2 to MD_0	$\|I_{in}\|$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	Port 7		—	—	1.0	µA	V_{in} = 0.5 V to AV_{CC} – 0.5 V



Note: * Specification from the earliest negation timing of A_{23} to A_0, $\overline{CSn}$, and $\overline{RD}$.

Figure 21.14 Burst ROM Access Timing: Two-State Access

FLMCR-Flash Memory Control Register | H'EE030 | Flash Memory

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	ESU	PSU	EV	PV	E	P
Modes 1 to 4, and 6 — Initial value	0	0	0	0	0	0	0	0
Modes 1 to 4, and 6 — Read/Write	R	R	R	R	R	R	R	R
Modes 5 and 7 — Initial value	1/0	0	0	0	0	0	0	0
Modes 5 and 7 — Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program mode

0	Program mode cleared (Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1

Erase mode

0	Erase mode cleared (Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1

Program-verify mode

0	Program-verify mode cleared (Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE = 1

Erase-verify mode

0	Erase-verify mode cleared (Initial value)
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE = 1

Program setup

0	Program setup cleared (Initial value)
1	Program setup [Setting condition] When FWE = 1 and SWE = 1

Erase setup bit

0	Erase setup cleared (Initial value)
1	Erase setup [Setting condition] When FWE = 1 and SWE = 1

Software write enable bit

0	Write/erase disabled (Initial value)
1	Write/erase enabled [Setting condition] When FWE = 1

Flash write enable bit

0	When a low level is input to the FWE pin (hardware protection state)
1	When a high level is input to the FWE pin

Note: This register is used only in the flash memory and flash memory R versions. Reading the corresponding address in a mask ROM version will always return 1s, and writes to this address are disabled. Fix the FWE pin low in mode 6.

P4PCR—Port 4 Input Pull-Up Control Register	H'EE03E	Port 4

Bit	7	6	5	4	3	2	1	0
	$P4_7PCR$	$P4_6PCR$	$P4_5PCR$	$P4_4PCR$	$P4_3PCR$	$P4_2PCR$	$P4_1PCR$	$P4_0PCR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 4 input pull-up control 7 to 0

0	Input pull-up transistor is off
1	Input pull-up transistor is on

Note: Valid when the corresponding P4DDR bit is cleared to 0 (designating generic input).

P5PCR—Port 5 Input Pull-Up Control Register	H'EE03F	Port 5

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P5_3PCR$	$P5_2PCR$	$P5_1PCR$	$P5_0PCR$
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Port 5 input pull-up control 3 to 0

0	Input pull-up transistor is off
1	Input pull-up transistor is on

Note: Valid when the corresponding P5DDR bit is cleared to 0 (designating generic input).

Pin Name	Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released Mode	Program Execution Mode
$P8_0$	1 to 5	T	T	When DRAM space is not selected[*1] (RFSHE=0) Keep (RFSHE=1) Illegal setting When DRAM space is selected[*2] (RFSHE=0) Keep (RFSHE=1, SRFMD=0, SSOE=0) T (RFSHE=1, SRFMD=0, SSOE=1) H (RFSHE=1, SRFMD=1) $\overline{RFSH}$	When DRAM space is selected[*1] (RFSHE=0) Keep (RFSHE=1) Illegal setting When DRAM space is selected[*2] (RFSHE=0) Keep (RFSHE=1) T	(RFSHE=0) I/O port (RFSHE=1) $\overline{RFSH}$
	6, 7	T	T	Keep	—	I/O port
$P8_1$	1 to 5	T	T	When DRAM space is selected[*3] (SSOE=0) T (SSOE=1) H When DRAM space is selected[*4] Keep Otherwise[*5 *1] (DDR=0) T (DDR=1, SSOE=0) T (DDR=1, SSOE=1) H	When DRAM space is selected[*3] T When DRAM space is selected[*4] Keep Otherwise[*1] (DDR=0) Keep (DDR=1) T	When DRAM space is selected and RAS3 is output $\overline{RAS_3}$ When DRAM space is selected and RAS3 is not output I/O port Otherwise (DDR=0) Input port (DDR=1) $\overline{CS_3}$
	6, 7	T	T	Keep	—	I/O port