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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3067rf20vtr

Section 5 Interrupt Controller

5.1 Overview

5.1.1 Features

The interrupt controller has the following features:

- Interrupt priority registers (IPRs) for setting interrupt priorities

  Interrupts other than NMI can be assigned to two priority levels on a module-by-module basis in interrupt priority registers A and B (IPRA and IPRB).
- Three-level masking by the I and UI bits in the CPU condition code register (CCR)
- Seven external interrupt pins

  NMI has the highest priority and is always accepted*; either the rising or falling edge can be selected. For each of IRQ_0 to IRQ_5, sensing of the falling edge or level sensing can be selected independently.

Note: * In the flash memory and flash memory R versions, NMI input is sometimes disabled. For details see 18.6.4, NMI Input Disable Conditions.

Bit 2—Priority Level B2 (IPRB2): Selects the priority level of SCI channel 1 interrupt requests.

Bit 2 IPRB2	Description	
0	SCI1 interrupt requests have priority level 0 (low priority)	(Initial value)
1	SCI1 interrupt requests have priority level 1 (high priority)	

Bit 1—Priority Level B1 (IPRB1): Selects the priority level of SCI channel 2 interrupt requests.

Bit 1 IPRB1	Description	
0	SCI channel 2 interrupt requests have priority level 0 (low priority)	(Initial value)
1	SCI channel 2 interrupt requests have priority level 1 (high priority)	

Bit 0—Reserved: This bit can be written and read, but it does not affect interrupt priority.

Bits 3 and 2—Area 5 Wait Control 1 and 0 (W51, W50): These bits select the number of program wait states when area 5 in external space is accessed while the AST5 bit in ASTCR is set to 1.

Bit 3 W51	Bit 2 W50	Description
0	0	Program wait not inserted when external space area 5 is accessed
	1	1 program wait state inserted when external space area 5 is accessed
1	0	2 program wait states inserted when external space area 5 is accessed
	1	3 program wait states inserted when external space area 5 is accessed (Initial value)

Bits 1 and 0—Area 4 Wait Control 1 and 0 (W41, W40): These bits select the number of program wait states when area 4 in external space is accessed while the AST4 bit in ASTCR is set to 1.

Bit 1 W41	Bit 0 W40	Description
0	0	Program wait not inserted when external space area 4 is accessed
	1	1 program wait state inserted when external space area 4 is accessed
1	0	2 program wait states inserted when external space area 4 is accessed
	1	3 program wait states inserted when external space area 4 is accessed (Initial value)

Bit 4—Burst Cycle Select 1 (BRSTS1): Selects the number of burst cycle states for the burst ROM interface.

Bit 4 BRSTS1	Description	
0	Burst access cycle comprises 2 states	(Initial value)
1	Burst access cycle comprises 3 states	

Bit 3—Burst Cycle Select 0 (BRSTS0): Selects the number of words that can be accessed in a burst ROM interface burst access.

Bit 3 BRSTS0	Description
0	Max. 4 words in burst access (burst access on match of address bits above A3)(
1	Max. 8 words in burst access (burst access on match of address bits above A4)

Bit 2—Reserved: Read-only bit, always read as 1.

Bit 1—Area Division Unit Select (RDEA): Selects the memory map area division units. This bit is valid in modes 3, 4, and 5, and is invalid in modes 1, 2, 6, and 7.

Bit 1 RDEA	Description		
0	Area divisions are as follows:	Area 0: 2 MB	Area 4: 1.93 MB
		Area 1: 2 MB	Area 5: 4 kB
		Area 2: 8 MB	Area 6: 23.75 kB
		Area 3: 2 MB	Area 7: 22 B
1	Areas 0 to 7 are the same size (2 MB)		(Initial value)

Bit 0—WAIT Pin Enable (WAITE): Enables or disables wait insertion by means of the $\overline{\text{WAIT}}$ pin.

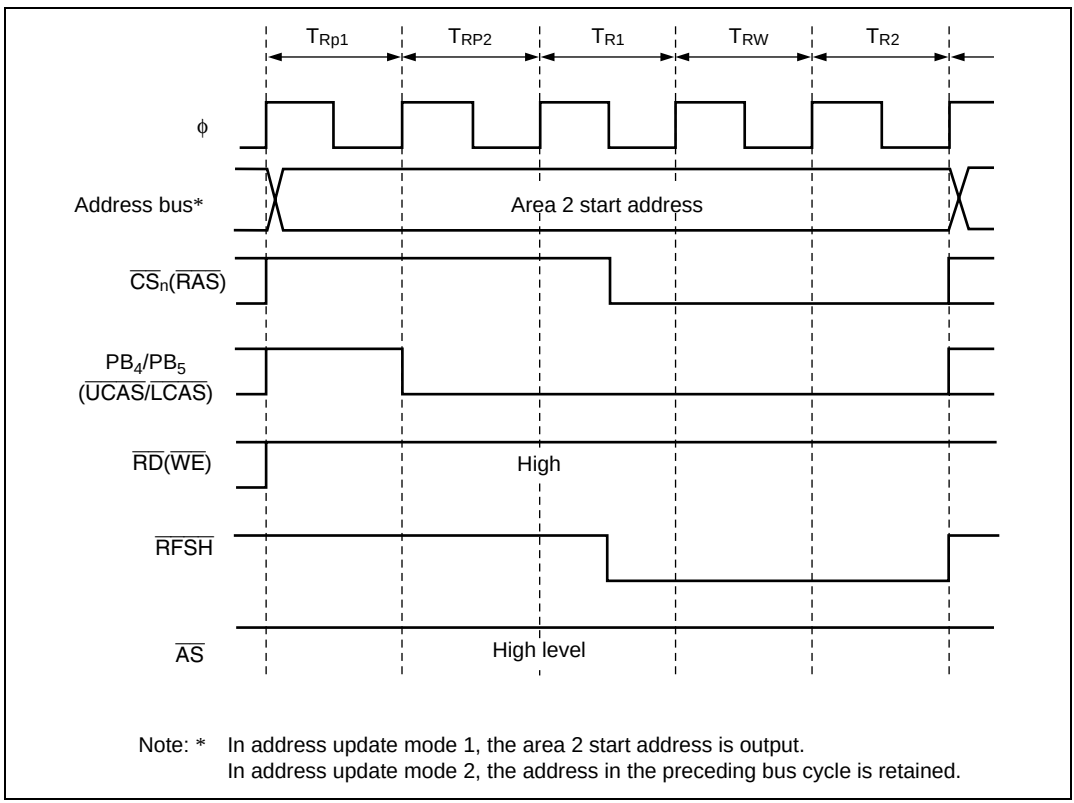
Bit 0 WAITE	Description
0	$\overline{\text{WAIT}}$ pin wait input is disabled, and the $\overline{\text{WAIT}}$ pin can be used as an input/output port (Initial value)
1	$\overline{\text{WAIT}}$ pin wait input is enabled

The basic CBS refresh cycle timing comprises three states: one RAS precharge cycle (T_{RP}) state, and two RAS output cycle (T_{R1}, T_{R2}) states. Either one or two states can be selected for the RAS precharge cycle. When the TPC bit is set to 1 in DRCRB, $\overline{RAS}$ signal output is delayed by one cycle. This does not affect the timing of $\overline{UCAS}$ and $\overline{LCAS}$ output.

Use the RLW bit in DRCRB to adjust the $\overline{RAS}$ signal width. A single refresh wait state (T_{RW}) can be inserted between the T_{R1} state and T_{R2} state by setting the RLW bit to 1.

The RLW bit setting is valid only for CBR refresh cycles, and does not affect DRAM read/write cycles. The number of states in the CBR refresh cycle is not affected by the settings in ASTCR, WCRH, or WCRL, or by the state of the $\overline{WAIT}$ pin.

Figure 6.29 shows the timing when the TPC bit and RLW bit are both set to 1.



Note: * In address update mode 1, the area 2 start address is output.
In address update mode 2, the address in the preceding bus cycle is retained.

Figure 6.29 CBR Refresh Timing (CSEL = 0, TPC = 1, RLW = 1)

Bits 2 to 0—Data Transfer Select 2B to 0B (DTS2B, DTS1B, DTS0B): These bits select the data transfer activation source. The selectable activation sources differ between normal mode and block transfer mode.

Normal mode

Bit 2 DTS2B	Bit 1 DTS1B	Bit 0 DTS0B	Description
0	0	0	Auto-request (burst mode) (Initial value)
		1	Cannot be used
	1	0	Auto-request (cycle-steal mode)
		1	Cannot be used
1	0	0	Cannot be used
		1	Cannot be used
	1	0	Falling edge of $\overline{\text{DREQ}}$
		1	Low level input at $\overline{\text{DREQ}}$

Block transfer mode

Bit 2 DTS2B	Bit 1 DTS1B	Bit 0 DTS0B	Description
0	0	0	Compare match/input capture A interrupt from 16-bit timer channel 0 (Initial value)
		1	Compare match/input capture A interrupt from 16-bit timer channel 1
	1	0	Compare match/input capture A interrupt from 16-bit timer channel 2
		1	Conversion-end interrupt from A/D converter
1	0	0	Cannot be used
		1	Cannot be used
	1	0	Falling edge of $\overline{\text{DREQ}}$
		1	Cannot be used

The same internal interrupt can be selected to activate two or more channels. The channels are activated in a priority order, highest priority first. For the priority order, see section 7.4.9, Multiple-Channel Operation.

Figure 7.15 shows an auto-requested burst-mode transfer. This example shows a transfer of three words from a 16-bit two-state access area to another 16-bit two-state access area.

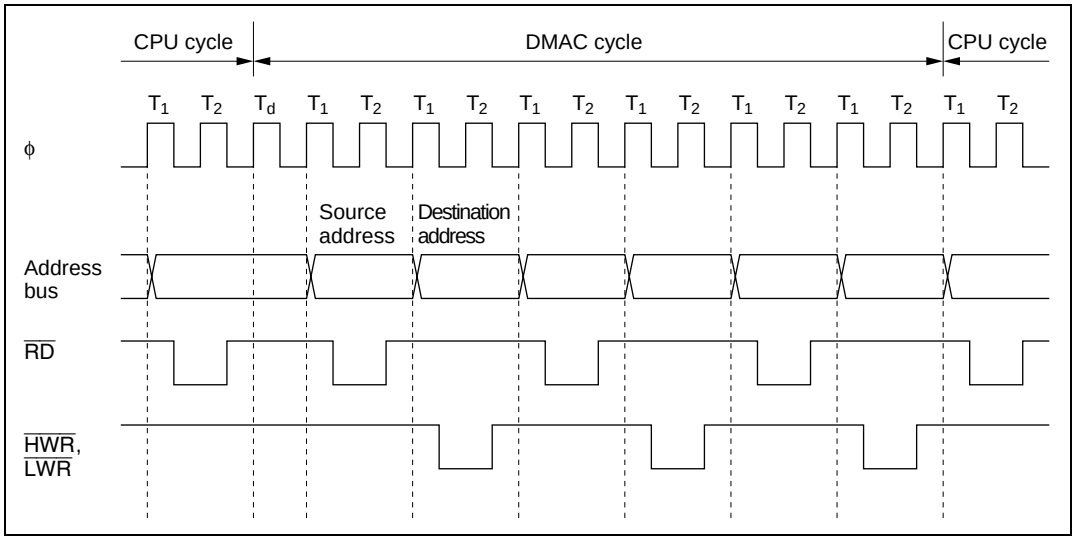


Figure 7.15 Burst DMA Bus Timing

When the DMAC is activated from a $\overline{\text{DREQ}}$ pin there is a minimum interval of four states from when the transfer is requested until the DMAC starts operating. The $\overline{\text{DREQ}}$ pin is not sampled during the time between the transfer request and the start of the transfer. In short address mode and normal mode, the pin is next sampled at the end of the read cycle. In block transfer mode, the pin is next sampled at the end of one block transfer.

8.2 Port 1

8.2.1 Overview

Port 1 is an 8-bit input/output port also used for address output, with the pin configuration shown in figure 8.1. The pin functions differ between the expanded modes with on-chip ROM disabled, expanded modes with on-chip ROM enabled, and single-chip mode. In modes 1 to 4 (expanded modes with on-chip ROM disabled), they are address bus output pins (A_7 to A_0).

In modes 5 (expanded modes with on-chip ROM enabled), settings in the port 1 data direction register (P1DDR) can designate pins for address bus output (A_7 to A_0) or generic input. In mode 6 and 7 (single-chip mode), port 1 is a generic input/output port.

When DRAM is connected to area 2, 3, 4, 5, A_7 to A_0 output row and column addresses in read and write cycles. For details see section 6.5, DRAM Interface.

Pins in port 1 can drive one TTL load and a 90-pF capacitive load. They can also drive an LED or a darlington transistor pair.

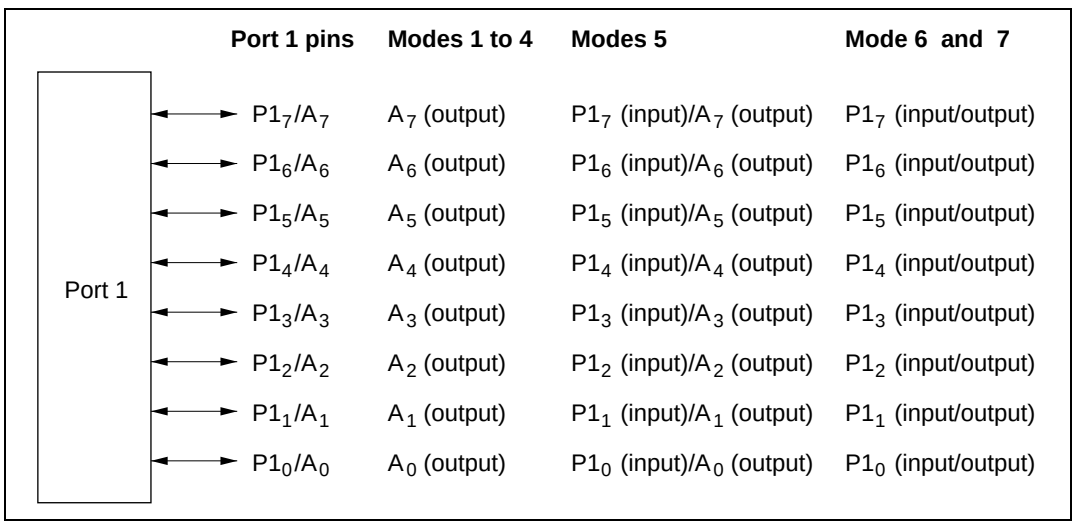


Figure 8.1 Port 1 Pin Configuration

becomes an output port if the corresponding bit of $P6_6DDR$ to $P6_0DDR$ is set to 1, and an input port if this pin is cleared to 0.

P6DDR is a write-only register. Its value cannot be read. All bits return 1 when read.

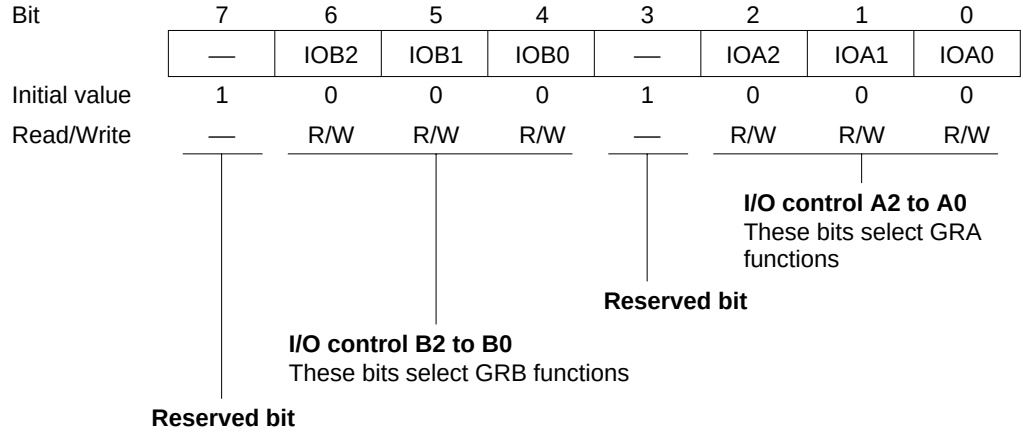
P6DDR is initialized to H'80 by a reset and in hardware standby mode. In software standby mode it retains its previous setting. Therefore, if a transition is made to software standby mode while port 6 is functioning as an input/output port and a P6DDR bit is set to 1, the corresponding pin maintains its output state.

Port 6 Data Register (P6DR): P6DR is an 8-bit readable/writable register that stores output data for port 6. When port 6 functions as an output port, the value of this register is output. For bit 7, a value of 1 is returned if the bit is read while the PSTOP bit in MSTCRH is cleared to 0, and the $P6_7$ pin logic level is returned if the bit is read while the PSTOP bit is set to 1. Bit 7 cannot be modified. For bits 6 to 0, the pin logic level is returned if the bit is read while the corresponding bit in P6DDR is cleared to 0, and the P6DR value is returned if the bit is read while the corresponding bit in P6DDR is set to 1.

Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	1	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 6 data 7 to 0
These bits store data for port 6 pins

P6DR is initialized to H'80 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.



Each TIOR is an 8-bit readable/writable register that selects the output compare or input capture function for GRA and GRB, and specifies the functions of the TIORA and TIORC pins. If the output compare function is selected, TIOR also selects the type of output. If input capture is selected, TIOR also selects the edge or edges of the input capture signal.

TIOR is initialized to H'88 by a reset and in standby mode.

Bit 7—Reserved: This bit cannot be modified and is always read as 1.

Bits 6 to 4—I/O Control B2 to B0 (IOB2 to IOB0): These bits select the GRB function.

Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	Function		
0	0	0	GRB is an output compare register	No output at compare match	(Initial value)
		1		0 output at GRB compare match*1	
	1	0		1 output at GRB compare match*1	
		1		Output toggles at GRB compare match (1 output in channel 2)*1 *2	
1	0	0	GRB is an input compare register	GRB captures rising edge of input	
		1		GRB captures falling edge of input	
	1	0		GRB captures both edges of input	
		1			

Notes: 1. After a reset, the output conforms to the TOLR setting until the first compare match.
2. Channel 2 output cannot be toggled by compare match. This setting selects 1 output instead.

Bits 7 and 6—Group 3 Compare Match Select 1 and 0 (G3CMS1, G3CMS0): These bits select the compare match event that triggers TPC output group 3 (TP_{15} to TP_{12}).

Bit 7 G3CMS1	Bit 6 G3CMS0	Description
0	0	TPC output group 3 (TP_{15} to TP_{12}) is triggered by compare match in 16-bit timer channel 0
	1	TPC output group 3 (TP_{15} to TP_{12}) is triggered by compare match in 16-bit timer channel 1
1	0	TPC output group 3 (TP_{15} to TP_{12}) is triggered by compare match in 16-bit timer channel 2
	1	TPC output group 3 (TP_{15} to TP_{12}) is triggered by compare match in 16-bit timer channel 2 (Initial value)

Bits 5 and 4—Group 2 Compare Match Select 1 and 0 (G2CMS1, G2CMS0): These bits select the compare match event that triggers TPC output group 2 (TP_{11} to TP_{8}).

Bit 5 G2CMS1	Bit 4 G2CMS0	Description
0	0	TPC output group 2 (TP_{11} to TP_{8}) is triggered by compare match in 16-bit timer channel 0
	1	TPC output group 2 (TP_{11} to TP_{8}) is triggered by compare match in 16-bit timer channel 1
1	0	TPC output group 2 (TP_{11} to TP_{8}) is triggered by compare match in 16-bit timer channel 2
	1	TPC output group 2 (TP_{11} to TP_{8}) is triggered by compare match in 16-bit timer channel 2 (Initial value)

12.4 Interrupts

During interval timer operation, an overflow generates an interval timer interrupt (WOVI). The interval timer interrupt is requested whenever the OVF bit is set to 1 in TCSR.

12.5 Usage Notes

Contention between TCNT Write and Increment: If a timer counter clock pulse is generated during the T_3 state of a write cycle to TCNT, the write takes priority and the timer count is not incremented. See figure 12.8.

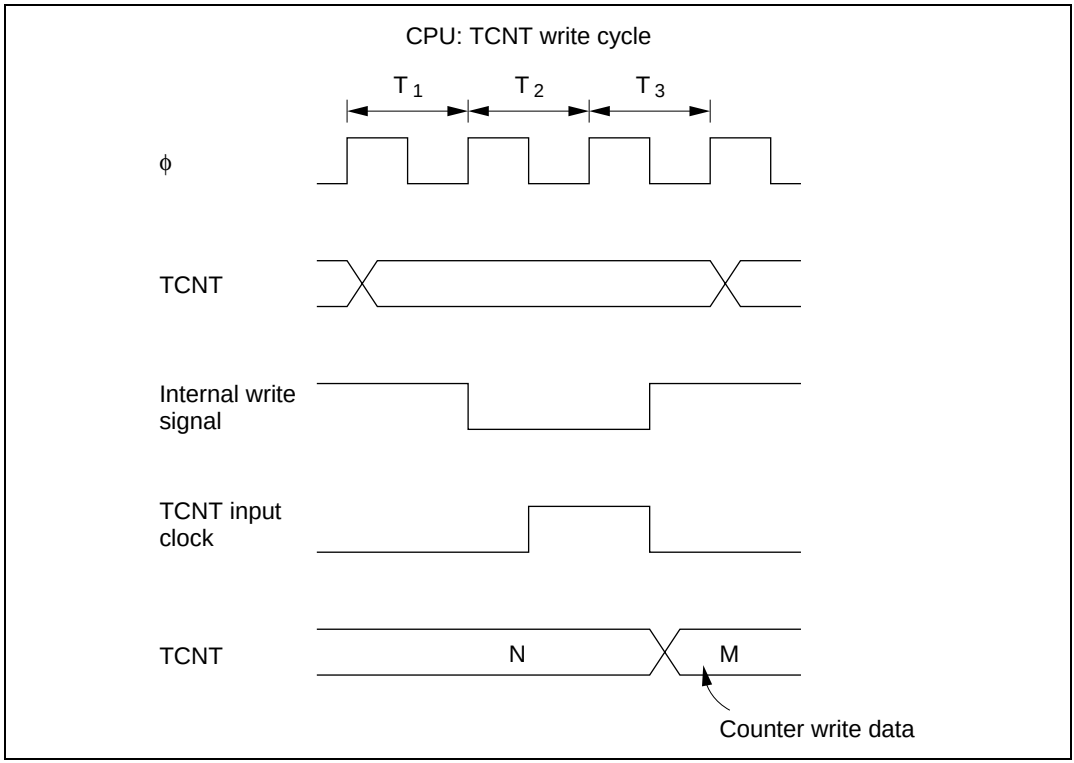


Figure 12.8 Contention between TCNT Write and Count up

Changing CKS2 to CKS0 Bit: Halt TCNT by clearing the TME bit to 0 in TCSR before changing the values of bits CKS2 to CKS0.

Bit 2—Smart Card Data Invert (SINV): Specifies inversion of the data logic level. This function is used in combination with the SDIR bit to communicate with inverse-convention cards.*2 The SINV bit does not affect the logic level of the parity bit. For parity settings, see section 14.3.4, Register Settings.

Bit 2 SINV	Description	
0	Unmodified TDR contents are transmitted	(Initial value)
	Receive data is stored unmodified in RDR	
1	Inverted TDR contents are transmitted	
	Receive data is inverted before storage in RDR	

Bit 1—Reserved: Read-only bit, always read as 1.

Bit 0—Smart Card Interface Mode Select (SMIF): Enables the smart card interface function.

Bit 0 SMIF	Description	
0	Smart card interface function is disabled	(Initial value)
1	Smart card interface function is enabled	

Notes: 1. The function for switching between LSB-first and MSB-first mode can also be used with the normal serial communication interface. Note that when the communication format data length is set to 7 bits and MSB-first mode is selected for the serial data to be transferred, bit 0 of TDR is not transmitted, and only bits 7 to 1 of the received data are valid.

2. The data logic level inversion function can also be used with the normal serial communication interface. Note that, when inverting the serial data to be transferred, parity transmission and parity checking is based on the number of high-level periods at the serial data I/O pin, and not on the register value.

Table 18.15 AC Characteristics in Transition from Memory Read Mode to Another Mode

(Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, T_a = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	t_{nxtc}	20	—	µs	
$\overline{CE}$ hold time	t_{ceh}	0	—	ns	
$\overline{CE}$ setup time	t_{ces}	0	—	ns	
Data hold time	t_{dh}	50	—	ns	
Data setup time	t_{ds}	50	—	ns	
Write pulse width	t_{wep}	70	—	ns	
$\overline{WE}$ rise time	t_r	—	30	ns	
$\overline{WE}$ fall time	t_f	—	30	ns	

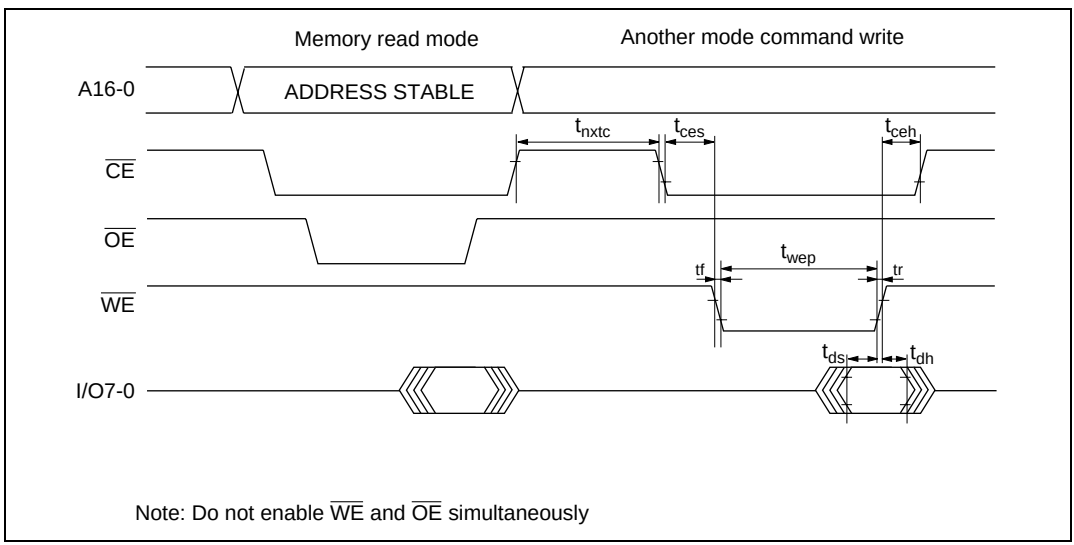
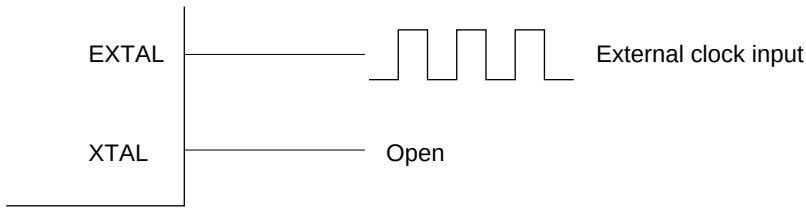


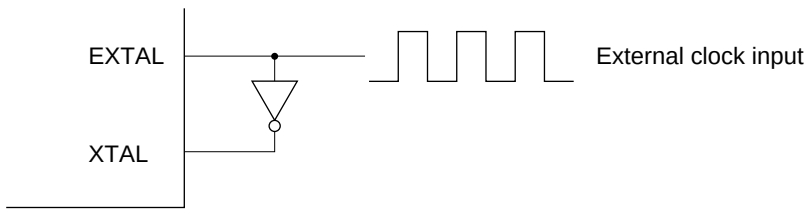
Figure 18.19 Transition From Memory Read Mode to Another Mode

19.2.2 External Clock Input

Circuit Configuration: An external clock signal can be input as shown in the examples in figure 19.5. If the XTAL pin is left open, the stray capacitance should not exceed 10 pF. If the stray capacitance at the XTAL pin exceeds 10 pF in configuration a, use configuration b instead and hold the clock high in standby mode.



a. XTAL pin left open



b. Complementary clock input at XTAL pin

Figure 19.5 External Clock Input (Examples)

Table 21.2 DC Characteristics (3)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 to 5.5 V, V_{REF} = 3.0 V to AV_{CC} *1,
V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port 7		$V_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	
	Ports 1 to 6 $P8_3$, $P8_4$, $P9_0$ to $P9_5$, port B		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 1 to 7 $P8_3$, $P8_4$, $P9_0$ to $P9_5$, port B		–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
					0.8	V	V_{CC} = 4.0 to 5.5 V
Output high voltage	All output pins (except $\overline{RESO}$)	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, 2, and 5		—	—	1.0	V	I_{OL} = 5 mA (V_{CC} < 4.0 V)
							I_{OL} = 10 mA (V_{CC} = 4.0 to 5.5 V)
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{STBY}$, $\overline{RES}$, NMI, MD_2 to MD_0	$\|I_{in}\|$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	Port 7		—	—	1.0	µA	V_{in} = 0.5 V to AV_{CC} – 0.5 V

Condition Code Notation

Symbol	Description
↕	Changed according to execution result
*	Undetermined (no guaranteed value)
0	Cleared to 0
1	Set to 1
—	Not affected by execution of the instruction
Δ	Varies depending on conditions, described in notes

DRCRB—DRAM Control Register B	H'EE027	DRAM interface

Bit	7	6	5	4	3	2	1	0
	MXC1	MXC0	CSEL	RCYCE	—	TPC	RCW	RLW
Initial value	0	0	0	0	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W

Refresh cycle wait control

0	Wait state (T_{RW}) insertion is disabled
1	1 wait state (T_{RW}) is inserted

$\overline{RAS}$-$\overline{CAS}$ wait

0	Wait state (T_{rw}) insertion is disabled
1	1 wait state (T_{rw}) is inserted

TP cycle control

0	1-state precharge cycle is inserted
1	2-state precharge cycle is inserted

Refresh cycle enable

0	Refresh cycles are disabled
1	DRAM refresh cycles are enabled

$\overline{CAS}$ output pin select

0	PB4 and PB5 selected as $\overline{UCAS}$ and $\overline{LCAS}$ output pins
1	$\overline{HWR}$ and $\overline{LWR}$ selected as $\overline{UCAS}$ and $\overline{LCAS}$ output pins

Multiplex control 1 and 0

MXC1	MXC0	Description		
0	0	Column address: 8 bits		
		Compared address:		
		Modes 1, 2	8-bit access space	A_{19} to A_8
			16-bit access space	A_{19} to A_9
		Modes 3, 4, 5	8-bit access space	A_{23} to A_8
			16-bit access space	A_{23} to A_9
	1	Column address: 9 bits		
		Compared address:		
		Modes 1, 2	8-bit access space	A_{19} to A_9
			16-bit access space	A_{19} to A_{10}
		Modes 3, 4, 5	8-bit access space	A_{23} to A_9
			16-bit access space	A_{23} to A_{10}
1	0	Column address: 10 bits		
		Compared address:		
		Modes 1, 2	8-bit access space	A_{19} to A_{10}
			16-bit access space	A_{19} to A_{11}
		Modes 3, 4, 5	8-bit access space	A_{23} to A_{10}
			16-bit access space	A_{23} to A_{11}
	1	Illegal setting		

FLMCR-Flash Memory Control Register | H'EE030 | Flash Memory

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	ESU	PSU	EV	PV	E	P
Modes 1 to 4, and 6 — Initial value	0	0	0	0	0	0	0	0
Modes 1 to 4, and 6 — Read/Write	R	R	R	R	R	R	R	R
Modes 5 and 7 — Initial value	1/0	0	0	0	0	0	0	0
Modes 5 and 7 — Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program mode

0	Program mode cleared (Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1

Erase mode

0	Erase mode cleared (Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1

Program-verify mode

0	Program-verify mode cleared (Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE = 1

Erase-verify mode

0	Erase-verify mode cleared (Initial value)
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE = 1

Program setup

0	Program setup cleared (Initial value)
1	Program setup [Setting condition] When FWE = 1 and SWE = 1

Erase setup bit

0	Erase setup cleared (Initial value)
1	Erase setup [Setting condition] When FWE = 1 and SWE = 1

Software write enable bit

0	Write/erase disabled (Initial value)
1	Write/erase enabled [Setting condition] When FWE = 1

Flash write enable bit

0	When a low level is input to the FWE pin (hardware protection state)
1	When a high level is input to the FWE pin

Note: This register is used only in the flash memory and flash memory R versions. Reading the corresponding address in a mask ROM version will always return 1s, and writes to this address are disabled. Fix the FWE pin low in mode 6.

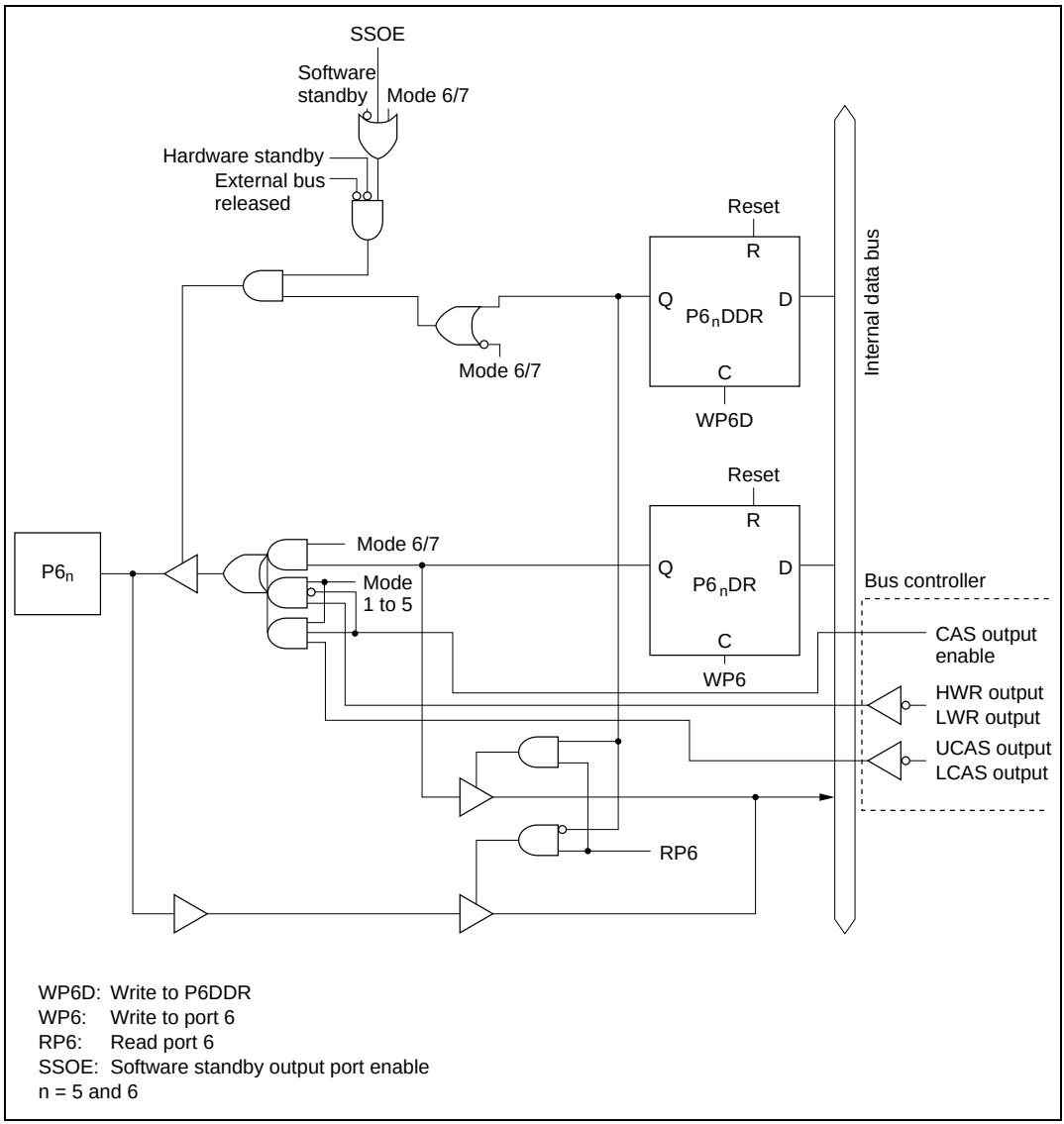


Figure C.6 (f) Port 6 Block Diagram (Pins $P6_5$ and $P6_6$)