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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	13MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3067rvf13v

Bit 2—Priority Level B2 (IPRB2): Selects the priority level of SCI channel 1 interrupt requests.

Bit 2 IPRB2	Description	
0	SCI1 interrupt requests have priority level 0 (low priority)	(Initial value)
1	SCI1 interrupt requests have priority level 1 (high priority)	

Bit 1—Priority Level B1 (IPRB1): Selects the priority level of SCI channel 2 interrupt requests.

Bit 1 IPRB1	Description	
0	SCI channel 2 interrupt requests have priority level 0 (low priority)	(Initial value)
1	SCI channel 2 interrupt requests have priority level 1 (high priority)	

Bit 0—Reserved: This bit can be written and read, but it does not affect interrupt priority.

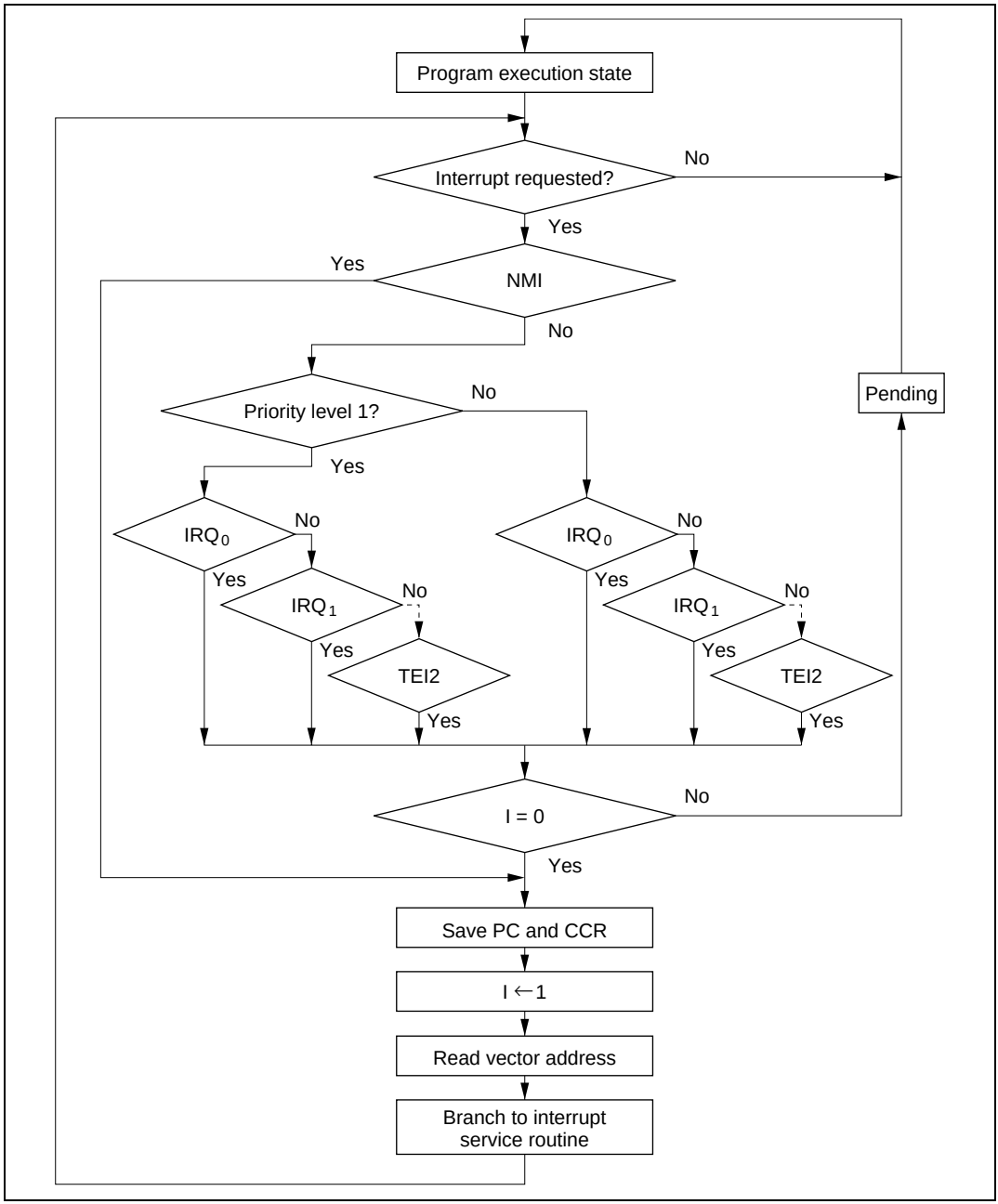


Figure 5.4 Process Up to Interrupt Acceptance when UE = 1

6.7 Interrupt Sources

Compare match interrupts (CMI) can be generated when the refresh timer is used as an interval timer. Compare match interrupt requests are masked/unmasked with the CMIE bit in RTMCSR.

6.8 Burst ROM Interface

6.8.1 Overview

With the H8/3067 Group, external space area 0 can be designated as burst ROM space, and burst ROM space interfacing can be performed. The burst ROM space interface enables 16-bit organization ROM with burst access capability to be accessed at high speed. Area 0 is designated as burst ROM space by means of the BROME bit in BCR.

Continuous burst access of a maximum or four or eight words can be performed on external space area 0. Two or three states can be selected for burst access.

6.8.2 Basic Timing

The number of states in the initial cycle (full access) and a burst cycle of the burst ROM interface is determined by the setting of the AST0 bit in ASTCR. When the AST0 bit is set to 1, wait states can also be inserted in the initial cycle. Wait states cannot be inserted in a burst cycle.

Burst access of up to four words is performed when the BRSTS0 bit is cleared to 0 in BCR, and burst access of up to eight words when the BRSTS0 bit is set to 1. The number of burst access states is two when the BRSTS1 bit is cleared to 0, and three when the BRSTS1 bit is set to 1.

The basic access timing for burst ROM space is shown in figure 6.42.

7.2 Register Descriptions (1) (Short Address Mode)

In short address mode, transfers can be carried out independently on channels A and B. Short address mode is selected by bits DTS2A and DTS1A in data transfer control register A (DTCRA) as indicated in table 7.4.

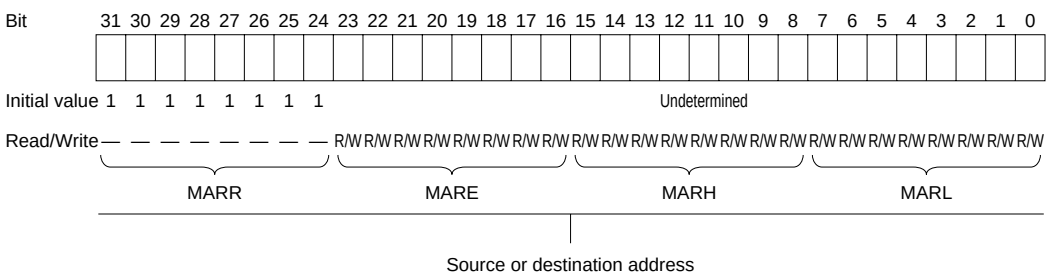
Table 7.4 Selection of Short and Full Address Modes

Channel	Bit 2 DTS2A	Bit 1 DTS1A	Description
0	1	1	DMAC channel 0 operates as one channel in full address mode
	Other than above		DMAC channels 0A and 0B operate as two independent channels in short address mode
1	1	1	DMAC channel 1 operates as one channel in full address mode
	Other than above		DMAC channels 1A and 1B operate as two independent channels in short address mode

7.2.1 Memory Address Registers (MAR)

A memory address register (MAR) is a 32-bit readable/writable register that specifies a source or destination address. The transfer direction is determined automatically from the activation source.

An MAR consists of four 8-bit registers designated MARR, MARE, MARH, and MARL. All bits of MARR are reserved; they cannot be modified and are always read as 1.



An MAR functions as a source or destination address register depending on how the DMAC is activated: as a destination address register if activation is by a receive-data-full interrupt from serial communication interface (SCI) channel 0 or by an A/D converter conversion-end interrupt, and as a source address register otherwise.

The MAR value is incremented or decremented each time one byte or word is transferred, automatically updating the source or destination memory address. For details, see section 7.3.4, Data Transfer Control Registers (DTCR).

Table 7.8 Register Functions in Repeat Mode

Register	Function: Activated by SCI 0 Receive-Data-Full Interrupt or by A/D Converter Conversion-End Interrupt	Function: Other Activation	Initial Setting	Operation
23 MAR 0	Destination address register	Source address register	Destination or source start address	Incremented or decremented at each transfer until ETCRH reaches H'0000, then restored to initial value
23 All 1s 7 IOAR 0	Source address register	Destination address register	Source or destination address	Held fixed
7 ETCRH 0	Transfer counter		Number of transfers	Decremented once per transfer until H'0000 is reached, then reloaded from ETCRL
7 ETCRL 0	Initial transfer count		Number of transfers	Held fixed

Legend

MAR: Memory address register

IOAR: I/O address register

ETCR: Execute transfer count register

In repeat mode ETCRH is used as the transfer counter while ETCRL holds the initial transfer count. ETCRH is decremented by 1 at each transfer until it reaches H'00, then is reloaded from ETCRL. MAR is also restored to its initial value, which is calculated from the DTSZ and DTID bits in DTCR. Specifically, MAR is restored as follows:

$$MAR \leftarrow MAR - (-1)^{DTID} \bullet 2^{DTSZ} \bullet ETCRL$$

ETCRH and ETCRL should be initially set to the same value.

Figure 7.18 shows the timing when the DMAC is activated by the falling edge of $\overline{\text{DREQ}}$ in block transfer mode.

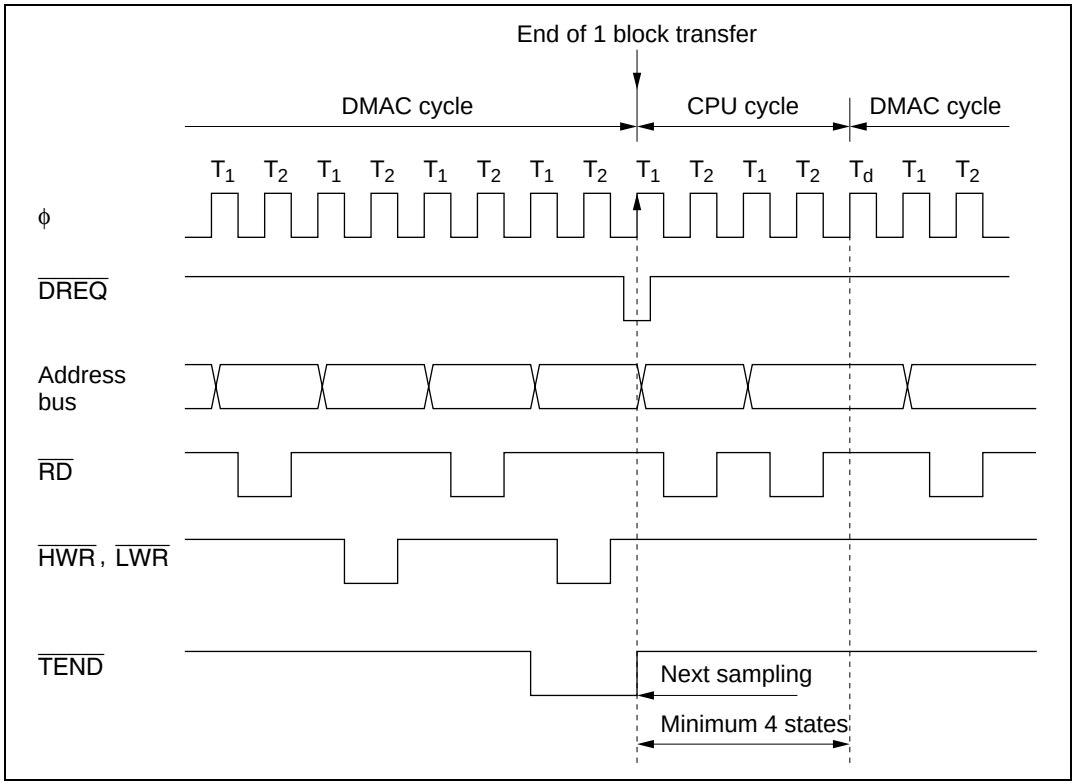


Figure 7.18 Timing of DMAC Activation by Falling Edge of $\overline{\text{DREQ}}$ in Block Transfer Mode

8.5 Port 4

8.5.1 Overview

Port 4 is an 8-bit input/output port with the pin configuration shown in figure 8.4. The pin functions differ depending on the operating mode.

In modes 1 to 5 (expanded modes), when the bus width control register (ABWCR) designates areas 0 to 7 all as 8-bit-access areas, the chip operates in 8-bit bus mode and port 4 is a generic input/output port. When at least one of areas 0 to 7 is designated as a 16-bit-access area, the chip operates in 16-bit bus mode and port 4 becomes part of the data bus. In mode 6, 7 (single-chip mode), port 4 is a generic input/output port.

Port 4 has software-programmable built-in pull-up transistors.

Pins in port 4 can drive one TTL load and a 90-pF capacitive load. They can also drive a darlington transistor pair.

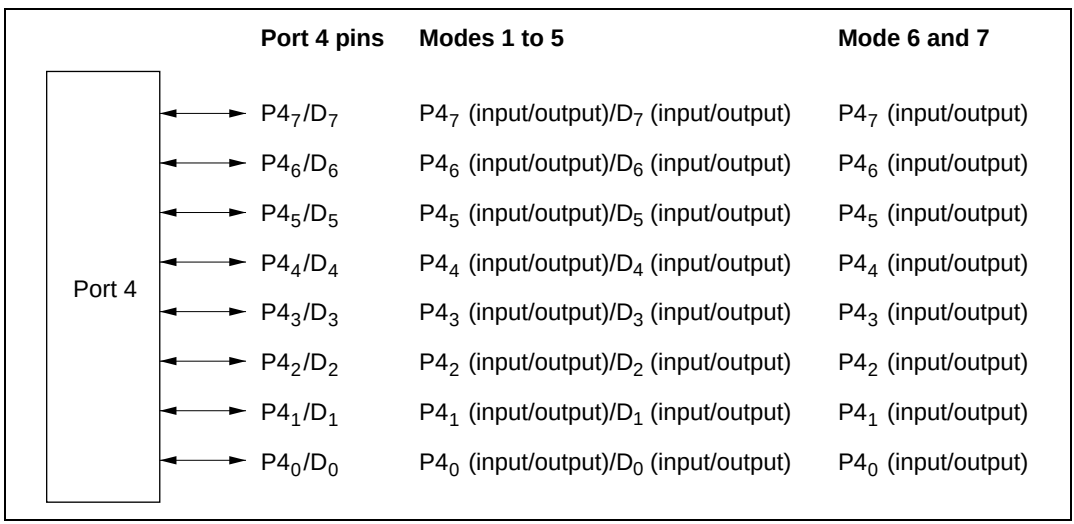


Figure 8.4 Port 4 Pin Configuration

Pin	Pin Functions and Selection Method

$PA_5/TP_5/TIOCB_1/A_{22}$

Bit PWM1 in TMDR, bits IOB2 to IOB0 in TIOR1, bit NDER5 in NDERA, bit A22E in BRCR, and bit PA_5DDR select the pin function as follows.

A22E	1				0
16-bit timer channel 1 settings	(1) in table below	(2) in table below			—
PA_5DDR	—	0	1	1	—
NDER5	—	—	0	1	—
Pin function	$TIOCB_1$ output	PA_5 input	PA_5 output	TP_5 output	A_{22} output
		$TIOCB_1$ input*			

Note: * $TIOCB_1$ input when IOB2 = 1 and PWM1 = 0.

16-bit timer channel 1 settings	(2)	(1)		(2)
IOB2	0			1
IOB1	0	0	1	—
IOB0	0	1	—	—

$PA_4/TP_4/TIOCA_1/A_{23}$

Bit PWM1 in TMDR, bits IOA2 to IOA0 in TIOR1, bit NDER4 in NDERA, bit A23E in BRCR, and bit PA_4DDR select the pin function as follows.

A23E	1				0
16-bit timer channel 1 settings	(1) in table below	(2) in table below			—
PA_4DDR	—	0	1	1	—
NDER4	—	—	0	1	—
Pin function	$TIOCA_1$ output	PA_4 input	PA_4 output	TP_4 output	A_{23} output
		$TIOCA_1$ input*			

Note: * $TIOCA_1$ input when IOA2 = 1.

16-bit timer channel 1 settings	(2)	(1)		(2)	(1)
PWM1	0				1
IOA2	0			1	—
IOA1	0	0	1	—	—
IOA0	0	1	—	—	—

Bits 3 and 2—Output/Input Capture Edge Select B3 and B2 (OIS3, OIS2): In combination with the ICE bit in TCSR1 (TCSR3), these bits select the compare match B output level or the input capture input detected edge.

The function of TCORB1 (TCORB3) depends on the setting of bit 4 of TCSR1 (TCSR3). TCORB0 and TCORB2 function as compare match registers regardless of the setting of bit 4 of TCSR1 (TCSR3).

ICE Bit in TCSR1 (TCSR3)	Bit 3 OIS3	Bit 2 OIS2	Description	
0	0	0	No change when compare match B occurs	(Initial value)
		1	0 is output when compare match B occurs	
	1	0	1 is output when compare match B occurs	
		1	Output is inverted when compare match B occurs (toggle output)	
1	0	0	TCORB input capture on rising edge	
		1	TCORB input capture on falling edge	
	1	0	TCORB input capture on both rising and falling edges	
		1		

- When the compare match register function is used, the timer output priority order is: toggle output > 1 output > 0 output.
- If compare match A and B occur simultaneously, the output changes in accordance with the higher-priority compare match.
- When bits OIS3, OIS2, OS1, and OS0 are all cleared to 0, timer output is disabled.

Bits 1 and 0—Output Select A1 and A0 (OS1, OS0): These bits select the compare match A output level.

Bit 1 OS1	Bit 0 OS0	Description	
0	0	No change when compare match A occurs	(Initial value)
	1	0 is output when compare match A occurs	
1	0	1 is output when compare match A occurs	
	1	Output is inverted when compare match A occurs (toggle output)	

- When the compare match register function is used, the timer output priority order is: toggle output > 1 output > 0 output.

Bit Rate (bit/s)	φ (MHz)											
	9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

Bit Rate (bit/s)	φ (MHz)																	
	13			14			14.7456			16			18			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	230	–0.08	2	248	–0.17	3	64	0.70	3	70	0.03	3	79	–0.12	3	88	–0.25
150	2	168	0.16	2	181	0.16	2	191	0.00	2	207	0.16	2	233	0.16	3	64	0.16
300	2	84	–0.43	2	90	0.16	2	95	0.00	2	103	0.16	2	116	0.16	2	129	0.16
600	1	168	0.16	1	181	0.16	1	191	0.00	1	207	0.16	1	233	0.16	2	64	0.16
1200	1	84	–0.43	1	90	0.16	1	95	0.00	1	103	0.16	1	116	0.16	1	129	0.16
2400	0	168	0.16	0	181	0.16	0	191	0.00	0	207	0.16	0	233	0.16	1	64	0.16
4800	0	84	–0.43	0	90	0.16	0	95	0.00	0	103	0.16	0	116	0.16	0	129	0.16
9600	0	41	0.76	0	45	–0.93	0	47	0.00	0	51	0.16	0	58	–0.69	0	64	0.16
19200	0	20	0.76	0	22	–0.93	0	23	0.00	0	25	0.16	0	28	1.02	0	32	–1.36
31250	0	12	0.00	0	13	0.00	0	14	–1.70	0	15	0.00	0	17	0.00	0	19	0.00
38400	0	10	–3.82	0	10	3.57	0	11	0.00	0	12	0.16	0	14	–2.34	0	15	1.73

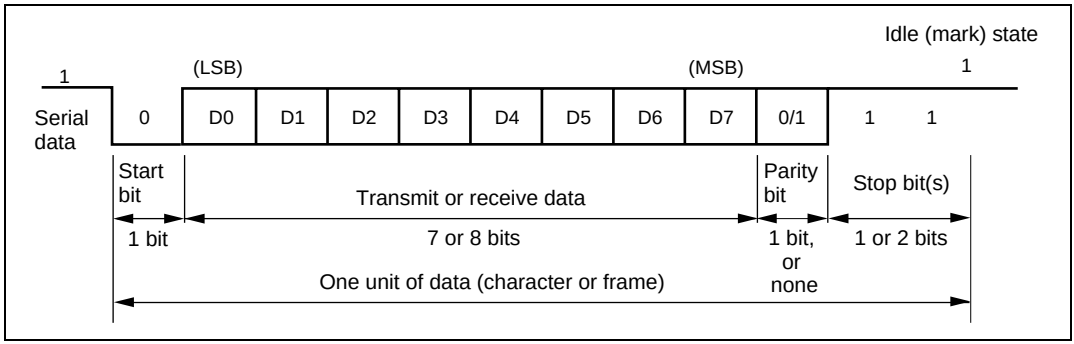


Figure 13.2 Data Format in Asynchronous Communication (Example: 8-Bit Data with Parity and 2 Stop Bits)

Communication Formats: Table 13.10 shows the 12 communication formats that can be selected in asynchronous mode. The format is selected by settings in SMR.

Bit 2—Smart Card Data Invert (SINV): Specifies inversion of the data logic level. This function is used in combination with the SDIR bit to communicate with inverse-convention cards.*2 The SINV bit does not affect the logic level of the parity bit. For parity settings, see section 14.3.4, Register Settings.

Bit 2 SINV	Description	
0	Unmodified TDR contents are transmitted	(Initial value)
	Receive data is stored unmodified in RDR	
1	Inverted TDR contents are transmitted	
	Receive data is inverted before storage in RDR	

Bit 1—Reserved: Read-only bit, always read as 1.

Bit 0—Smart Card Interface Mode Select (SMIF): Enables the smart card interface function.

Bit 0 SMIF	Description	
0	Smart card interface function is disabled	(Initial value)
1	Smart card interface function is enabled	

Notes: 1. The function for switching between LSB-first and MSB-first mode can also be used with the normal serial communication interface. Note that when the communication format data length is set to 7 bits and MSB-first mode is selected for the serial data to be transferred, bit 0 of TDR is not transmitted, and only bits 7 to 1 of the received data are valid.

2. The data logic level inversion function can also be used with the normal serial communication interface. Note that, when inverting the serial data to be transferred, parity transmission and parity checking is based on the number of high-level periods at the serial data I/O pin, and not on the register value.

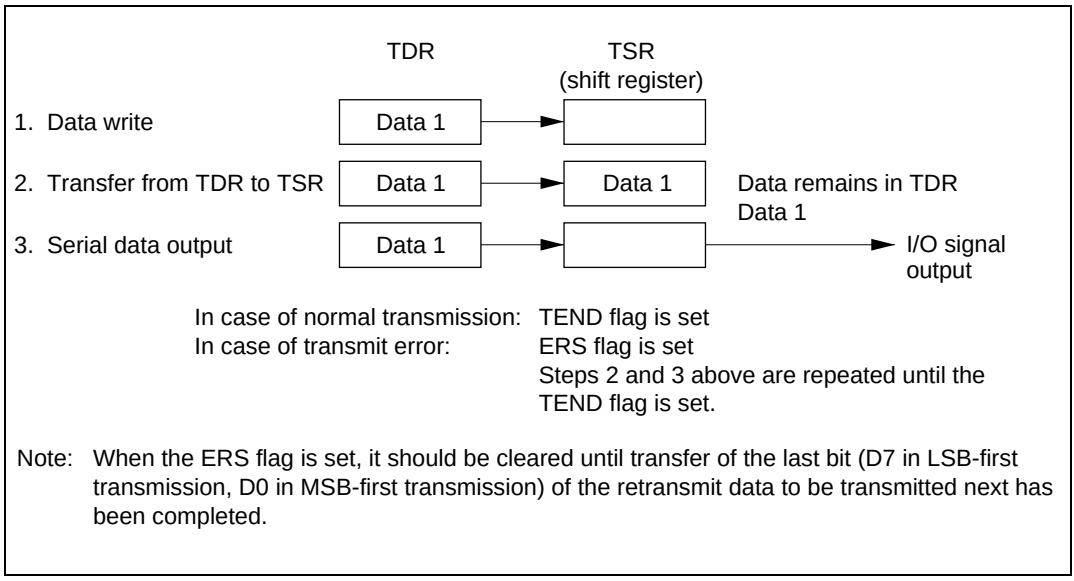


Figure 14.6 Relation Between Transmit Operation and Internal Registers

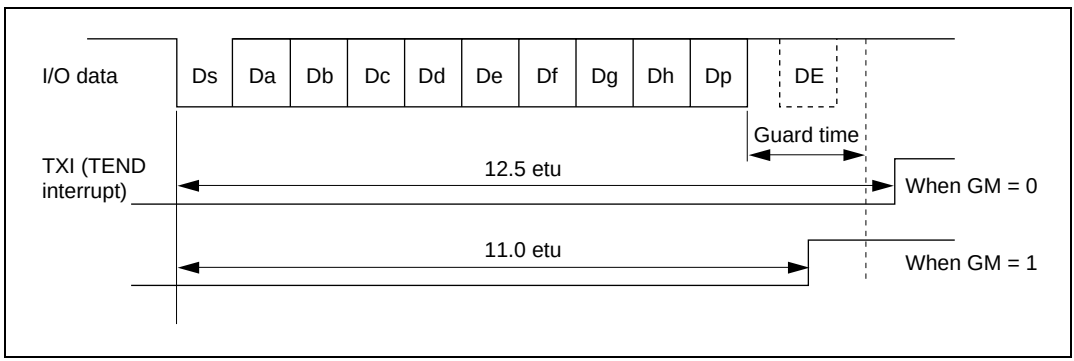


Figure 14.7 Timing of TEND Flag Setting

Receiving Serial Data: Data reception in smart card mode uses the same processing procedure as for the normal SCI. Figure 14.8 shows a sample reception processing flowchart.

1. Perform smart card interface mode initialization as described in Initialization above.
2. Check that the ORER flag and PER flag are cleared to 0 in SSR. If either is set, perform the appropriate receive error handling, then clear both the ORER and the PER flag to 0.
3. Repeat steps 2 and 3 until it can be confirmed that the RDRF flag is set to 1.
4. Read the receive data from RDR.
5. To continue receiving data, clear the RDRF flag to 0 and go back to step 2.

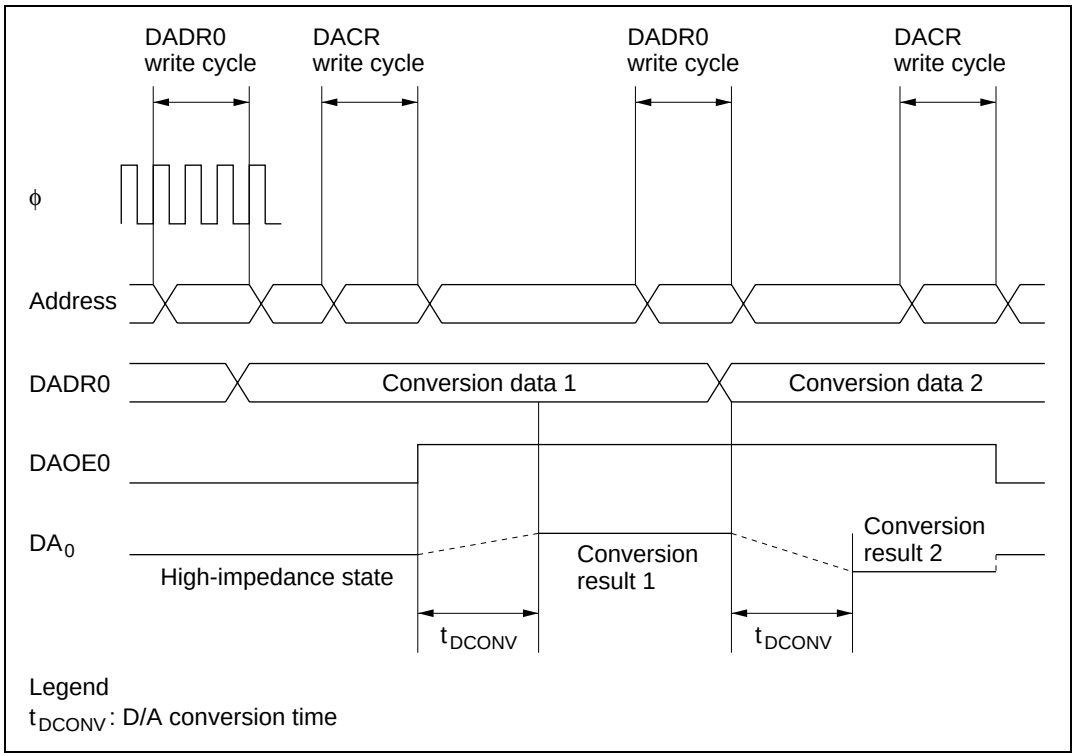


Figure 16.2 Example of D/A Converter Operation

16.4 D/A Output Control

In the H8/3067 Group, D/A converter output can be enabled or disabled in software standby mode.

When the DASTE bit is set to 1 in DASTCR, D/A converter output is enabled in software standby mode. The D/A converter registers retain the values they held prior to the transition to software standby mode.

When D/A output is enabled in software standby mode, the reference supply current is the same as during normal operation.

18.2.3 Pin Configuration

The flash memory is controlled by means of the pins shown in table 18.2.

Table 18.2 Flash Memory Pins

Pin Name	Abbreviation	I/O	Function
Reset	$\overline{\text{RES}}$	Input	Reset
Flash write enable	FWE*	Input	Flash program/erase protection by hardware
Mode 2	MD_2	Input	Sets this LSI operating mode
Mode 1	MD_1	Input	Sets this LSI operating mode
Mode 0	MD_0	Input	Sets this LSI operating mode
Transmit data	TxD_1	Output	Serial transmit data output
Receive data	RxD_1	Input	Serial receive data input

Note: The transmit data and receive data pins are used in boot mode.
* In the mask ROM versions, the FWE pin functions as the $\overline{\text{RESO}}$ pin.

18.2.4 Register Configuration

The registers used to control the on-chip flash memory when enabled are shown in table 18.3.

Table 18.3 Flash Memory Registers

Register Name	Abbreviation	R/W	Initial Value	Address*1
Flash memory control register	FLMCR	R/W	H'00*2	H'EE030
Erase block register	EBR	R/W	H'00	H'EE032
RAM control register	RAMCR	R/W	H'F1	H'EE077
Flash memory status register	FLMSR	R	H'7F	H'EE07D

Notes: 1. Lower 20 bits of address in advanced mode.
2. When a high level is input to the FWE pin, the initial value is H'80.

The registers in table 18.3 are used in the flash memory and flash memory R versions only. Reading the corresponding addresses in a mask ROM version will always return 1s, and writes to these addresses are disabled.

18.8 Flash Memory PROM Mode

18.8.1 PROM Mode Setting

This LSI has a PROM mode, besides an on-board programming mode, as a flash memory program/erase mode. In the PROM mode, a program can be freely written to the on-chip ROM using a PROM writer that supports the Renesas 128kbytes flash memory on-chip microcomputer device type.

For notes on PROM mode use, see sections 18.8.9, Notes on Memory Programming and 18.9, Notes on Flash Memory Programming/Erasing.

18.8.2 Memory Map

Figure 18.15 shows the PROM mode memory map.

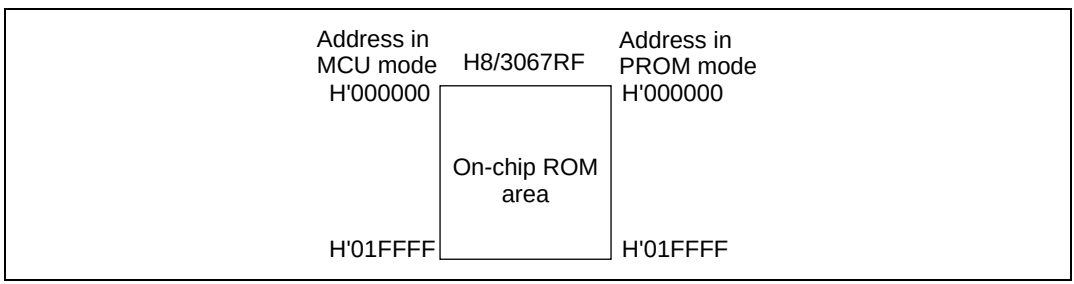


Figure 18.15 PROM Mode Memory Map

18.8.3 PROM Mode Operation

Table 18.10 shows how the different operating modes are set when using PROM mode, and table 18.11 lists the commands used in PROM mode. Details of each mode are given below.

- Memory Read Mode

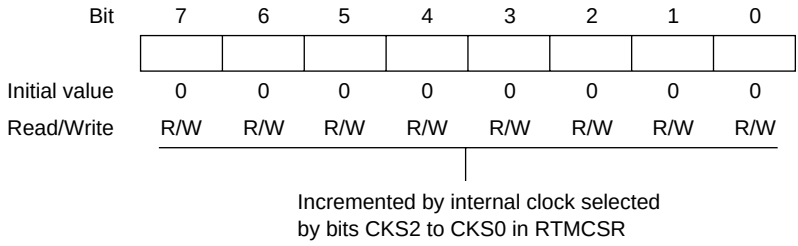
  Memory read mode supports byte reads.
- Auto-Program Mode

  Auto-program mode supports programming of 128 bytes at a time. Status polling is used to confirm the end of auto-programming.
- Auto-Erase Mode

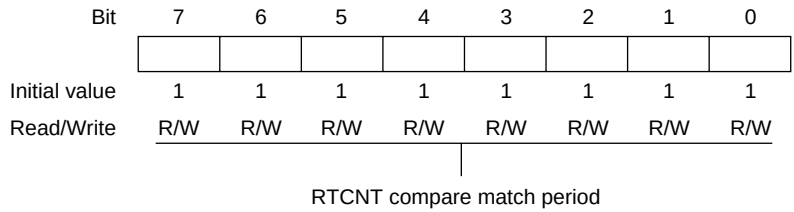
  Auto-erase mode supports automatic erasing of the entire flash memory. Status polling is used to confirm the end of auto-erasing.

Item	Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
$\overline{RAS}$ access time	t_{RAC}	—	2.5 t_{cyc} – 70	—	2.5 t_{cyc} – 40	ns	Figure 21.17 to figure 21.19
Address access time	t_{AA}	—	2.0 t_{cyc} – 80	—	2.0 t_{cyc} – 50	ns	
$\overline{CAS}$ access time	t_{CAC}	—	1.5 t_{cyc} – 80	—	1.5 t_{cyc} – 50	ns	
$\overline{WE}$ setup time	t_{WCS}	0.5 t_{cyc} – 35	—	0.5 t_{cyc} – 20	—	ns	
$\overline{WE}$ hold time	t_{WCH}	0.5 t_{cyc} – 28	—	0.5 t_{cyc} – 15	—	ns	
Write data setup time	t_{WDS}	0.5 t_{cyc} – 35	—	0.5 t_{cyc} – 20	—	ns	
$\overline{WE}$ write data hold time	t_{WDH}	0.5 t_{cyc} – 25	—	0.5 t_{cyc} – 15	—	ns	
$\overline{CAS}$ setup time 1	t_{CSR1}	0.5 t_{cyc} – 25	—	0.5 t_{cyc} – 20	—	ns	
$\overline{CAS}$ setup time 2	t_{CSR2}	0.5 t_{cyc} – 25	—	0.5 t_{cyc} – 15	—	ns	
$\overline{CAS}$ hold time	t_{CHR}	0.5 t_{cyc} – 25	—	0.5 t_{cyc} – 15	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	1.5 t_{cyc} – 25	—	1.5 t_{cyc} – 15	—	ns	

RTCNT—Refresh Timer Counter	H'EE029	DRAM interface



RTCOR—Refresh Time Constant Register	H'EE02A	DRAM interface



Note: Only byte access can be used on this register.

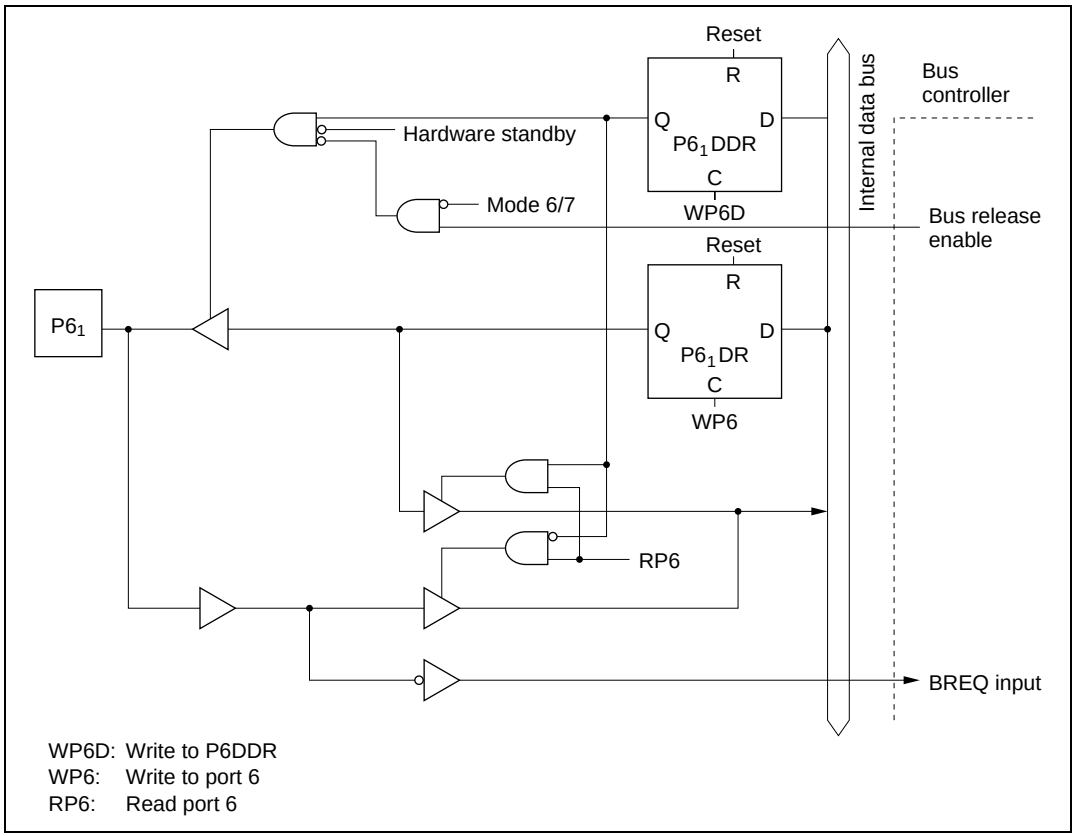


Figure C.6 (b) Port 6 Block Diagram (Pin $P6_1$)

C.9 Port 9 Block Diagrams

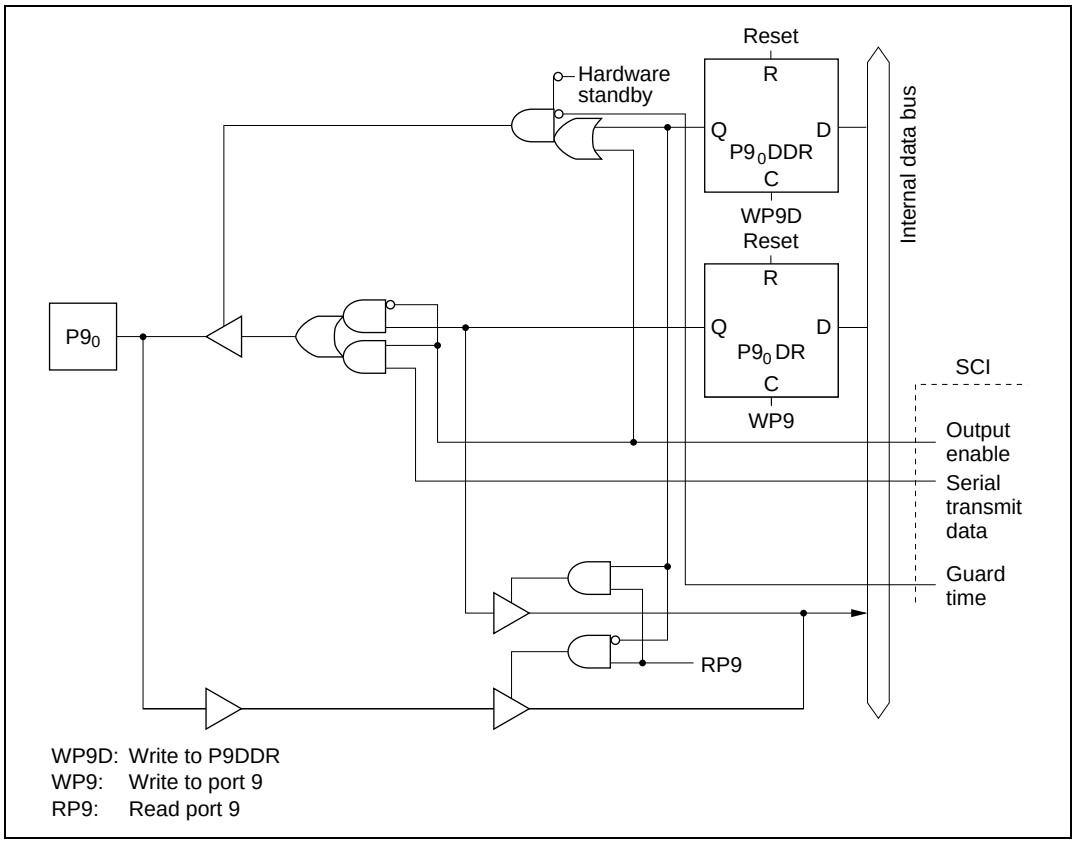


Figure C.9 (a) Port 9 Block Diagram (Pin $P9_0$)