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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	13MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3067rvfi13v

Figure 5.3 shows the timing of the setting of the interrupt flags (IRQnF).

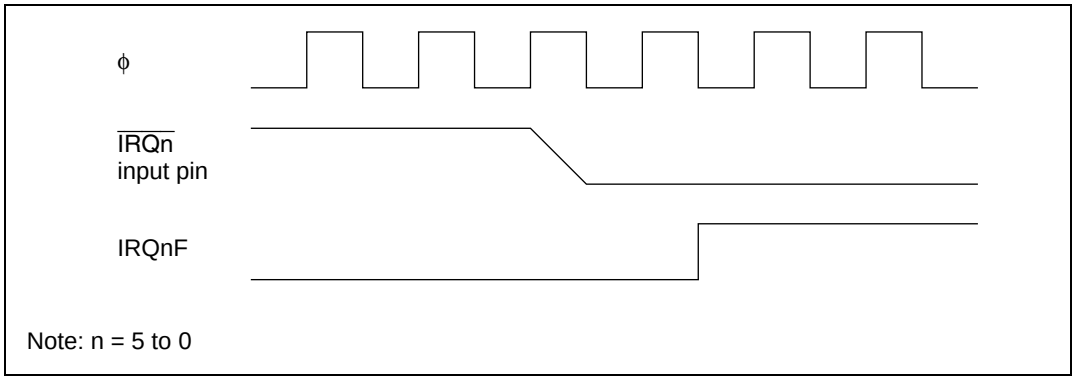


Figure 5.3 Timing of Setting of IRQnF

Interrupts IRQ_0 to IRQ_5 have vector numbers 12 to 17. These interrupts are detected regardless of whether the corresponding pin is set for input or output. When using a pin for external interrupt input, clear its DDR bit to 0 and do not use the pin for chip select output, refresh output, SCI input/output, or A/D external trigger input.

5.3.2 Internal Interrupts

Thirty-Six internal interrupts are requested from the on-chip supporting modules.

- Each on-chip supporting module has status flags for indicating interrupt status, and enable bits for enabling or disabling interrupts.
- Interrupt priority levels can be assigned in IPRA and IPRB.
- 16-bit timer, SCI, and A/D converter interrupt requests can activate the DMAC, in which case no interrupt request is sent to the interrupt controller, and the I and UI bits are disregarded.

5.3.3 Interrupt Vector Table

Table 5.3 lists the interrupt sources, their vector addresses, and their default priority order. In the default priority order, smaller vector numbers have higher priority. The priority of interrupts other than NMI can be changed in IPRA and IPRB. The priority order after a reset is the default order shown in table 5.3.

5.5 Usage Notes

5.5.1 Contention between Interrupt and Interrupt-Disabling Instruction

When an instruction clears an interrupt enable bit to 0 to disable the interrupt, the interrupt is not disabled until after execution of the instruction is completed. If an interrupt occurs while a BCLR, MOV, or other instruction is being executed to clear its interrupt enable bit to 0, at the instant when execution of the instruction ends the interrupt is still enabled, so its interrupt exception handling is carried out. If a higher-priority interrupt is also requested, however, interrupt exception handling for the higher-priority interrupt is carried out, and the lower-priority interrupt is ignored. This also applies to the clearing of an interrupt flag to 0.

Figure 5.8 shows an example in which an IMIEA bit is cleared to 0 in the 16-bit timer's TISRA register.

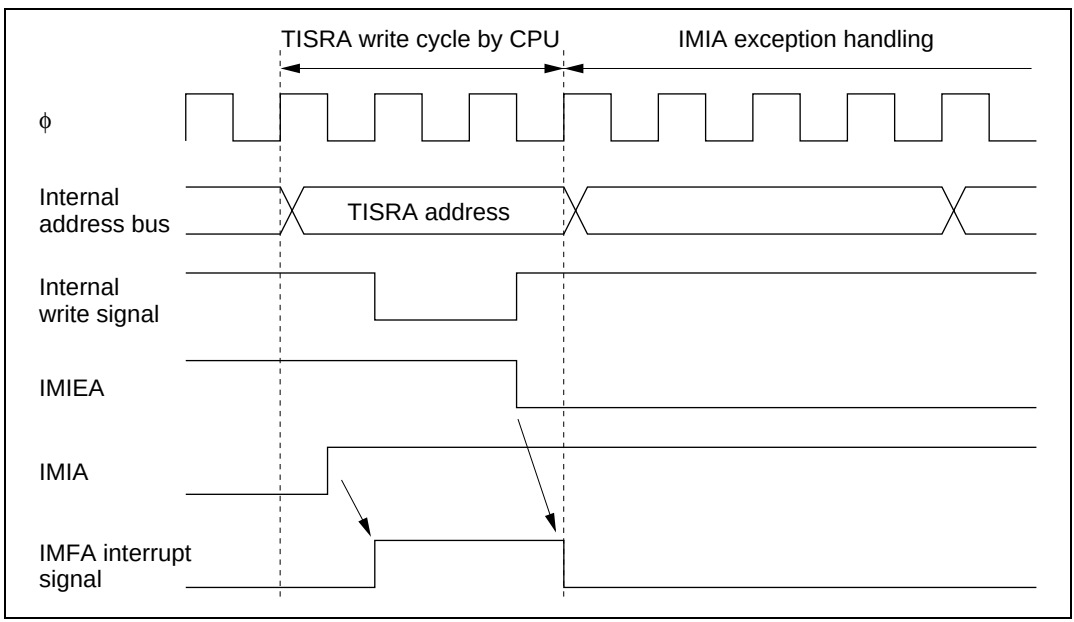


Figure 5.8 Contention between Interrupt and Interrupt-Disabling Instruction

This type of contention will not occur if the interrupt is masked when the interrupt enable bit or flag is cleared to 0.

6.2.9 Refresh Timer Control/Status Register (RTMCSR)

Bit	7	6	5	4	3	2	1	0
	CMF	CMIE	CKS2	CKS1	CKS0	—	—	—
Initial value	0	0	0	0	0	1	1	1
Read/Write	R(W)*	R/W	R/W	R/W	R/W	—	—	—

RTMCSR is an 8-bit readable/writable register that selects the refresh timer counter clock. When the refresh timer is used as an interval timer, RTMCSR also enables or disables interrupt requests. Bits 7 and 6 of RTMCSR are initialized to 0 by a reset and in the standby modes. Bits 5 to 3 are initialized to 0 by a reset and in hardware standby mode; they are not initialized in software standby mode.

Note: Only 0 can be written to clear the flag.

Bit 7—Compare Match Flag (CMF): Status flag that indicates a match between the values of RTCNT and RTCOR.

Bit 7 CMF	Description	
0	Clearing conditions When the chip is reset and in standby mode Read CMF when CMF = 1, then write 0 in CMF	(Initial value)
1	Setting condition When RTCNT = RTCOR	

Bit 6—Compare Match Interrupt Enable (CMIE): Enables or disables the CMI interrupt requested when the CMF flag is set to 1 in RTMCSR. The CMIE bit is always cleared to 0 when any of areas 2 to 5 is designated as DRAM space.

Bit 6 CMIE	Description	
0	The CMI interrupt requested by CMF is disabled	(Initial value)
1	The CMI interrupt requested by CMF is enabled	

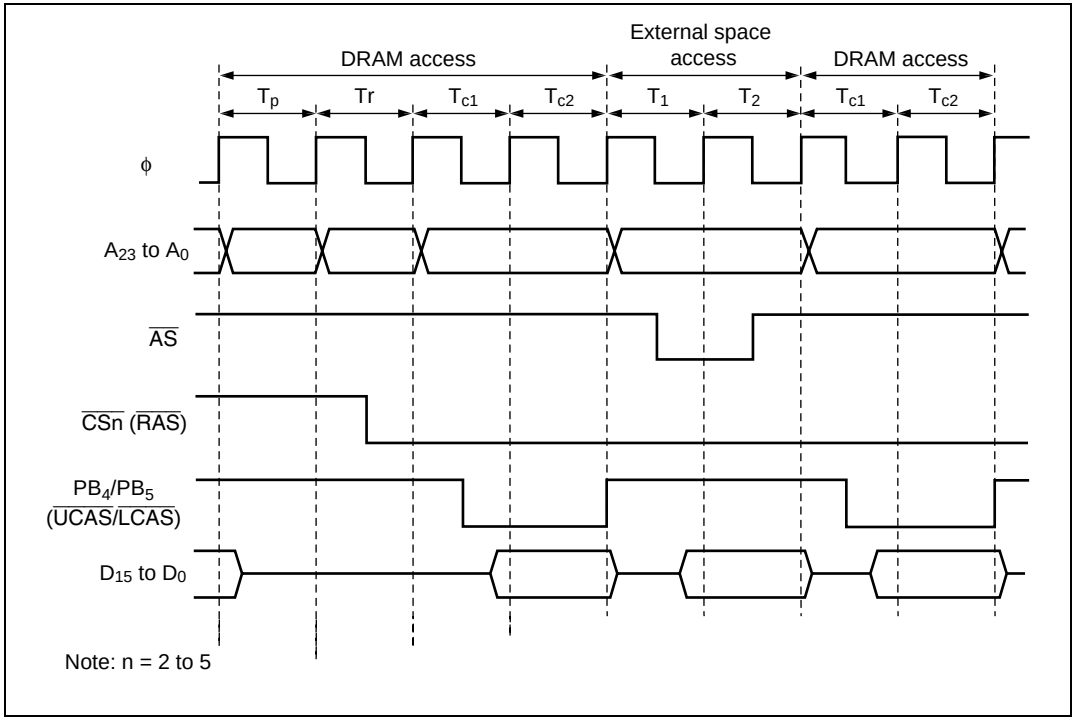


Figure 6.23 Example of Operation Timing in RAS Down Mode (CSEL = 0)

When RAS down mode is selected, the conditions for an asserted $\overline{\text{RAS}}$n signal to return to the high level are as shown below. The timing in these cases is shown in figure 6.24.

— When DRAM space with a different row address is accessed

— Immediately before a CAS-before-RAS refresh cycle

— When the BE bit or RDM bit is cleared to 0 in DRCRA

— Immediately before release of the external bus

6.6 Interval Timer

6.6.1 Operation

When DRAM is not connected to the H8/3067 Group chip, the refresh timer can be used as an interval timer by clearing bits DRAS2 to DRAS0 in DRCRA to 0. After setting RTCOR, selection a clock source with bits CKS2 to CKS0 in RTMCSR, and set the CMIE bit to 1.

Timing of Setting of Compare Match Flag and Clearing by Compare Match: The CMF flag in RTMCSR is set to 1 by a compare match output when the RTCOR and RTCNT values match. The compare match signal is generated in the last state in which the values match (when RTCNT is updated from the matching value to a new value). Accordingly, when RTCNT and RTCOR match, the compare match signal is not generated until the next counter clock pulse. Figure 6.38 shows the timing.

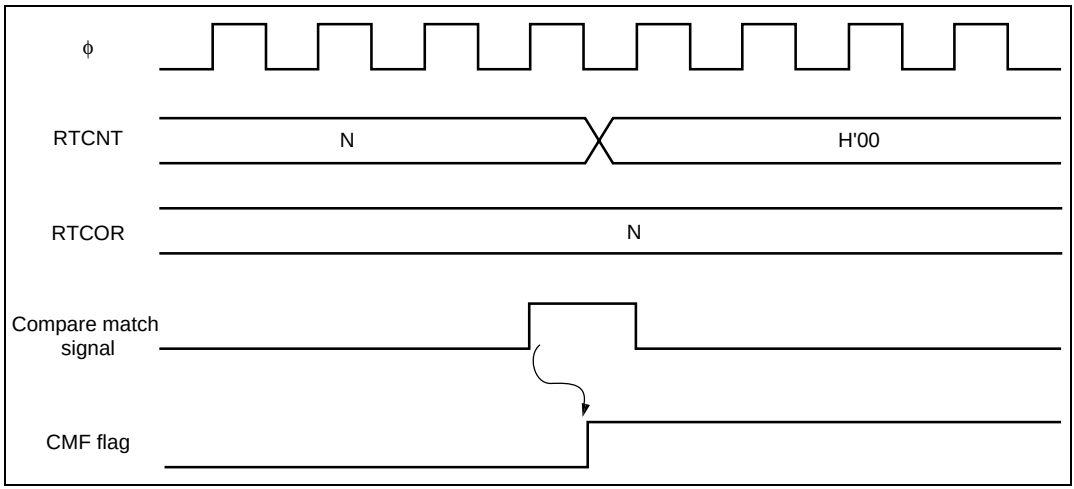


Figure 6.38 Timing of CMF Flag Setting

Contention between RTCOR Write and Compare Match: If a compare match occurs in the T_3 state of an RTCOR write cycle, writing takes priority and the compare match signal is inhibited. See Figure 6.41.

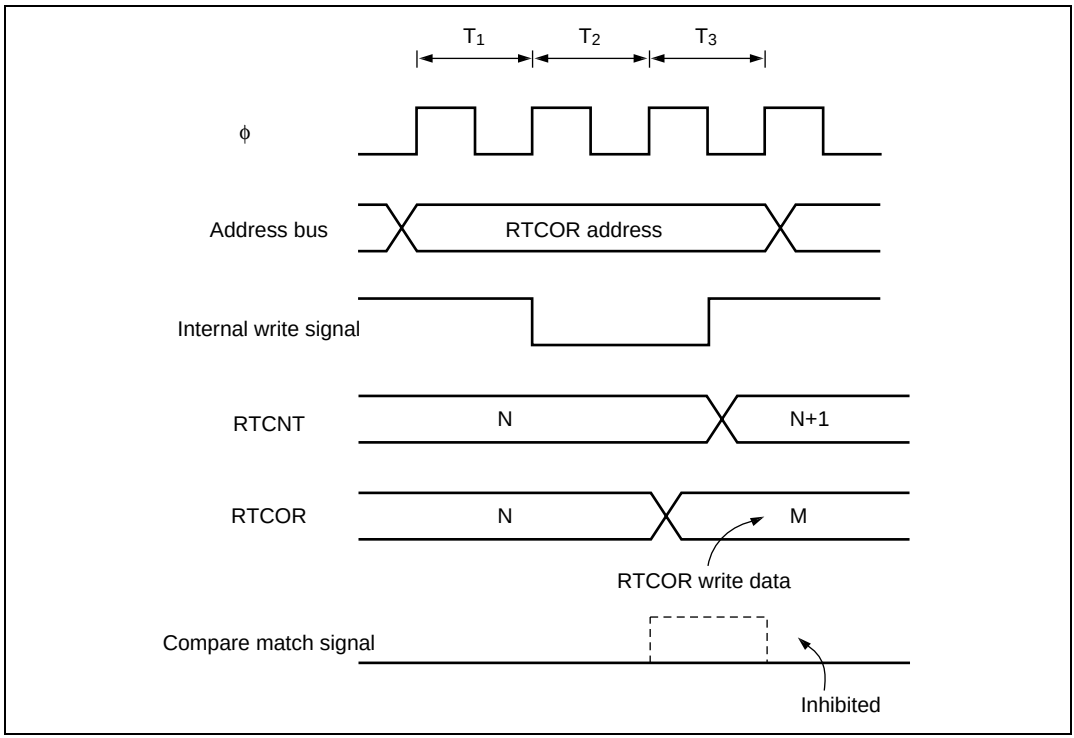


Figure 6.41 Contention between RTCOR Write and Compare Match

RTCNT Operation at Internal Clock Source Switchover: Switching internal clock sources may cause RTCNT to increment, depending on the switchover timing. Table 6.10 shows the relation between the time of the switchover (by writing to bits CKS2 to CKS0) and the operation of RTCNT.

The RTCNT input clock is generated from the internal clock source by detecting the falling edge of the internal clock. If a switchover is made from a high clock source to a low clock source, as in case No. 3 in table 6.10, the switchover will be regarded as a falling edge, an RTCNT clock pulse will be generated, and RTCNT will be incremented.

DMAC: When the DMAC receives an activation request, it requests the bus right from the bus arbiter. If the DMAC is bus master and the DRAM interface or an external bus master requests the bus, the bus arbiter transfers the bus right from the DMAC to the bus master that requested the bus. The bus right is transferred at the following times.

The bus right is transferred when the DMAC finishes transferring one byte or one word. A DMAC transfer cycle consists of a read cycle and a write cycle. The bus right is not transferred between the read cycle and the write cycle.

There is a priority order among the DMAC channels. For details see section 7.4.9, Multiple-Channel Operation.

DRAM Interface: The DRAM interface requests the bus right from the bus arbiter when a refresh cycle request is issued, and releases the bus at the end of the refresh cycle. For details see section 6.5, DRAM Interface.

External Bus Master: When the BRLE bit is set to 1 in BRCR, the bus can be released to an external bus master. The external bus master has highest priority, and requests the bus right from the bus arbiter y driving the $\overline{\text{BREQ}}$ signal low. Once the external bus master acquires the bus, it keeps the bus until the $\overline{\text{BREQ}}$ signal goes high. While the bus is released to an external bus master, the H8/3067 Group chip holds the address bus, data bus, bus control signals ($\overline{\text{AS}}$, $\overline{\text{RD}}$, $\overline{\text{HWR}}$, and $\overline{\text{LWR}}$), and chip select signals ($\overline{\text{CS}}$n: n = 7 to 0) in the high-impedance state, and holds the $\overline{\text{BACK}}$ pin in the low output state.

The bus arbiter samples the $\overline{\text{BREQ}}$ pin at the rise of the system clock (ϕ). If $\overline{\text{BREQ}}$ is low, the bus is released to the external bus master at the appropriate opportunity. The $\overline{\text{BREQ}}$ signal should be held low until the $\overline{\text{BACK}}$ signal goes low.

When the $\overline{\text{BREQ}}$ pin is high in two consecutive samples, the $\overline{\text{BACK}}$ pin is driven high to end the bus-release cycle.

Figure 6.48 shows the timing when the bus right is requested by an external bus master during a read cycle in a two-state access area. There is a minimum interval of three states from when the $\overline{\text{BREQ}}$ signal goes low until the bus is released.

7.1.3 Functional Overview

Table 7.1 gives an overview of the DMAC functions.

Table 7.1 DMAC Functional Overview

Transfer Mode		Activation	Address Reg. Length	
			Source	Destination
Short address mode	I/O mode • Transfers one byte or one word per request • Increments or decrements the memory address by 1 or 2 • Executes 1 to 65,536 transfers	• Compare match/input capture A interrupts from 16-bit timer channels 0 to 2 • Transmit-data-empty interrupt from SCI channel 0	24	8
	Idle mode • Transfers one byte or one word per request • Holds the memory address fixed • Executes 1 to 65,536 transfers	• Conversion-end interrupt from A/D converter • Receive-data-full interrupt from SCI channel 0	8	24
	Repeat mode • Transfers one byte or one word per request • Increments or decrements the memory address by 1 or 2 • Executes a specified number (1 to 255) of transfers, then returns to the initial state and continues	• External request	24	8
Full address mode	Normal mode • Auto-request — Retains the transfer request internally — Executes a specified number(1 to 65,536) of transfers continuously — Selection of burst mode or cycle-steal mode • External request — Transfers one byte or one word per request — Executes 1 to 65,536 transfers	• Auto-request • External request	24	24
	Block transfer • Transfers one block of a specified size per request • Executes 1 to 65,536 transfers • Allows either the source or destination to be a fixed block area • Block size can be 1 to 255 bytes or words	• Compare match/ input capture A interrupts from 16-bit timer channels 0 to 2 • External request • Conversion-end interrupt from A/D converter	24	24

If M (1 to 255) is the size of the block transferred at each request and N (1 to 65,536) is the number of blocks to be transferred, then ETCRAH and ETCRAL should initially be set to M and ETCRB should initially be set to N.

Figure 7.10 illustrates how block transfer mode operates. In this figure, bit TMS is cleared to 0, meaning the block area is the destination.

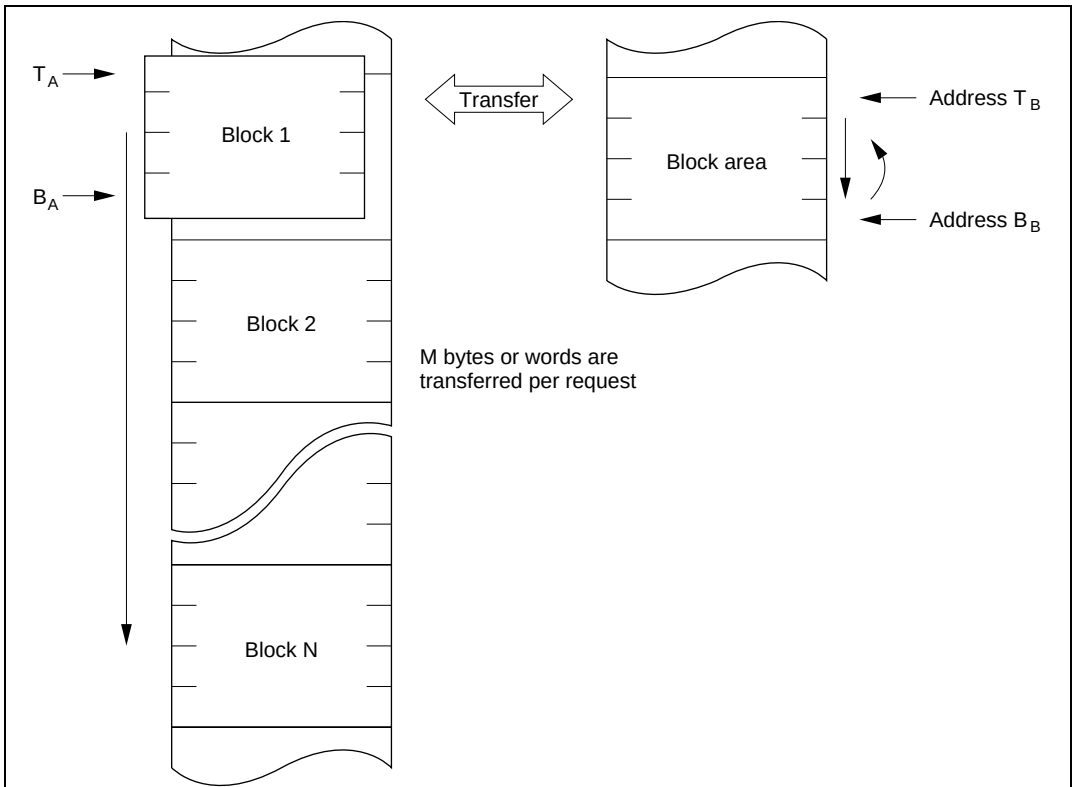


Figure 7.10 Operation in Block Transfer Mode

executed. If level sensing is selected, the transfer continues while $\overline{\text{DREQ}}$ is low, until the transfer is completed. The bus is released temporarily after each byte or word has been transferred, however. If the $\overline{\text{DREQ}}$ input goes high during a transfer, the transfer is suspended after the current byte or word has been transferred. When $\overline{\text{DREQ}}$ goes low, the request is held internally until one byte or word has been transferred. The $\overline{\text{TEND}}$ signal goes low during the last write cycle.

In block transfer mode, an external request operates as follows. Only edge-sensitive transfer requests are possible in block transfer mode. Each time a high-to-low transition of the $\overline{\text{DREQ}}$ input is detected, a block of the specified size is transferred. The $\overline{\text{TEND}}$ signal goes low during the last write cycle in each block.

Activation by Auto-Request: The transfer starts as soon as enabled by register setup, and continues until completed. Cycle-steal mode or burst mode can be selected.

In cycle-steal mode the DMAC releases the bus temporarily after transferring each byte or word. Normally, DMAC cycles alternate with CPU cycles.

In burst mode the DMAC keeps the bus until the transfer is completed, unless there is a higher-priority bus request. If there is a higher-priority bus request, the bus is released after the current byte or word has been transferred.

13.1.3 Input/Output Pins

The SCI has serial pins for each channel as listed in table 13.1.

Table 13.1 SCI Pins

Channel	Name	Abbreviation	I/O	Function
0	Serial clock pin	SCK_0	Input/output	SCI_0 clock input/output
	Receive data pin	RxD_0	Input	SCI_0 receive data input
	Transmit data pin	TxD_0	Output	SCI_0 transmit data output
1	Serial clock pin	SCK_1	Input/output	SCI_1 clock input/output
	Receive data pin	RxD_1	Input	SCI_1 receive data input
	Transmit data pin	TxD_1	Output	SCI_1 transmit data output
2	Serial clock pin	SCK_2	Input/output	SCI_2 clock input/output
	Receive data pin	RxD_2	Input	SCI_2 receive data input
	Transmit data pin	TxD_2	Output	SCI_2 transmit data output

Transmitting and Receiving Data:

- SCI Initialization (Synchronous Mode): Before transmitting or receiving data, clear the TE and RE bits to 0 in SCR, then initialize the SCI as follows.

  When changing the communication mode or format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets the TDRE flag to 1 and initializes TSR. Note that clearing RE to 0, however, does not initialize the RDRF, PER, and ORE flags, or RDR, which retain their previous contents.

Figure 13.15 shows a sample flowchart for initializing the SCI.

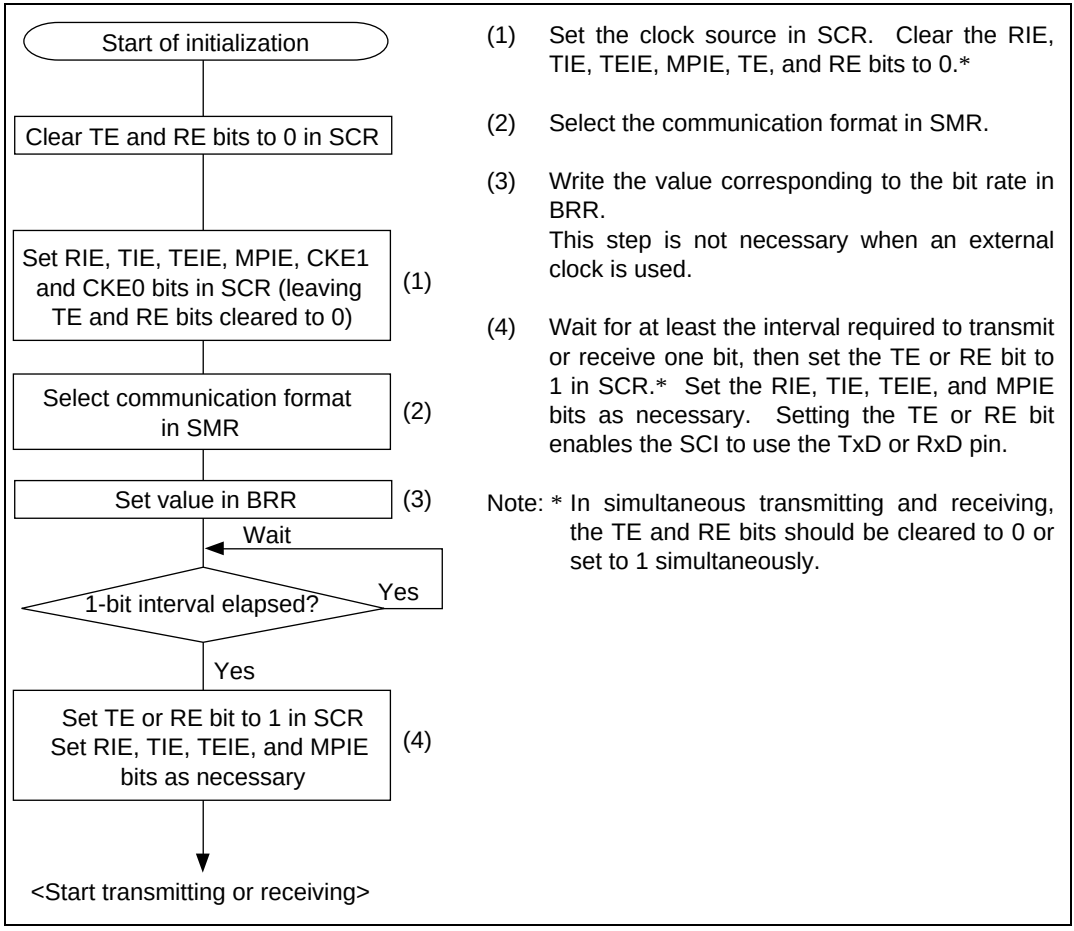


Figure 13.15 Sample Flowchart for SCI Initialization

the receiving device places the signal line in the high-impedance state again. The signal line is pulled high again by a pull-up resistor.

5. If the transmitting device does not receive an error signal, it proceeds to transmit the next data frame. If it receives an error signal, however, it returns to step 2 and transmits the same data again.

14.3.4 Register Settings

Table 14.3 shows a bit map of the registers used in the smart card interface. Bits indicated as 0 or 1 must be set to the value shown. The setting of other bits is described in this section.

Table 14.3 Smart Card Interface Register Settings

		Bit							
Register	**Address**[*1]	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SMR	H'FFFB0	GM	0	1	O/$\overline{E}$	1	0	CKS1	CKS0
BRR	H'FFFB1	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
SCR	H'FFFB2	TIE	RIE	TE	RE	0	0	CKE1[*2]	CKE0
TDR	H'FFFB3	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
SSR	H'FFFB4	TDRE	RDRF	ORER	ERS	PER	TEND	0	0
RDR	H'FFFB5	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
SCMR	H'FFFB6	—	—	—	—	SDIR	SINV	—	SMIF

Notes: — Unused bit.
1. Lower 20 bits of the address in advanced mode.
2. When GM is cleared to 0 in SMR, the CKE1 bit must also be cleared to 0.

Serial Mode Register (SMR) Settings: Clear the GM bit to 0 when using the normal smart card interface mode, or set to 1 when using GSM mode. Clear the O/$\overline{E}$ bit to 0 if the smart card is of the direct convention type, or set to 1 if of the inverse convention type.

Bits CKS1 and CKS0 select the clock source of the built-in baud rate generator. See section 14.3.5, Clock.

Bit Rate Register (BRR) Settings: BRR is used to set the bit rate. See section 14.3.5, Clock, for the method of calculating the value to be set.

Serial Control Register (SCR) Settings: The TIE, RIE, TE, and RE bits have their normal serial communication functions. See section 13, Serial Communication Interface, for details. The CKE1 and CKE0 bits specify clock output. To disable clock output, clear these bits to 00; to enable clock

If a filter circuit is used, be careful of interference with digital signals on the same board, and make sure the circuit does not act as an antenna.

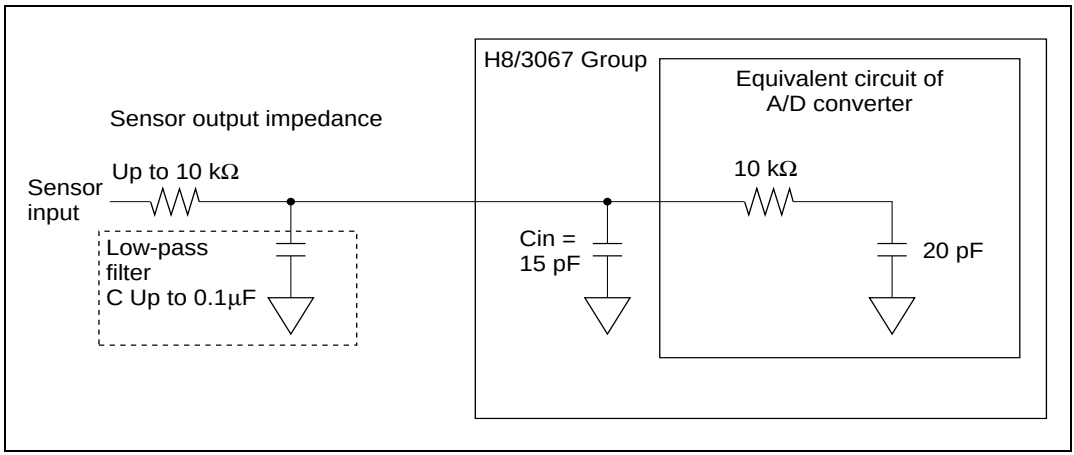


Figure 15.11 Analog Input Circuit (Example)

Notes on use of the RAM emulation function

(1) Notes on flash write enable (FWE) high/low

Care is necessary to prevent erroneous programming/erasing at FWE=high/low, the same as in the on-board programming mode. To prevent erroneous programming and erasing due to program runaway, etc., during FWE application, in particular, the watchdog timer should be set when the PSU, P, ESU, or E bit is set to 1 in FLMCR, even while the emulation function is being used. For more information, see section 18.9, Notes on Flash Memory Programming/Erasing.

(2) NMI input disable conditions

When the P and E bits in FLMCR are set, NMI input is disabled, the same as normal program/erase even when using the emulation function.

NMI input is cleared when the P and E bits are reset (including watchdog timer reset), in the standby mode, when a high level is not applied to FWE, and when the SWE bit in FLMCR is 0 in state in which a high level is input to FWE.

20.4.6 Cautions on Clearing the Software Standby Mode of F-ZTAT Version

(1) Operation phenomena

When using operating mode 5, 6, or 7* (on-chip flash memory enabled), the first read of on-chip flash memory after exiting software standby mode may not be carried out correctly.

Software standby mode is exited by means of an external interrupt (via the NMI, $\overline{IRQ_0}$, $\overline{IRQ_1}$, or $\overline{IRQ_2}$ pin), the $\overline{RES}$ pin, or the $\overline{STBY}$ pin. In the case of an external interrupt via the NMI, $\overline{IRQ_0}$, $\overline{IRQ_1}$, or $\overline{IRQ_2}$ pin, the first read after exiting software standby mode is a read of the vector corresponding to the respective exception handling interrupt source. This vector may not be read correctly, resulting in program runaway.

Note: * Mode 5: expanded 16-Mbyte mode with on-chip ROM enabled
Mode 6: single-chip normal mode
Mode 7: single-chip advanced mode

(2) Exemplary procedures to avoid program runaway

This operation phenomenon can be avoided by writing or amending program code in accordance with the following procedures.

(a) When using mode 5 or mode 7, assign addresses in the 64-kbyte space from H'00000 to H'0FFFF as the vector addresses for the external interrupts that clear software standby mode.

(b) When using mode 6, change the mode to mode 7 in the program, and use change (a) above.

Note that it is necessary to change vector address assignments and to extend addresses as follows.

- Addresses H'DFFF and below (on-chip ROM area): H'xxxx → H'0xxxx
- Addresses H'E000 to H'E0FF (internal I/O registers-1): H'yyyy → H'Eyyyy
- Addresses H'EF20 and above (on-chip RAM area and internal I/O registers-2): H'zzzz → H'Fzzzz
  (Where x, y and z are any hexadecimal numbers)

With the production lots prior to the week code “9K1” of the HD64F3067 and HD64F3067R, avoid program runaway according to the procedures designated above.

Meanwhile, as for the production lots of the week code “9K1” and after, the special constraint according to of the aforementioned Section (2) is not applicable.

BRCR—Bus Release Control Register | H'EE013 | Bus controller

Bit	7	6	5	4	3	2	1	0
	A23E	A22E	A21E	A20E	—	—	—	BRLE
Modes 1, 2, 6, 7 Initial value	1	1	1	1	1	1	1	0
Modes 1, 2, 6, 7 Read/Write	—	—	—	—	—	—	—	R/W
Modes 3, 4 Initial value	1	1	1	0	1	1	1	0
Modes 3, 4 Read/Write	R/W	R/W	R/W	—	—	—	—	R/W
Mode 5 Initial value	1	1	1	1	1	1	1	0
Mode 5 Read/Write	R/W	R/W	R/W	R/W	—	—	—	R/W

Address 23 to 20 enable

0	Address output
1	Other input/output

Bus release enable

0	The bus cannot be released to an external device
1	The bus can be released to an external device

ISCR—IRQ Sense Control Register | H'EE014 | Interrupt Controller

Bit	7	6	5	4	3	2	1	0
	—	—	IRQ5SC	IRQ4SC	IRQ3SC	IRQ2SC	IRQ1SC	IRQ0SC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ_5 to IRQ_0 sense control

0	Interrupts are requested when $\overline{IRQ}_5$ to $\overline{IRQ}_0$ are low
1	Interrupts are requested by falling-edge input at $\overline{IRQ}_5$ to $\overline{IRQ}_0$

FLMSR-Flash Memory Status Register	H'EE07D	Flash Memory

Bit	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
R/W	R	—	—	—	—	—	—	—

Reserved bits

RAM select, RAM2, RAM1

Bit 7 FLER	Description
0	Flash memory program/erase protection (error protection) is disabled (Initial value) [Clearing condition] WDT reset, reset via the $\overline{\text{RES}}$ pin or hardware standby mode
1	An error has occurred during flash memory programming/erasing, and error protection*1 is enabled [Setting conditions] 1. Flash memory was read*2 while being programmed or erased (including vector or instruction fetch, but not including reading of a RAM area overlapped onto flash memory). 2. A hardware exception-handling sequence (other than a reset, invalid instruction, trap instruction, or zero-divide exception) was executed just before programming or erasing.*3 3. The SLEEP instruction (including software standby mode) was executed during programming or erasing.

Notes 1. See 18.6.3, Error Protection, for details.
2. The read value in this case is undefined.
3. Before stack and vector read by exception handling.

Note: This register is used only in the flash memory and flash memory R versions. Reading the corresponding address in a mask ROM version will always return 1s, and writes to this address are disabled.

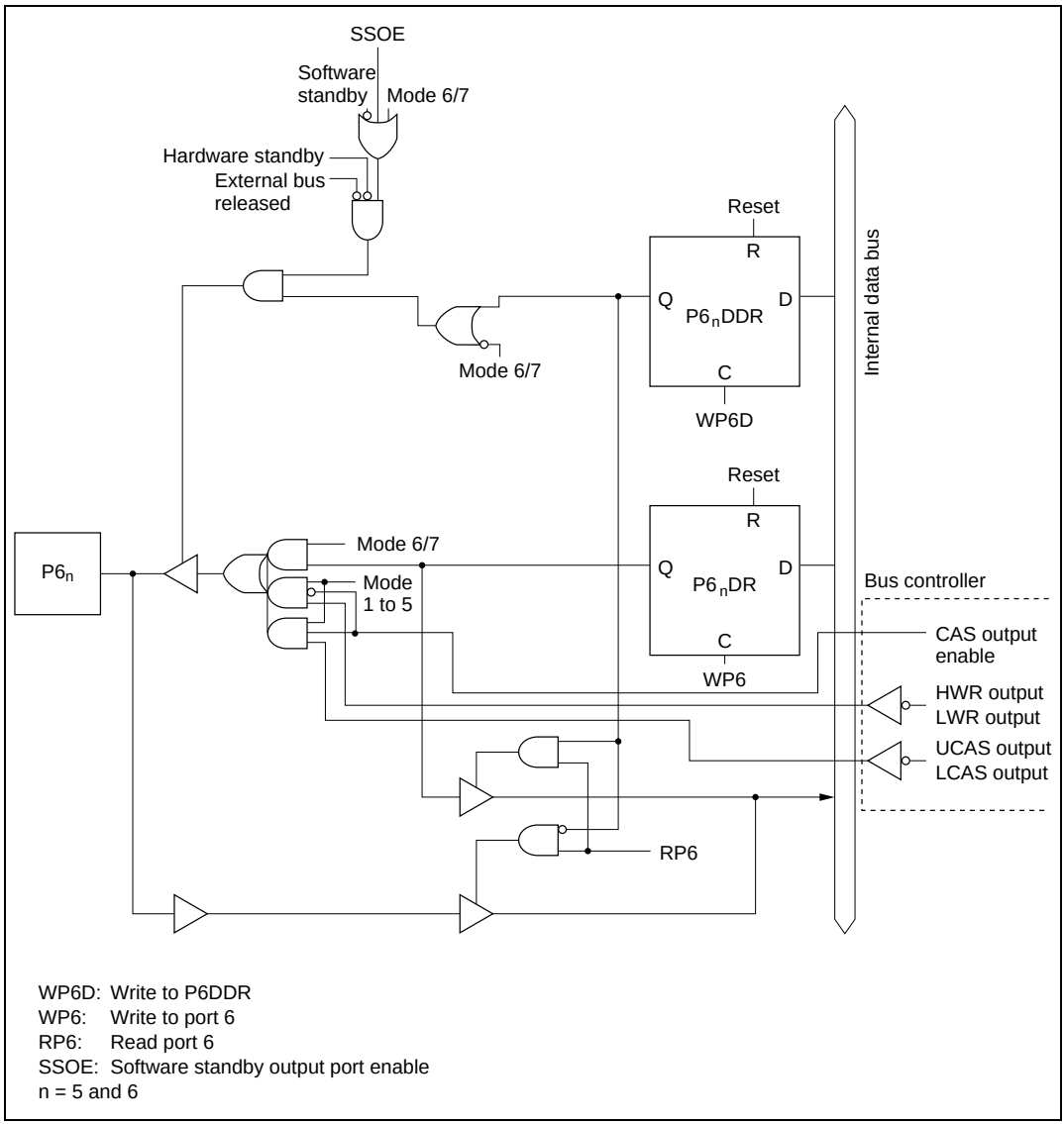
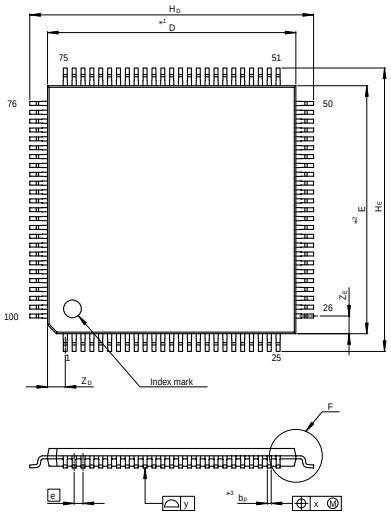
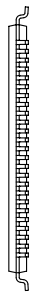
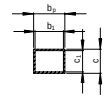


Figure C.6 (f) Port 6 Block Diagram (Pins $P6_5$ and $P6_6$)

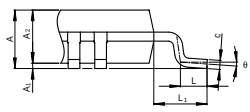
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TQFP100-14x14-0.50	PTQP0100KA-A	TFP-100B/TFP-100BV	0.5g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2"
DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	1.00	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.20
A_1	0.00	0.10	0.20
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.00	—
Z_E	—	1.00	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure G.2 Package Dimensions (PTQP0100KA-A)