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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	13MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-QFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3067rvx13v

Contents

16 bits. A_{23} to A_{21} are valid when 0 is written in bits 7 to 5 of the bus release control register (BRCR). (In this mode A_{20} is always used for address output.)

3.4.4 Mode 4

Ports 1, 2, and 5 and part of port A function as address pins A_{23} to A_0, permitting access to a maximum 16-Mbyte address space. The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. If all areas are designated for 8-bit access in ABWCR, the bus mode switches to 8 bits. A_{23} to A_{21} are valid when 0 is written in bits 7 to 5 of BRCR. (In this mode A_{20} is always used for address output.)

3.4.5 Mode 5

Ports 1, 2, and 5 and part of port A can function as address pins A_{23} to A_0, permitting access to a maximum 16-Mbyte address space, but following a reset they are input ports. To use ports 1, 2, and 5 as an address bus, the corresponding bits in their data direction registers (P1DDR, P2DDR, and P5DDR) must be set to 1. For A_{23} to A_{20} output, write 0 in bits 7 to 4 of BRCR. The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. If at least one area is designated for 16-bit access in ABWCR, the bus mode switches to 16 bits.

3.4.6 Mode 6

This mode operates using the on-chip ROM, RAM, and registers. All I/O ports are available. Mode 6 supports a maximum address space of 64 kbytes.

3.4.7 Mode 7

This mode operates using the on-chip ROM, RAM, and registers. All I/O ports are available. Mode 7 supports a 1-Mbyte address space.

5.1.3 Pin Configuration

Table 5.1 lists the interrupt pins.

Table 5.1 Interrupt Pins

Name	Abbreviation	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable interrupt*, rising edge or falling edge selectable
External interrupt request 5 to 0	$\overline{IRQ}_5$ to $\overline{IRQ}_0$	Input	Maskable interrupts, falling edge or level sensing selectable

Note: * In the flash memory and flash memory R versions, NMI input is sometimes disabled. For details see 18.6.4, NMI Input Disable Conditions.

5.1.4 Register Configuration

Table 5.2 lists the registers of the interrupt controller.

Table 5.2 Interrupt Controller Registers

Address*1	Name	Abbreviation	R/W	Initial Value
H'EE012	System control register	SYSCR	R/W	H'09
H'EE014	IRQ sense control register	ISCR	R/W	H'00
H'EE015	IRQ enable register	IER	R/W	H'00
H'EE016	IRQ status register	ISR	R/(W)*2	H'00
H'EE018	Interrupt priority register A	IPRA	R/W	H'00
H'EE019	Interrupt priority register B	IPRB	R/W	H'00

Notes: 1. Lower 20 bits of the address in advanced mode.
2. Only 0 can be written, to clear flags.

If a DRAM read/write cycle is followed by an access cycle for an external area other than DRAM space when $\overline{HWR}$ and $\overline{LWR}$ are selected as the $\overline{UCAS}$ and $\overline{LCAS}$ output pins, an idle cycle (Ti) is inserted unconditionally immediately after the DRAM access cycle. See section 6.9, Idle Cycle, for details.

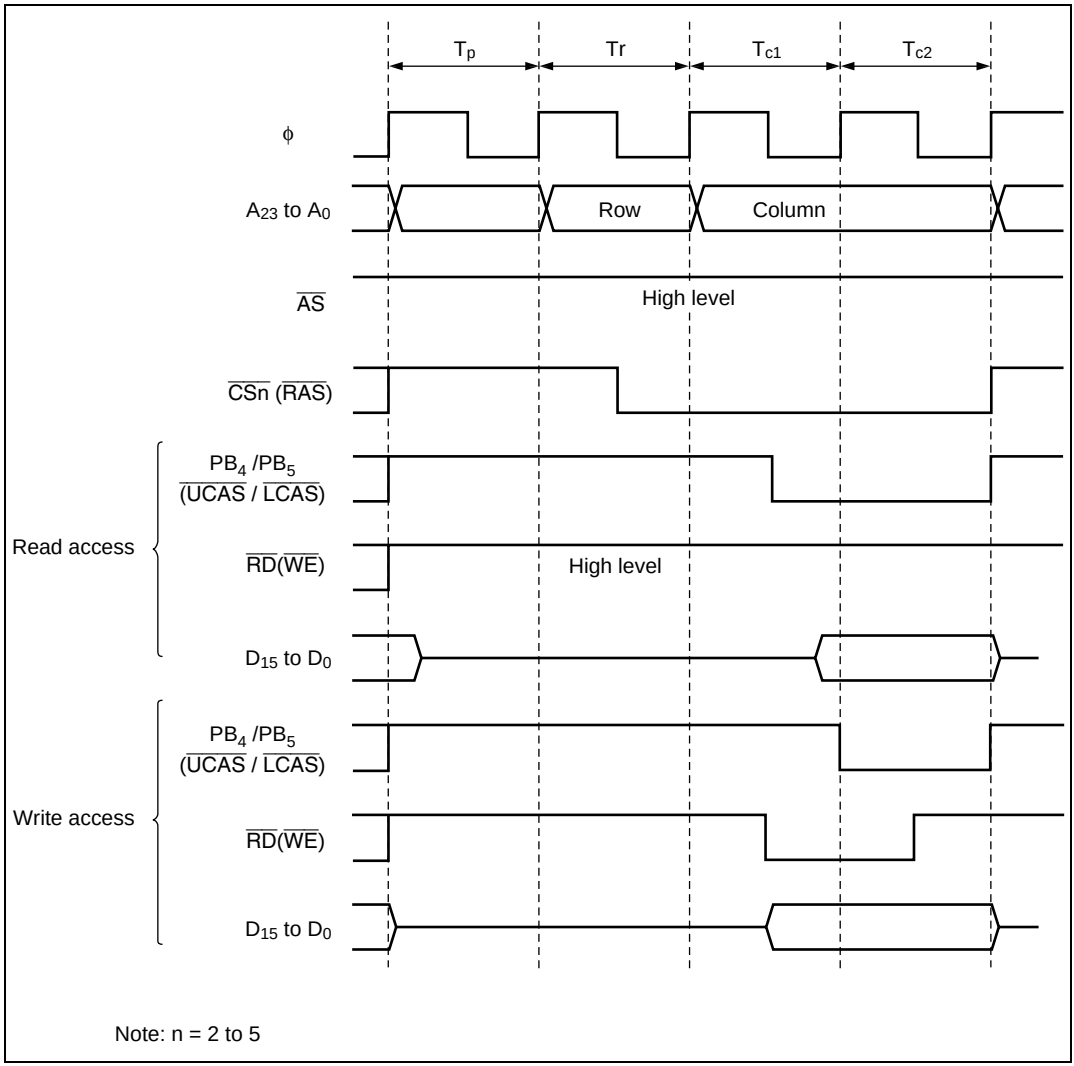


Figure 6.18 Basic Access Timing (CSEL = 0 in DRCRB)

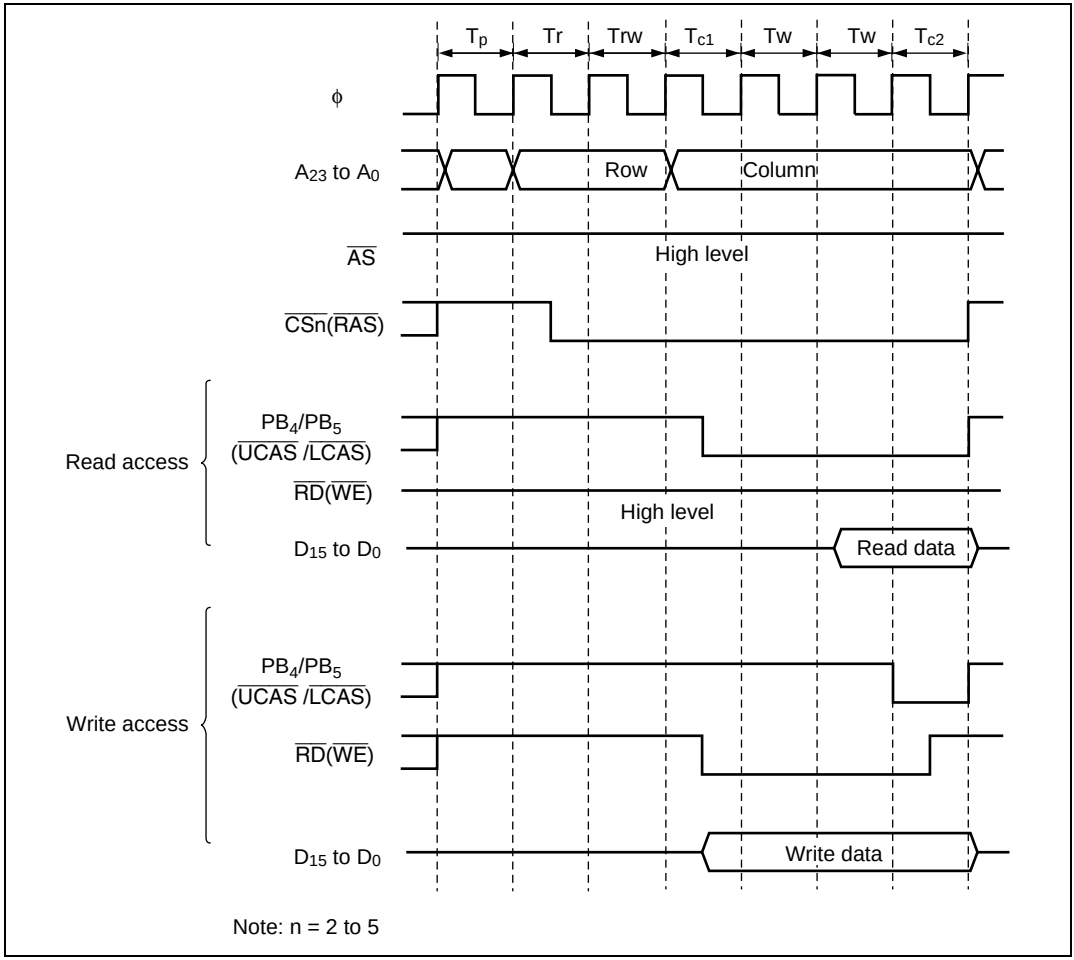


Figure 6.20 Example of Wait State Insertion Timing (CSEL = 0)

6.5.9 Byte Access Control and $\overline{\text{CAS}}$ Output Pin

When an access is made to DRAM space designated as a 16-bit-access area in ABWCR, column address strobes ($\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$) corresponding to the upper and lower halves of the external data bus are output. In the case of × 16-bit organization DRAM, the 2-CAS type can be connected.

Either PB4 and PB5, or $\overline{\text{HWR}}$ and $\overline{\text{LWR}}$, can be used as the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ output pins, the selection being made with the CSEL bit in DRCRB. Table 6.8 shows the CSEL bit settings and corresponding output pin selections.

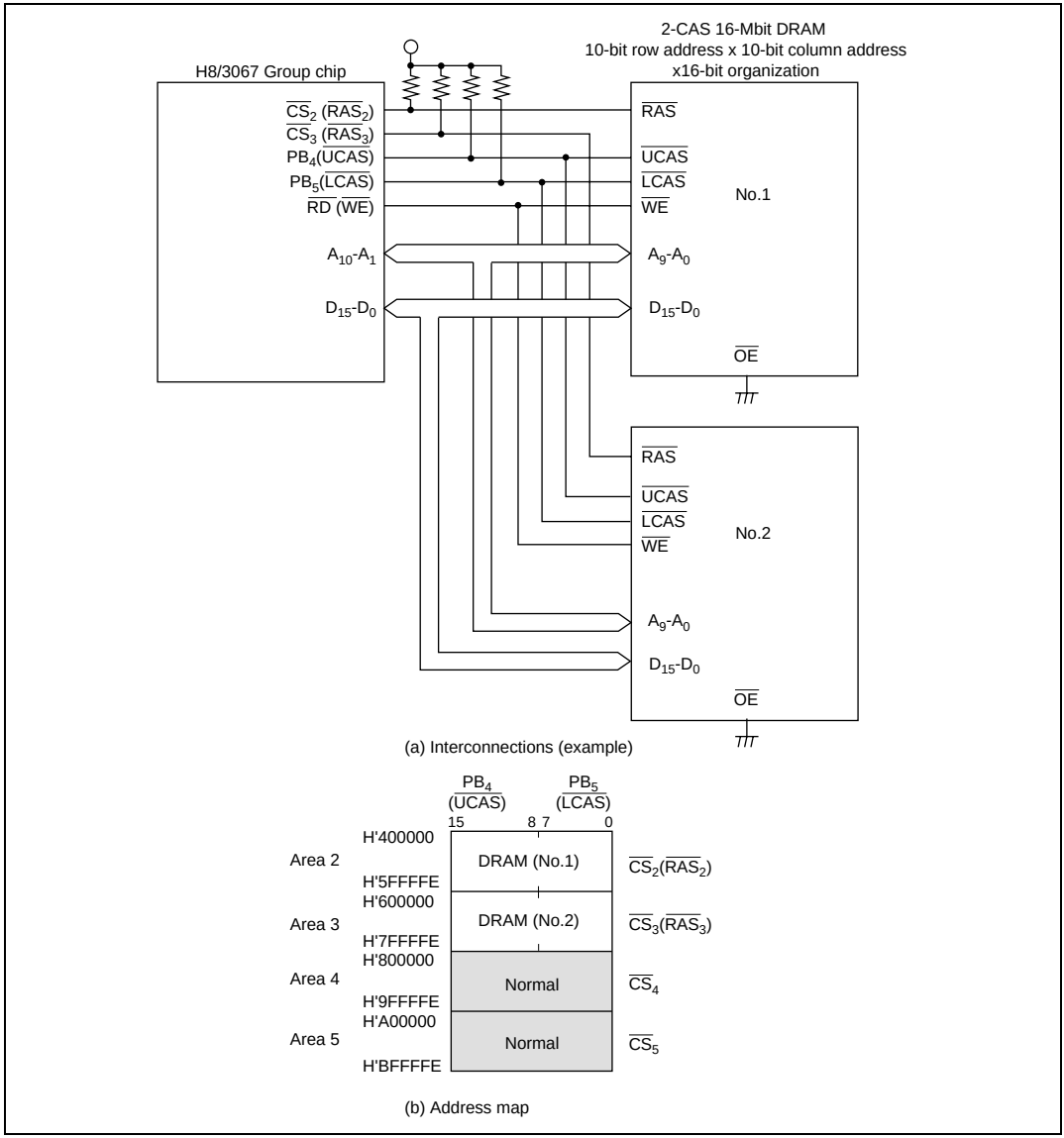


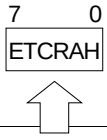
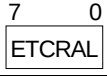
Figure 6.31 Interconnections and Address Map for 2-CAS 16-Mbit DRAMs with × 16-Bit Organization

7.4.6 Block Transfer Mode

In block transfer mode the A and B channels are combined. One block of a specified size is transferred per request. A designated number of block transfers are executed. Addresses are specified in MARA and MARB. The block area address can be either held fixed or cycled.

Table 7.10 indicates the register functions in block transfer mode.

Table 7.10 Register Functions in Block Transfer Mode

Register	Function	Initial Setting	Operation
	Source address register	Source start address	Incremented or decremented once per transfer, or held fixed
	Destination address register	Destination start address	Incremented or decremented once per transfer, or held fixed
	Block size counter	Block size	Decremented once per transfer until H'00 is reached, then reloaded from ETCRL
	Initial block size	Block size	Held fixed
	Block transfer counter	Number of block transfers	Decremented once per block transfer until H'0000 is reached and the transfer ends

Legend
MARA: Memory address register A
MARB: Memory address register B
ETCRA: Execute transfer count register A
ETCRB: Execute transfer count register B

The source and destination addresses are both 24-bit addresses. MARA specifies the source address. MARB specifies the destination address. MARA and MARB can be independently incremented, decremented, or held fixed as data is transferred. One of these registers operates as a block area register: even if it is incremented or decremented, it is restored to its initial value at the end of each block transfer. The TMS bit in DTCRB selects whether the block area is the source or destination.

Table 7.14 Address Ranges Specifiable in MAR and IOAR

	1-Mbyte Mode	16-Mbyte Mode
MAR	H'00000 to H'FFFFF (0 to 1048575)	H'000000 to H'FFFFFF (0 to 16777215)
IOAR	H'FFF00 to H'FFFFF (1048320 to 1048575)	H'FFFF00 to H'FFFFFF (16776960 to 16777215)

MAR bits 23 to 20 are ignored in 1-Mbyte mode.

7.6.8 Bus Cycle when Transfer is Aborted

When a transfer is aborted by clearing the DTE bit or suspended by an NMI that clears the DTME bit, if this halts a channel for which the DMAC has a transfer request pending internally, a dead cycle may occur. This dead cycle does not update the halted channel's address register or counter value. Figure 7.27 shows an example in which an auto-requested transfer in cycle-steal mode on channel 0 is aborted by clearing the DTE bit in channel 0.

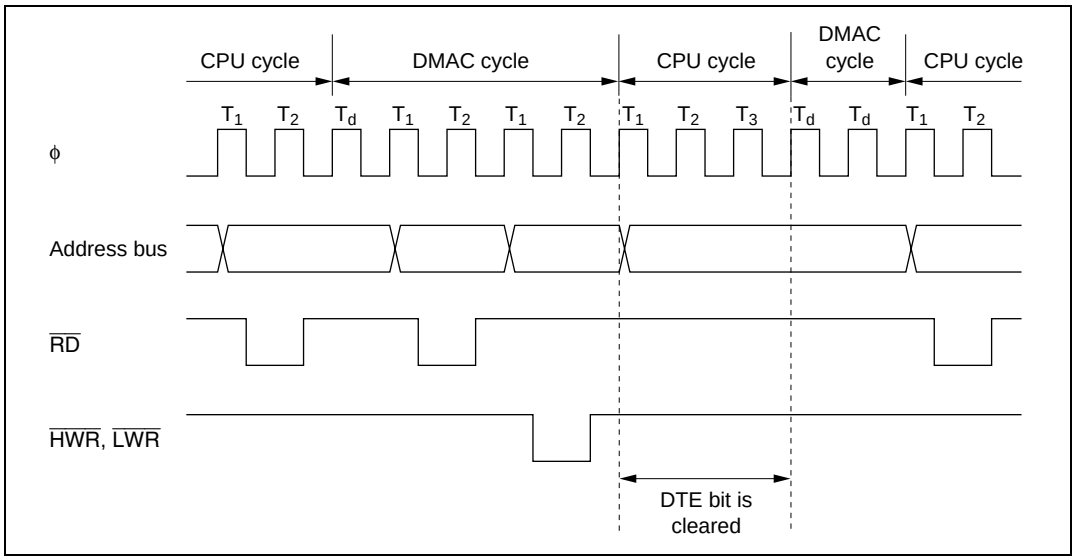


Figure 7.27 Bus Timing at Abort of DMA Transfer in Cycle-Steal Mode

ABWCR and P4DDR are not initialized in software standby mode. Therefore, if a transition is made to software standby mode while port 4 is functioning as an input/output port and a P4DDR bit is set to 1, the corresponding pin maintains its output state.

Port 4 Data Register (P4DR): P4DR is an 8-bit readable/writable register that stores output data for port 4. When port 4 functions as an output port, the value of this register is output. When a bit in P4DDR is set to 1, if port 4 is read the value of the corresponding P4DR bit is returned. When a bit in P4DDR is cleared to 0, if port 4 is read the corresponding pin logic level is read.

Bit	7	6	5	4	3	2	1	0
	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 4 data 7 to 0
These bits store data for port 4 pins

P4DR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

Port 4 Input Pull-Up MOS Control Register (P4PCR): P4PCR is an 8-bit readable/writable register that controls the MOS input pull-up transistors in port 4.

Bit	7	6	5	4	3	2	1	0
	$P4_7$PCR	$P4_6$PCR	$P4_5$PCR	$P4_4$PCR	$P4_3$PCR	$P4_2$PCR	$P4_1$PCR	$P4_0$PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 4 input pull-up control 7 to 0
These bits control input pull-up transistors built into port 4

In mode 6 and 7 (single-chip mode), and in 8-bit bus mode in modes 1 to 5 (expanded modes), when a P4DDR bit is cleared to 0 (selecting generic input), if the corresponding P4PCR bit is set to 1, the input pull-up transistor is turned on.

P4PCR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

9.4.6 Setting Initial Value of 16-Bit Timer Output

Any desired value can be specified for the initial 16-bit timer output value when a timer count operation is started by making a setting in TOLR.

Figure 9.32 shows the timing for setting the initial output value with TOLR.

Only write to TOLR when the corresponding bit in TSTR is cleared to 0.

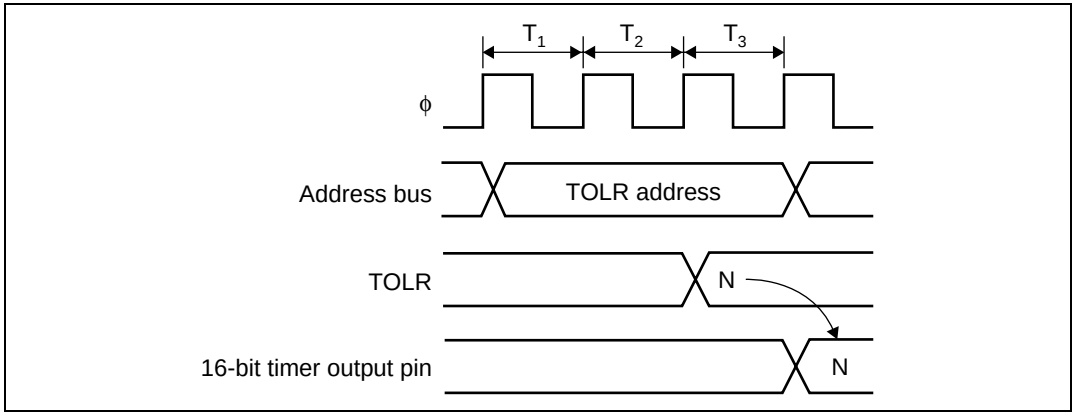


Figure 9.32 Example of Timing for Setting Initial Value of 16-Bit Timer Output by Writing to TOLR

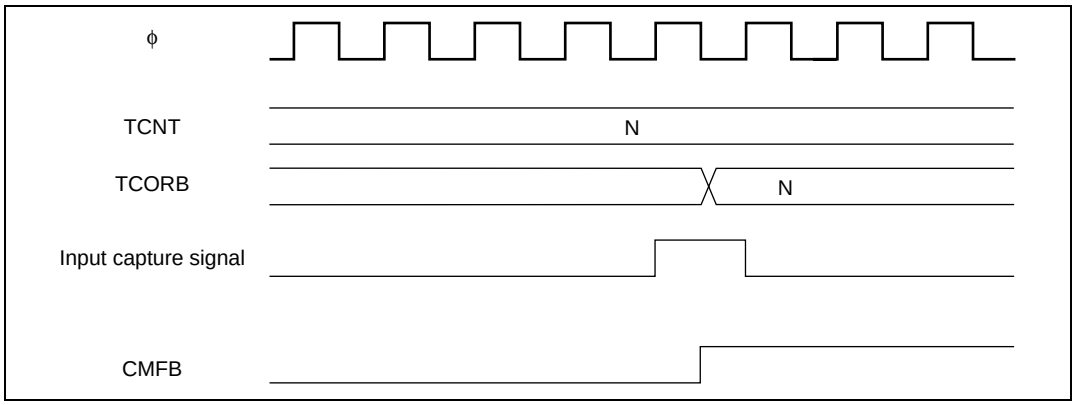


Figure 10.15 CMFB Flag Setting Timing when Input Capture Occurs

Timing of Overflow Flag (OVF) Setting: The OVF flag in TCSR is set to 1 by the overflow signal generated when TCNT overflows (from H'FF to H'00). Figure 10.16 shows the timing in this case.

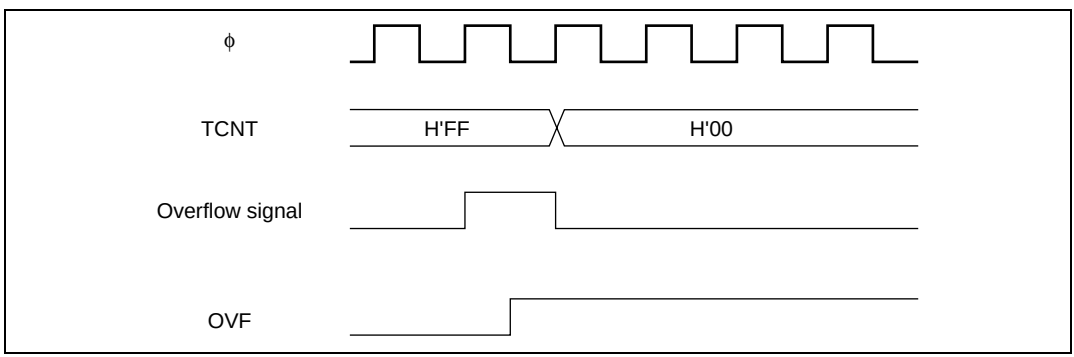


Figure 10.16 Timing of OVF Setting

10.4.5 Operation with Cascaded Connection

If bits CKS2 to CKS0 are set to B'100 in either TCR0 or TCR1, the 8-bit timers of channels 0 and 1 are cascaded. With this configuration, the two timers can be used as a single 16-bit timer (16-bit count mode), or channel 0 8-bit timer compare matches can be counted in channel 1 (compare match count mode). In this case, the timer operates as below. Similarly, if bits CKS2 to CKS0 are set to B'100 in either TCR2 or TCR3, the 8-bit timers of channels 0 and 1 are cascaded. With this configuration, the two timers can be used as a single 16-bit timer (16-bit count mode),or channel 2 8-bit timer compare matches can be counted in channel 3 (compare match count mode). Timer operation in these cases is described below.

11.2.8 Next Data Enable Register B (NDERB)

NDERB is an 8-bit readable/writable register that enables or disables TPC output groups 3 and 2 (TP_{15} to TP_8) on a bit-by-bit basis.

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Next data enable 15 to 8
These bits enable or disable TPC output groups 3 and 2

If a bit is enabled for TPC output by NDERB, then when the 16-bit timer compare match event selected in the TPC output control register (TPCR) occurs, the NDRB value is automatically transferred to the corresponding PBDR bit, updating the output value. If TPC output is disabled, the bit value is not transferred from NDRB to PBDR and the output value does not change.

NDERB is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 0—Next Data Enable 15 to 8 (NDER15 to NDER8): These bits enable or disable TPC output groups 3 and 2 (TP_{15} to TP_8) on a bit-by-bit basis.

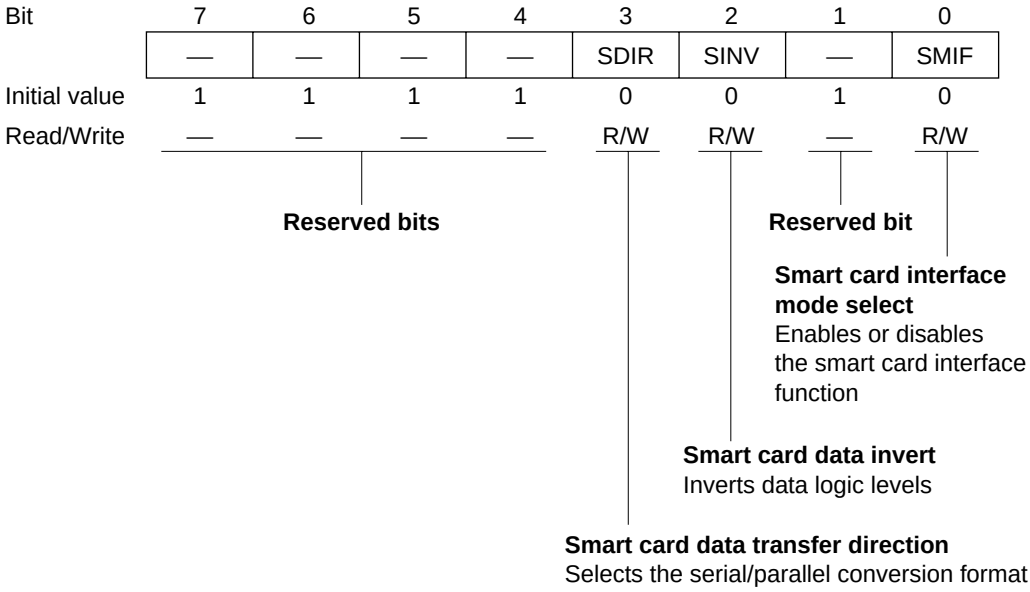
Bits 7 to 0 NDER15 to NDER8	Description	
0	TPC outputs TP_{15} to TP_8 are disabled (NDR15 to NDR8 are not transferred to PB_7 to PB_0)	(Initial value)
1	TPC outputs TP_{15} to TP_8 are enabled (NDR15 to NDR8 are transferred to PB_7 to PB_0)	

14.2 Register Descriptions

This section describes the new or modified registers and bit functions in the smart card interface.

14.2.1 Smart Card Mode Register (SCMR)

SCMR is an 8-bit readable/writable register that selects smart card interface functions.



SCMR is initialized to H'F2 by a reset and in standby mode.

Bits 7 to 4—Reserved: Read-only bits, always read as 1.

Bit 3—Smart Card Data Transfer Direction (SDIR): Selects the serial/parallel conversion format.*[1]

Bit 3 SDIR	Description	
0	TDR contents are transmitted LSB-first	(Initial value)
	Receive data is stored LSB-first in RDR	
1	TDR contents are transmitted MSB-first	
	Receive data is stored MSB-first in RDR	

The following equation calculates the bit rate register (BRR) setting from the operating frequency and bit rate. N is an integer from 0 to 255, specifying the value with the smaller error.

$$N = \frac{\phi}{1488 \times 2^{2n-1} \times B} \times 10^6 - 1$$

Table 14.6 BRR Settings for Typical Bit Rates (bits/s) (When n = 0)

	ϕ (MHz)													
	7.1424		**10.00**		**10.7136**		**13.00**		**14.2848**		**16.00**		**18.00**	
bit/s	**N**	**Error**	**N**	**Error**	**N**	**Error**	**N**	**Error**	**N**	**Error**	**N**	**Error**	**N**	**Error**
9600	0	0.00	1	30	1	25	1	8.99	1	0.00	1	12.01	2	15.99

Table 14.7 Maximum Bit Rates for Various Frequencies (Smart Card Interface Mode)

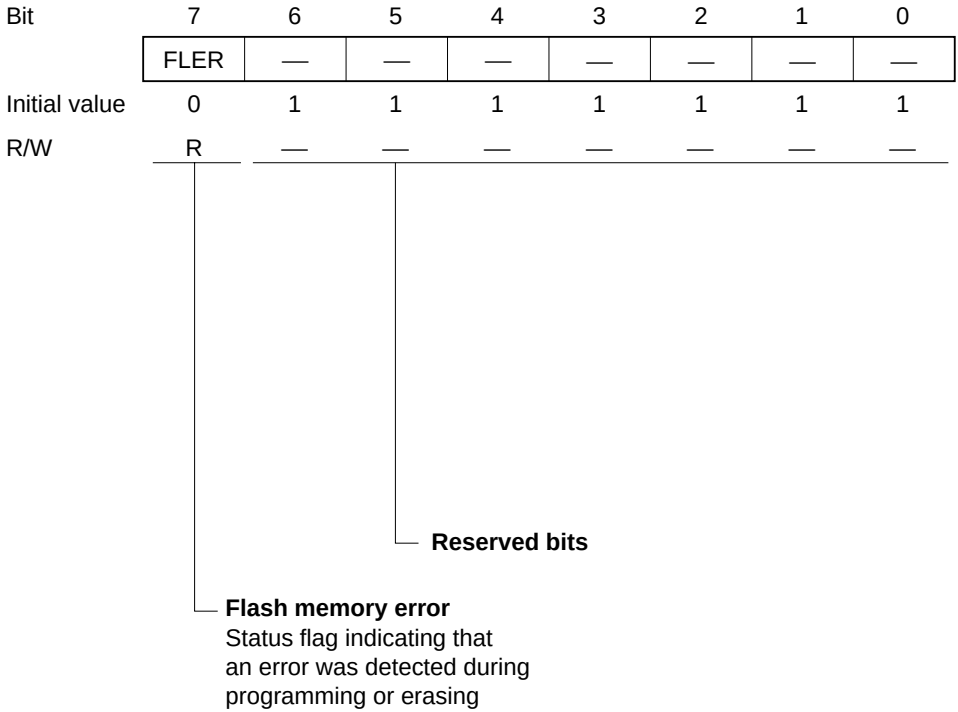
ϕ (MHz)	**Maximum Bit Rate (bits/s)**	**N**	**n**
7.1424	9600	0	0
10.00	13441	0	0
10.7136	14400	0	0
13.00	17473	0	0
14.2848	19200	0	0
16.00	21505	0	0
18.00	24194	0	0

The bit rate error is given by the following equation:

$$\text{Error (\%)} = \left(\frac{\phi}{1488 \times 2^{2n-1} \times B \times (N + 1)} \times 10^6 - 1 \right) \times 100$$

18.3.4 Flash Memory Status Register

The flash memory status register (FLMSR) detects flash memory errors.



Item	Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
Read data access time 1	t_{ACC1}	—	2.0 t_{cyc} – 80	—	2.0 t_{cyc} – 45	ns	Figure 21.11, figure 21.12, figure 21.14, figure 21.15, figure 21.17
Read data access time 2	t_{ACC2}	—	3.0 t_{cyc} – 80	—	3.0 t_{cyc} – 45	ns	
Read data access time 3	t_{ACC3}	—	1.5 t_{cyc} – 80	—	1.5 t_{cyc} – 45	ns	
Read data access time 4	t_{ACC4}	—	2.5 t_{cyc} – 80	—	2.5 t_{cyc} – 45	ns	
Precharge time 1	t_{PCH1}	1.0 t_{cyc} – 30	—	1.0 t_{cyc} – 20	—	ns	
Precharge time 2	t_{PCH2}	0.5 t_{cyc} – 30	—	0.5 t_{cyc} – 20	—	ns	
Wait setup time	t_{WTS}	40	—	25	—	ns	Figure 21.13
Wait hold time	t_{WTH}	5	—	5	—	ns	
Bus request setup time	t_{BRQS}	40	—	25	—	ns	Figure 21.16
Bus acknowledge delay time 1	t_{BACD1}	—	50	—	30	ns	
Bus acknowledge delay time 2	t_{BACD2}	—	50	—	30	ns	
Bus-floating time	t_{BZD}	—	50	—	30	ns	
$\overline{RAS}$ precharge time	t_{RP}	1.5 t_{cyc} – 40	—	1.5 t_{cyc} – 25	—	ns	Figure 21.17 to figure 21.19
$\overline{CAS}$ precharge time	t_{CP}	0.5 t_{cyc} – 25	—	0.5 t_{cyc} – 15	—	ns	
Low address hold time	t_{RAH}	0.5 t_{cyc} – 25	—	0.5 t_{cyc} – 15	—	ns	
$\overline{RAS}$ delay time 1	t_{RAD1}	—	50	—	25	ns	
$\overline{RAS}$ delay time 2	t_{RAD2}	—	50	—	30	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	50	—	25	ns	
$\overline{CAS}$ delay time 2	t_{CASD2}	—	50	—	25	ns	
$\overline{WE}$ delay time	t_{WCD}	—	50	—	25	ns	
$\overline{CAS}$ pulse width 1	t_{CAS1}	1.5 t_{cyc} – 40	—	1.5 t_{cyc} – 20	—	ns	
$\overline{CAS}$ pulse width 2	t_{CAS2}	1.0 t_{cyc} – 40	—	1.0 t_{cyc} – 20	—	ns	
$\overline{CAS}$ pulse width 3	t_{CAS3}	1.0 t_{cyc} – 40	—	1.0 t_{cyc} – 20	—	ns	

DTCR0A—Data Transfer Control Register 0A	H'FFF27	DMAC0

- Short address mode

Bit	7	6	5	4	3	2	1	0
	DTE	DTSZ	DTID	RPE	DTIE	DTS2	DTS1	DTS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data transfer select

Bit 2	Bit 1	Bit 0	Data Transfer Activation Source
DTS2	DTS1	DTS0	
0	0	0	Compare match/input capture A interrupt from 16-bit timer channel 0
		1	Compare match/input capture A interrupt from 16-bit timer channel 1
	1	0	Compare match/input capture A interrupt from 16-bit timer channel 2
		1	A/D converter conversion end interrupt
1	0	0	SCI0 transmit-data-empty interrupt
		1	SCI0 receive-data-full interrupt
	1	0	Transfer in full address mode
		1	Transfer in full address mode

Data transfer interrupt enable

0	Interrupt requested by DTE bit is disabled
1	Interrupt requested by DTE bit is enabled

Repeat enable

RPE	DTIE	Description
0	0	I/O mode
	1	
1	0	Repeat mode
	1	Idle mode

Data transfer increment/decrement

0	Incremented: If DTSZ = 0, MAR is incremented by 1 after each transfer If DTSZ = 1, MAR is incremented by 2 after each transfer
1	Decremented: If DTSZ = 0, MAR is decremented by 1 after each transfer If DTSZ = 1, MAR is decremented by 2 after each transfer

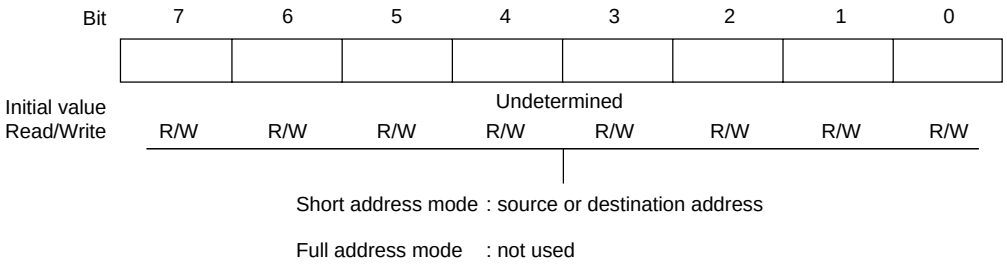
Data transfer size

0	Byte-size transfer
1	Word-size transfer

Data transfer enable

0	Data transfer is disabled
1	Data transfer is enabled

IOAR0B—I/O Address Register 0B	H'FFF2E	DMAC0



Short address mode : source or destination address

Full address mode : not used

TISRA—Timer Interrupt Status Register A	H'FFF64	16-bit timer (all channels)

Bit:	7	6	5	4	3	2	1	0
	—	IMIEA2	IMIEA1	IMIEA0	—	IMFA2	IMFA1	IMFA0
Initial value:	1	0	0	0	1	0	0	0
Read/Write:	—	R/W	R/W	R/W	—	R/(W)*	R/(W)*	R/(W)*

Input capture/compare match flag A0

0	[Clearing conditions] (Initial value) Read IMFA0 when IMFA0=1, then write 0 in IMFA0 DMAC activated by IMIA0 interrupt.
1	[Setting conditions] TCNT0=GRA0 when GRA0 functions as an output compare register. TCNT0 value is transferred to GRA0 by an input capture signal when GRA0 functions as an input capture register.

Input capture/compare match flag A1

0	[Clearing conditions] (Initial value) Read IMFA1 when IMFA1=1, then write 0 in IMFA1 DMAC activated by IMIA1 interrupt.
1	[Setting conditions] TCNT1=GRA1 when GRA1 functions as an output compare register. TCNT1 value is transferred to GRA1 by an input capture signal when GRA1 functions as an input capture register.

Input capture/compare match flag A2

0	[Clearing conditions] (Initial value) Read IMFA2 when IMFA2=1, then write 0 in IMFA2 DMAC activated by IMIA2 interrupt.
1	[Setting conditions] TCNT2=GRA2 when GRA2 functions as an output compare register. TCNT2 value is transferred to GRA2 by an input capture signal when GRA2 functions as an input capture register.

Input capture/compare match interrupt enable A0

0	IMIA0 interrupt requested by IMFA0 flag is disabled	(Initial value)
1	IMIA0 interrupt requested by IMFA0 is enabled	

Input capture/compare match interrupt enable A1

0	IMIA1 interrupt requested by IMFA1 flag is disabled	(Initial value)
1	IMIA1 interrupt requested by IMFA1 is enabled	

Input capture/compare match interrupt enable A2

0	IMIA2 interrupt requested by IMFA2 flag is disabled	(Initial value)
1	IMIA2 interrupt requested by IMFA2 is enabled	

Note: * Only 0 can be written, to clear the flag.

Pin Name	Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released Mode	Program Execution Mode
$P8_0$	1 to 5	T	T	When DRAM space is not selected[*1] (RFSHE=0) Keep (RFSHE=1) Illegal setting When DRAM space is selected[*2] (RFSHE=0) Keep (RFSHE=1, SRFMD=0, SSOE=0) T (RFSHE=1, SRFMD=0, SSOE=1) H (RFSHE=1, SRFMD=1) $\overline{RFSH}$	When DRAM space is selected[*1] (RFSHE=0) Keep (RFSHE=1) Illegal setting When DRAM space is selected[*2] (RFSHE=0) Keep (RFSHE=1) T	(RFSHE=0) I/O port (RFSHE=1) $\overline{RFSH}$
	6, 7	T	T	Keep	—	I/O port
$P8_1$	1 to 5	T	T	When DRAM space is selected[*3] (SSOE=0) T (SSOE=1) H When DRAM space is selected[*4] Keep Otherwise[*5 *1] (DDR=0) T (DDR=1, SSOE=0) T (DDR=1, SSOE=1) H	When DRAM space is selected[*3] T When DRAM space is selected[*4] Keep Otherwise[*1] (DDR=0) Keep (DDR=1) T	When DRAM space is selected and RAS3 is output $\overline{RAS_3}$ When DRAM space is selected and RAS3 is not output I/O port Otherwise (DDR=0) Input port (DDR=1) $\overline{CS_3}$
	6, 7	T	T	Keep	—	I/O port