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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f1713-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic16f1713-i-ml</a>

# PIC16(L)F1713/6

## 5.13 Power Control (PCON) Register

The PCON register bits are shown in Register 5-2.

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset ( $\overline{\text{POR}}$ )
- Brown-out Reset ( $\overline{\text{BOR}}$ )
- Reset Instruction Reset ( $\overline{\text{RI}}$ )
- MCLR Reset ( $\overline{\text{RMCLR}}$ )
- Watchdog Timer Reset ( $\overline{\text{RWDT}}$ )
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)

## 5.14 Register Definitions: Power Control

REGISTER 5-2: PCON: POWER CONTROL REGISTER

R/W/HS-0/q	R/W/HS-0/q	U-0	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

### Legend:

HC = Bit is cleared by hardware

HS = Bit is set by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-m/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7 **STKOVF:** Stack Overflow Flag bit

1 = A Stack Overflow occurred

0 = A Stack Overflow has not occurred or cleared by firmware

bit 6 **STKUNF:** Stack Underflow Flag bit

1 = A Stack Underflow occurred

0 = A Stack Underflow has not occurred or cleared by firmware

bit 5 **Unimplemented:** Read as '0'

bit 4  **$\overline{\text{RWDT}}$ :** Watchdog Timer Reset Flag bit

1 = A Watchdog Timer Reset has not occurred or set to '1' by firmware

0 = A Watchdog Timer Reset has occurred (cleared by hardware)

bit 3  **$\overline{\text{RMCLR}}$ :** MCLR Reset Flag bit

1 = A  $\overline{\text{MCLR}}$  Reset has not occurred or set to '1' by firmware

0 = A MCLR Reset has occurred (cleared by hardware)

bit 2  **$\overline{\text{RI}}$ :** RESET Instruction Flag bit

1 = A RESET instruction has not been executed or set to '1' by firmware

0 = A RESET instruction has been executed (cleared by hardware)

bit 1  **$\overline{\text{POR}}$ :** Power-on Reset Status bit

1 = No Power-on Reset occurred

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0  **$\overline{\text{BOR}}$ :** Brown-out Reset Status bit

1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

## 6.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 6-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

1. IRCF<3:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. The new clock is now active.
6. The OSCSTAT register is updated as required.
7. Clock switch is complete.

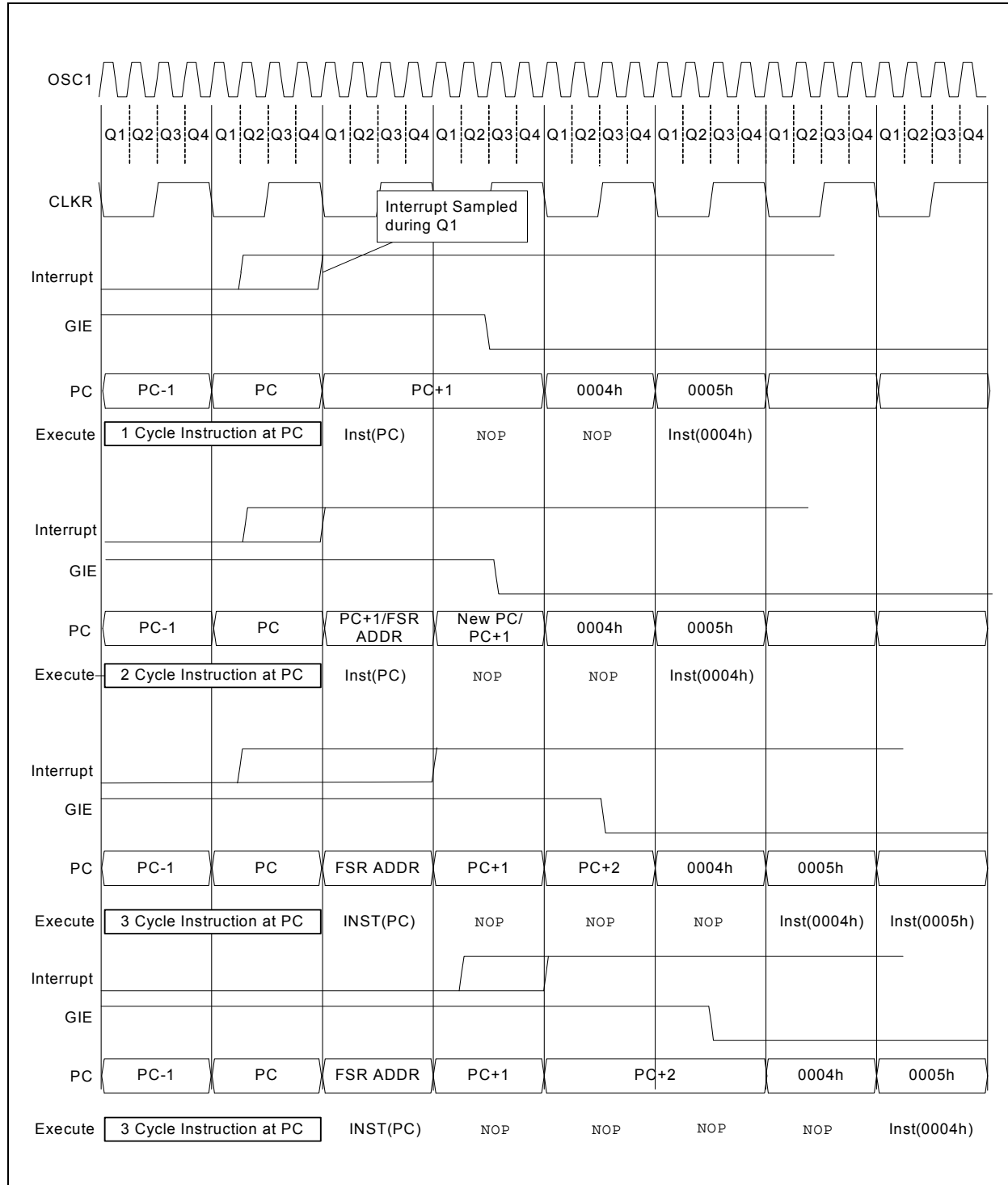
See Figure 6-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 6-1.

Start-up delay specifications are located in the oscillator tables of **Section 34.0 “Electrical Specifications”**.

# PIC16(L)F1713/6

**FIGURE 7-2: INTERRUPT LATENCY**



## REGISTER 7-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7	<b>TMR1GIF:</b> Timer1 Gate Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 6	<b>ADIF:</b> Analog-to-Digital Converter (ADC) Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 5	<b>RCIF:</b> USART Receive Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 4	<b>TXIF:</b> USART Transmit Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 3	<b>SSP1IF:</b> Synchronous Serial Port (MSSP) Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 2	<b>CCP1IF:</b> CCP1 Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 1	<b>TMR2IF:</b> Timer2 to PR2 Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending
bit 0	<b>TMR1IF:</b> Timer1 Overflow Interrupt Flag bit 1 = Interrupt is pending 0 = Interrupt is not pending

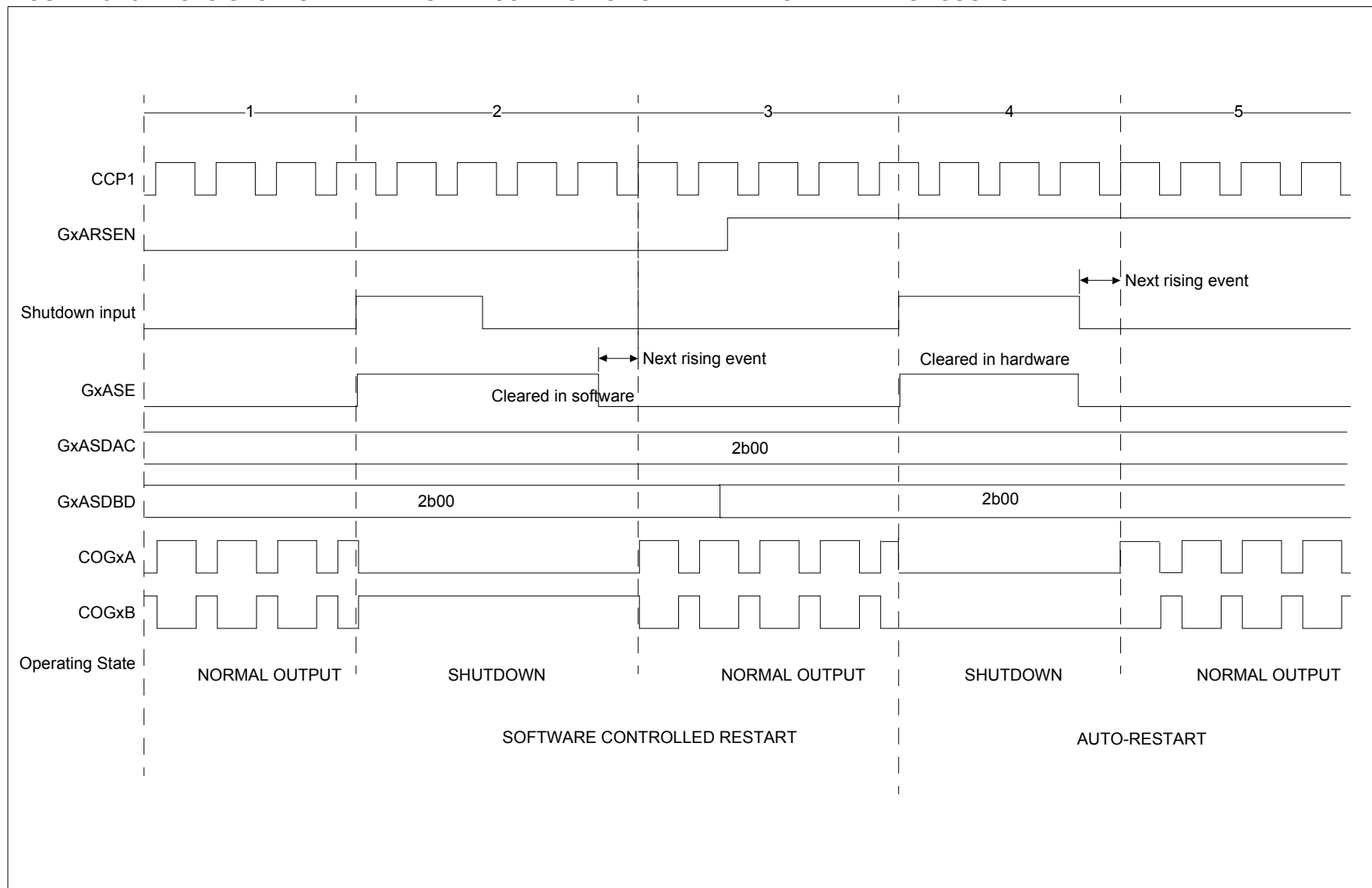
**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**TABLE 11-5: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSEL	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	131
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	132
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	130
ODCONC	ODC7	ODC6	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	132
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	130
SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	132
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	130
WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	131

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

FIGURE 18-15: AUTO-SHUTDOWN WAVEFORM – CCP1 AS RISING AND FALLING EVENT INPUT SOURCE



# PIC16(L)F1713/6

## REGISTER 18-12: COGxBLKR: COG RISING EVENT BLANKING COUNT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	GxBLKR<5:0>					
bit 7		bit 0					

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-6      **Unimplemented:** Read as '0'

bit 5-0      **GxBLKR<5:0>:** Rising Event Blanking Count Value bits  
= Number of COGx clock periods to inhibit falling event inputs

## REGISTER 18-13: COGxBLKF: COG FALLING EVENT BLANKING COUNT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	GxBLKF<5:0>					
bit 7		bit 0					

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-6      **Unimplemented:** Read as '0'

bit 5-0      **GxBLKF<5:0>:** Falling Event Blanking Count Value bits  
= Number of COGx clock periods to inhibit rising event inputs



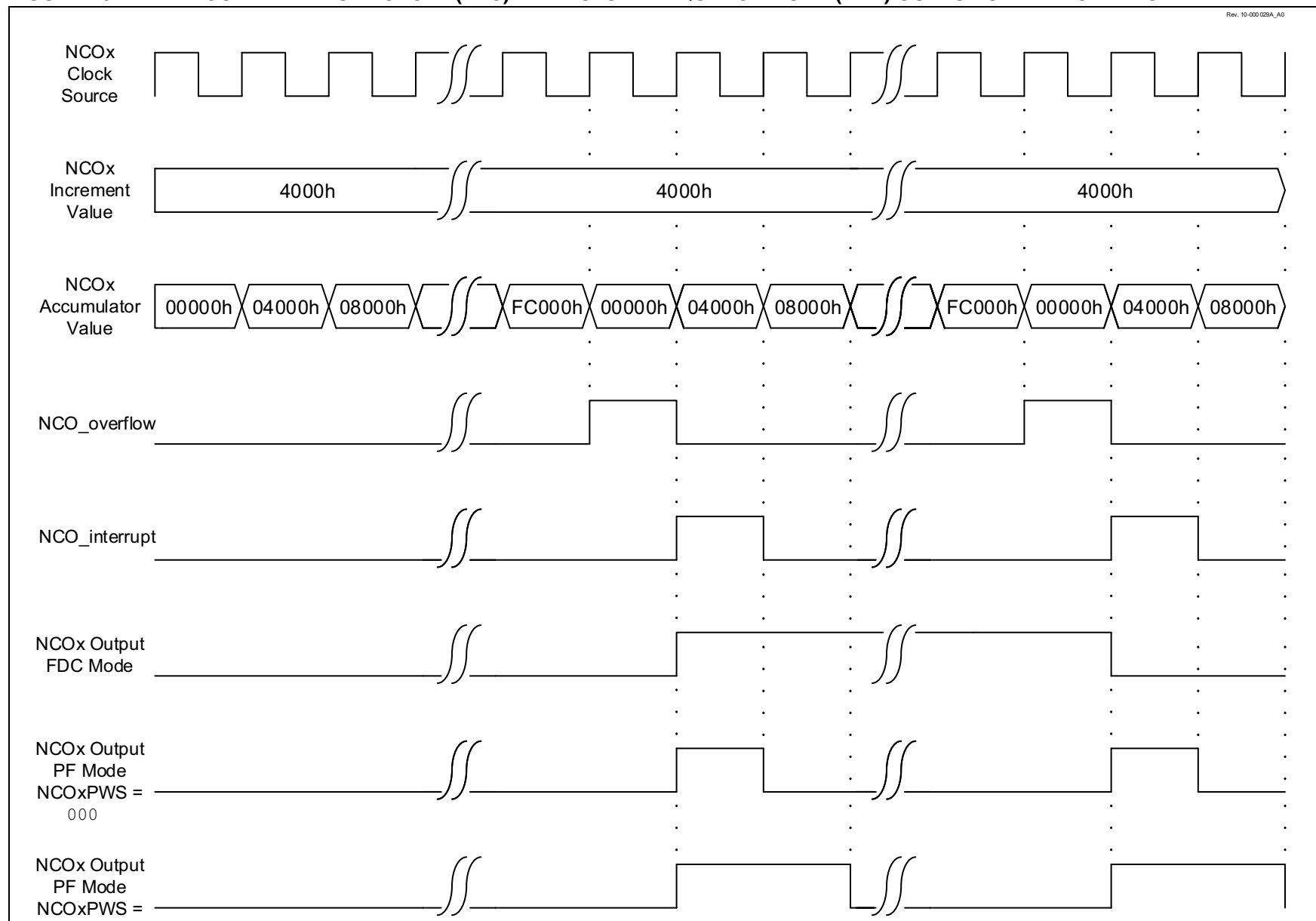
# PIC16(L)F1713/6

**TABLE 18-2: SUMMARY OF REGISTERS ASSOCIATED WITH COG**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	120
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	126
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	131
COG1PHR	—	—	G1PHR<5:0>						201
COG1PHF	—	—	G1PHF<5:0>						201
COG1BLKR	—	—	G1BLKR<5:0>						200
COG1BLKF	—	—	G1BLKF<5:0>						200
COG1DBR	—	—	G1DBR<5:0>						199
COG1DBF	—	—	G1DBF<5:0>						199
COG1RIS	G1RIS7	G1RIS6	G1RIS5	G1RIS4	G1RIS3	G1RIS2	G1RIS1	G1RIS0	190
COG1RSIM	G1RSIM7	G1RSIM6	G1RSIM5	G1RSIM4	G1RSIM3	G1RSIM2	G1RSIM1	G1RSIM0	191
COG1FIS	G1FIS7	G1FIS6	G1FIS5	G1FIS4	G1FIS3	G1FIS2	G1FIS1	G1FIS0	193
COG1FSIM	G1FSIM7	G1FSIM6	G1FSIM5	G1FSIM4	G1FSIM3	G1FSIM2	G1FSIM1	G1FSIM0	194
COG1CON0	G1EN	G1LD	—	G1CS<1:0>		G1MD<2:0>			188
COG1CON1	G1RDBS	G1FDBS	—	—	G1POLD	G1POLC	G1POLB	G1POLA	189
COG1ASD0	G1ASE	G1ARSEN	G1ASDBD<1:0>		G1ASDAC<1:0>		—	—	196
COG1ASD1	—	—	—	—	G1AS3E	G1AS2E	G1AS1E	G1AS0E	197
COG1STR	G1SDATD	G1SDATC	G1SDATB	G1SDATA	G1STRD	G1STRC	G1STRB	G1STRA	198
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	83
COG1PPS	—	—	—	COG1PPS<4:0>					136
PIE2	OSFIE	C2IE	C1IE	—	BCL1IE	TMR6IE	TMR4IE	CCP2IE	85
PIR2	OSFIF	C2IF	C1IF	—	BCL1IF	TMR6IF	TMR4IF	CCP2IF	88
RxyPPS	—	—	—	RxyPPS<4:0>					137

**Legend:** x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by COG.

**FIGURE 20-2: NCO – FIXED DUTY CYCLE (FDC) AND PULSE FREQUENCY MODE (PFM) OUTPUT OPERATION DIAGRAM**



## 23.6 Register Definitions: DAC Control

### REGISTER 23-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS
bit 7							bit 0

#### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged                      x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
 '1' = Bit is set                      '0' = Bit is cleared

bit 7                      **DAC1EN:** DAC1 Enable bit  
                             1 = DAC is enabled  
                             0 = DAC is disabled  
  
 bit 6                      **Unimplemented:** Read as '0'  
 bit 5                      **DAC1OE1:** DAC1 Voltage Output 1 Enable bit  
                             1 = DAC voltage level is also an output on the DAC1OUT1 pin  
                             0 = DAC voltage level is disconnected from the DAC1OUT1 pin  
  
 bit 4                      **DAC1OE2:** DAC1 Voltage Output 2 Enable bit  
                             1 = DAC voltage level is also an output on the DAC1OUT2 pin  
                             0 = DAC voltage level is disconnected from the DAC1OUT2 pin  
  
 bit 3-2                      **DAC1PSS<1:0>:** DAC1 Positive Source Select bits  
                             11 = Reserved, do not use  
                             10 = FVR Buffer2 output  
                             01 = VREF+ pin  
                             00 = VDD  
  
 bit 1                      **Unimplemented:** Read as '0'  
 bit 0                      **DAC1NSS:** DAC1 Negative Source Select bits  
                             1 = VREF- pin  
                             0 = VSS

### REGISTER 23-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DAC1R<7:0>							
bit 7							bit 0

#### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged                      x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
 '1' = Bit is set                      '0' = Bit is cleared

bit 7-0                      **DAC1R<7:0>:** DAC1 Voltage Output Select bits

### TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC1 MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	249
DAC1CON1	DAC1R<7:0>								249

**Legend:** — = Unimplemented location, read as '0'. Shaded cells are not used with the DAC module.

The pull-up and pull-down resistor values are significantly affected by small variations of ZCPINV. Measuring ZCPINV can be difficult, especially when the waveform is relative to VDD. However, by combining Equations 28-2 and 28-3, the resistor value can be determined from the time difference between the ZCDx\_output high and low periods. Note that the time difference, ΔT, is 4\*TOFFSET. The equation for determining the pull-up and pull-down resistor values from the high and low ZCDx\_output periods is shown in Equation 28-4. The ZCDx\_output signal can be directly observed on a pin by routing the ZCDx\_output signal through one of the CLCs.

## EQUATION 28-4:

$$R = R_{SERIES} \left( \frac{V_{BIAS}}{V_{PEAK} \left( \sin \left( \pi Freq \frac{(\Delta T)}{2} \right) \right)} - 1 \right)$$

R is pull-up or pull-down resistor.

VBIAS is VPULLUP when R is pull-up or VDD when R is pull-down.

ΔT is the ZCDOUT high and low period difference.

## 28.6 Handling VPEAK Variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of ± 600 μA and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed ± 600 μA and the minimum is at least ± 100 μA, compute the series resistance as shown in Equation 28-5. The compensating pull-up for this series resistance can be determined with Equation 28-3 because the pull-up value is independent from the peak voltage.

## EQUATION 28-5: SERIES R FOR V RANGE

$$R_{SERIES} = \frac{V_{MAXPEAK} + V_{MINPEAK}}{7 \times 10^{-4}}$$

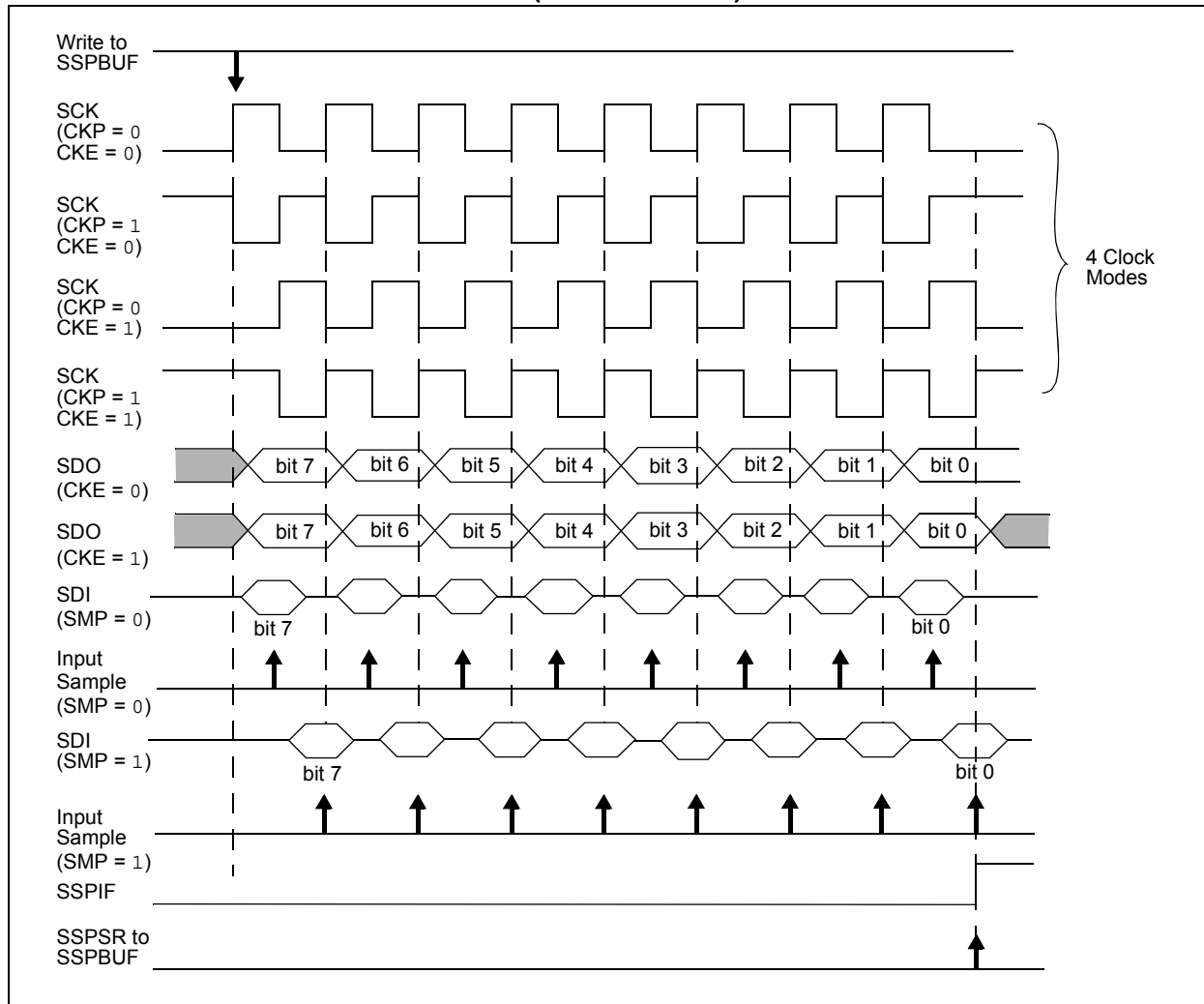
## 28.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

## 28.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-on Reset (POR). When the ZCDDIS Configuration bit is cleared, the ZCD circuit will be active at POR. When the ZCDDIS Configuration bit is set, the ZCDxEN bit of the ZCDxCON register must be set to enable the ZCD module.

**FIGURE 30-6: SPI MODE WAVEFORM (MASTER MODE)**



## 30.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit of the SSPCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

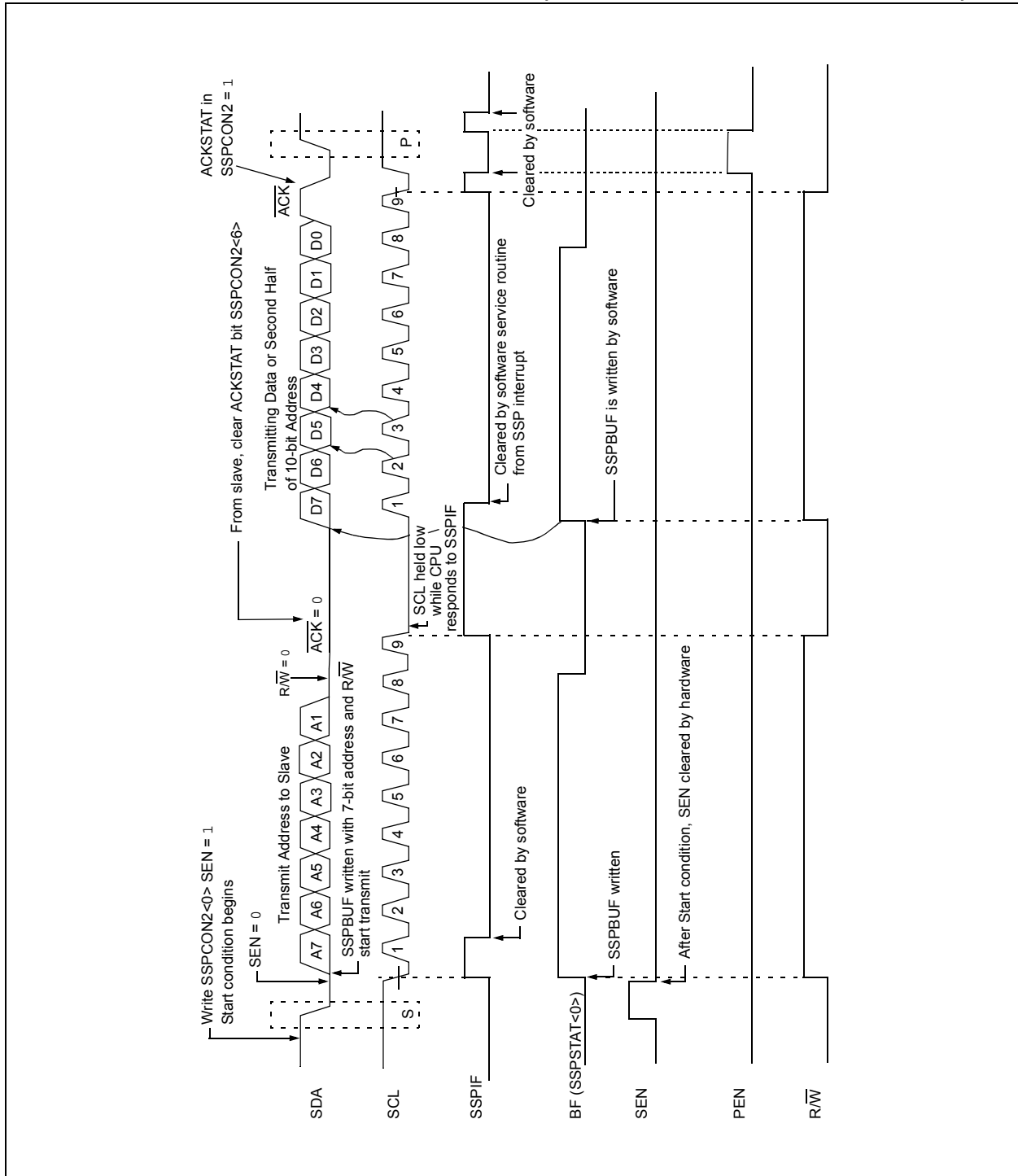
### Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 30-7 shows the block diagram of a typical daisy-chain connection when operating in SPI mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPCON3 register will enable writes to the SSPBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

**FIGURE 30-28: I<sup>2</sup>C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)**



# PIC16(L)F1713/6

## 30.8 Register Definitions: MSSP Control

### REGISTER 30-1: SSP1STAT: SSP STATUS REGISTER

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
SMP	CKE	D/A	P	S	R/W	UA	BF
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	<b>SMP:</b> SPI Data Input Sample bit <u>SPI Master mode:</u> 1 = Input data sampled at end of data output time 0 = Input data sampled at middle of data output time <u>SPI Slave mode:</u> SMP must be cleared when SPI is used in Slave mode <u>In I<sup>2</sup>C Master or Slave mode:</u> 1 = Slew rate control disabled for Standard Speed mode (100 kHz and 1 MHz) 0 = Slew rate control enabled for High-Speed mode (400 kHz)
bit 6	<b>CKE:</b> SPI Clock Edge Select bit (SPI mode only) <u>In SPI Master or Slave mode:</u> 1 = Transmit occurs on transition from active to Idle clock state 0 = Transmit occurs on transition from Idle to active clock state <u>In I<sup>2</sup>C™ mode only:</u> 1 = Enable input logic so that thresholds are compliant with SMBus specification 0 = Disable SMBus specific inputs
bit 5	<b>D/A:</b> Data/Address bit (I <sup>2</sup> C mode only) 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address
bit 4	<b>P:</b> Stop bit (I <sup>2</sup> C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.) 1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset) 0 = Stop bit was not detected last
bit 3	<b>S:</b> Start bit (I <sup>2</sup> C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.) 1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset) 0 = Start bit was not detected last
bit 2	<b>R/W:</b> Read/Write bit information (I <sup>2</sup> C mode only) This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit. <u>In I<sup>2</sup>C Slave mode:</u> 1 = Read 0 = Write <u>In I<sup>2</sup>C Master mode:</u> 1 = Transmit is in progress 0 = Transmit is not in progress OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.
bit 1	<b>UA:</b> Update Address bit (10-bit I <sup>2</sup> C mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated
bit 0	<b>BF:</b> Buffer Full Status bit <u>Receive (SPI and I<sup>2</sup>C modes):</u> 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty <u>Transmit (I<sup>2</sup>C mode only):</u> 1 = Data transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data transmit complete (does not include the ACK and Stop bits), SSPBUF is empty

# PIC16(L)F1713/6

**TABLE 31-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)**

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—



## 31.5.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

<b>Note:</b> If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.
---

## 31.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

<b>Note:</b> If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.
--

## 31.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

## 31.5.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

## 31.5.1.9 Synchronous Master Reception Setup:

1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

# PIC16(L)F1713/6

FIGURE 34-1: VOLTAGE FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , PIC16F1713/6 ONLY

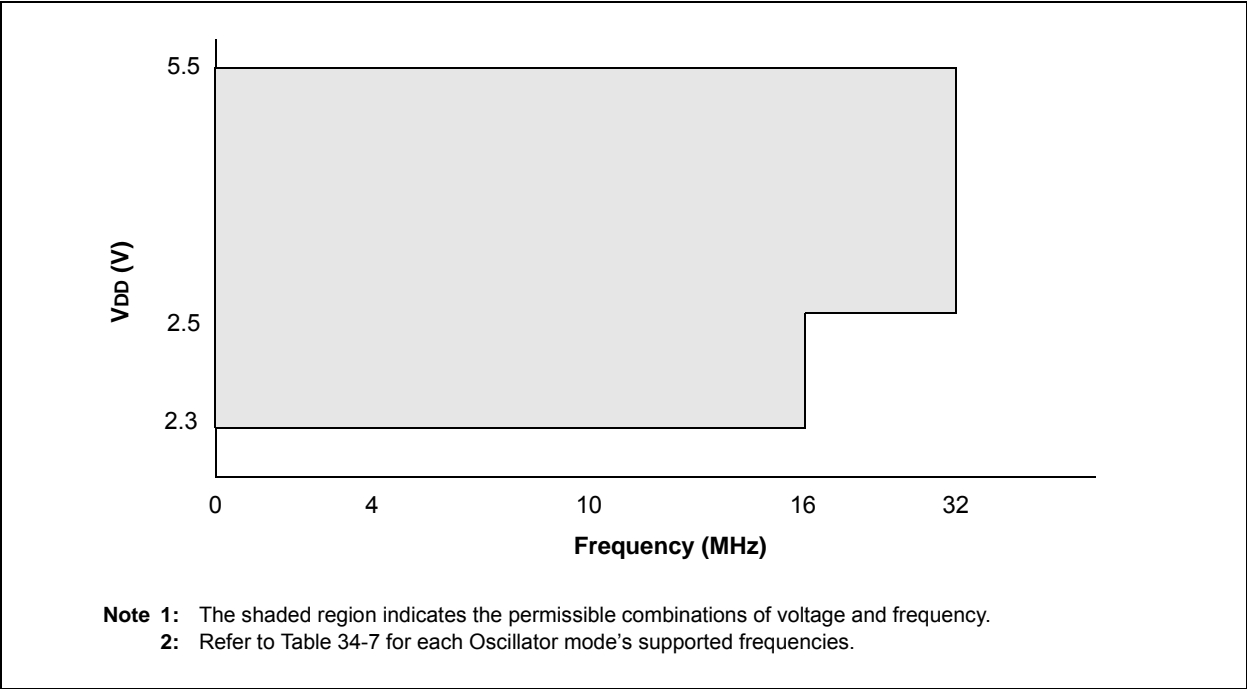
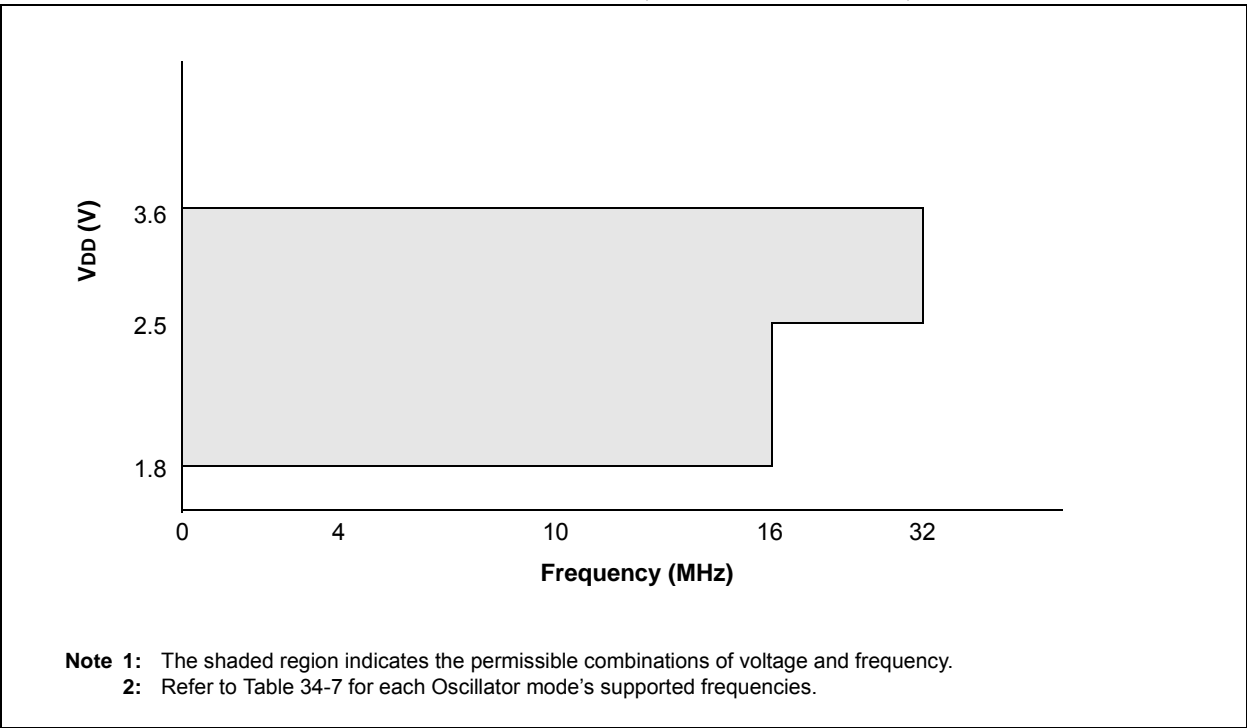
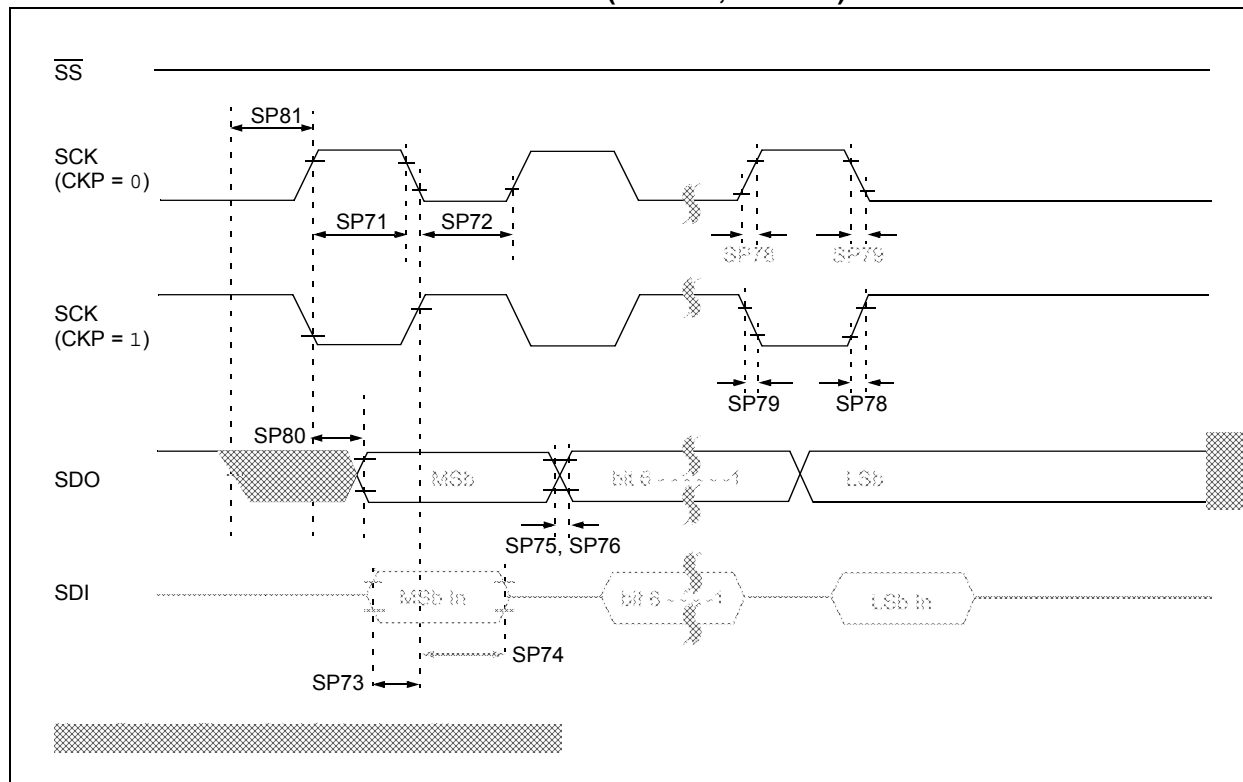


FIGURE 34-2: VOLTAGE FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , PIC16LF1713/6 ONLY

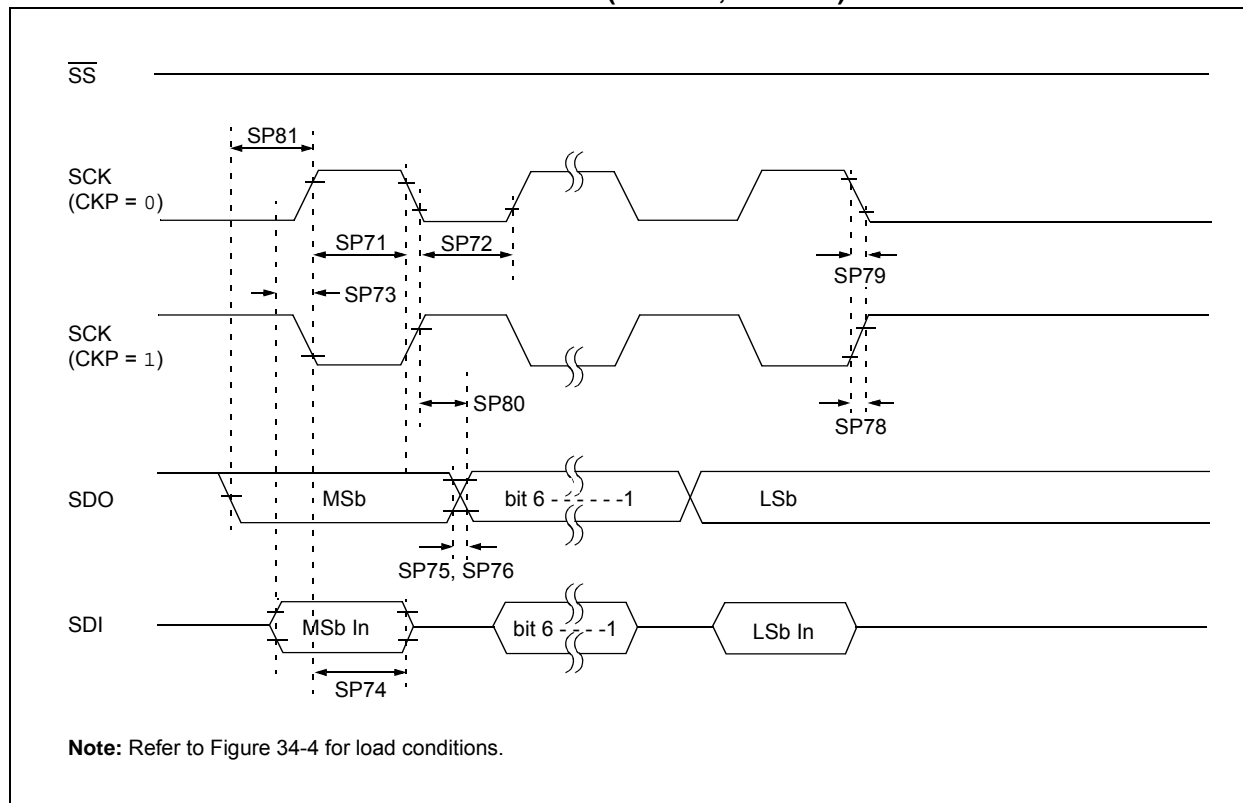


# PIC16(L)F1713/6

**FIGURE 34-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)**

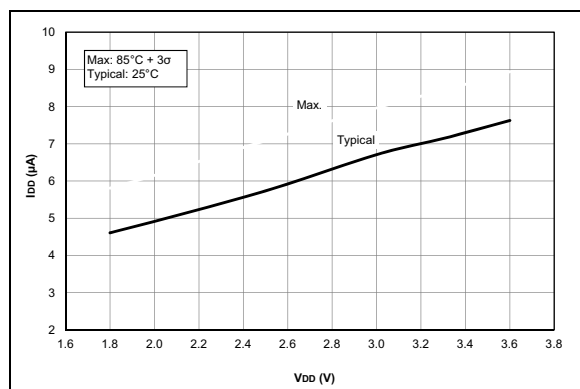


**FIGURE 34-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)**

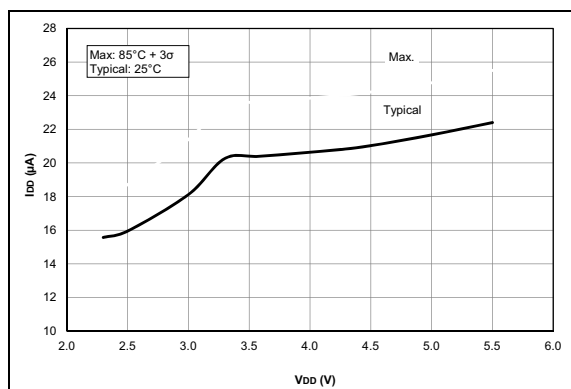


# PIC16(L)F1713/6

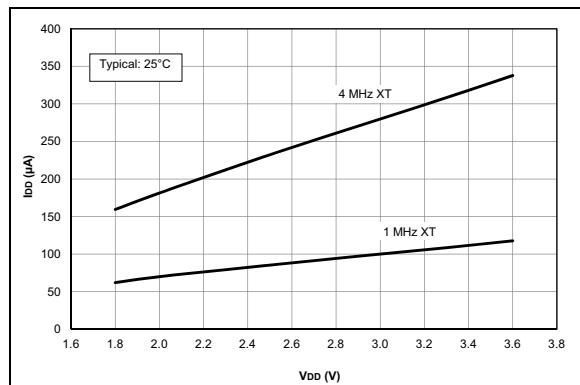
**Note:** Unless otherwise noted,  $V_{IN} = 5V$ ,  $F_{OSC} = 300\text{ kHz}$ ,  $C_{IN} = 0.1\text{ }\mu\text{F}$ ,  $T_A = 25^\circ\text{C}$ .



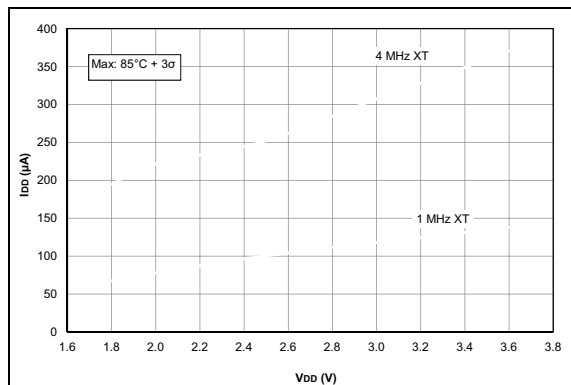
**FIGURE 35-1:**  $I_{DD}$ , LP Oscillator Mode,  $F_{osc} = 32\text{ kHz}$ , PIC16LF1713/6 Only.



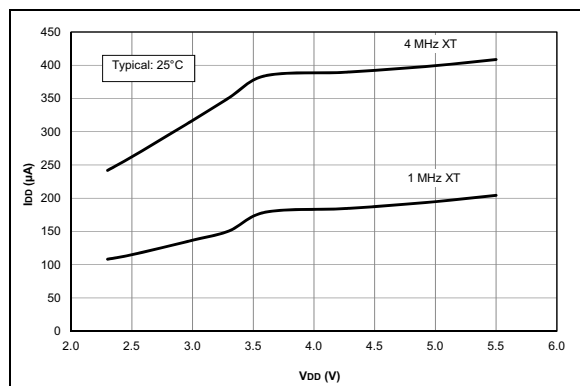
**FIGURE 35-2:**  $I_{DD}$ , LP Oscillator Mode,  $F_{osc} = 32\text{ kHz}$ , PIC16F1713/6 Only.



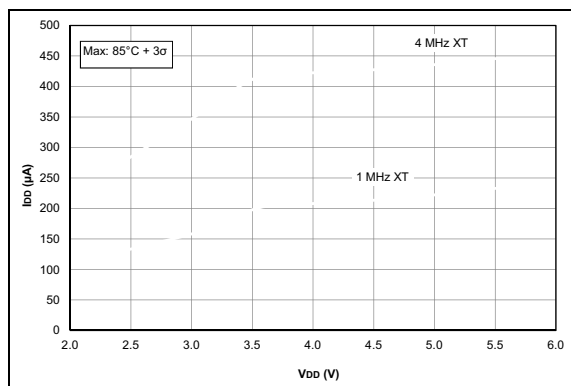
**FIGURE 35-3:**  $I_{DD}$  Typical, XT and EXTRC Oscillator, PIC16LF1713/6 Only.



**FIGURE 35-4:**  $I_{DD}$  Maximum, XT and EXTRC Oscillator, PIC16LF1713/6 Only.



**FIGURE 35-5:**  $I_{DD}$  Typical, XT and EXTRC Oscillator, PIC16F1713/6 Only.

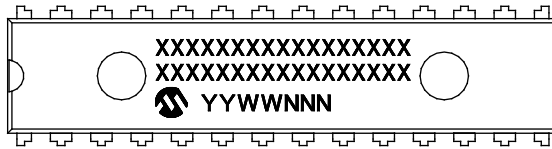


**FIGURE 35-6:**  $I_{DD}$  Maximum, XT and EXTRC Oscillator, PIC16F1713/6 Only.

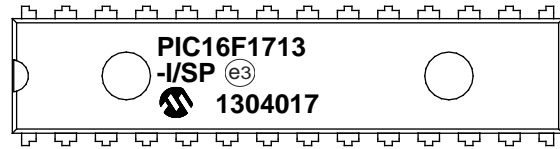
## 37.0 PACKAGING INFORMATION

### 37.1 Package Marking Information

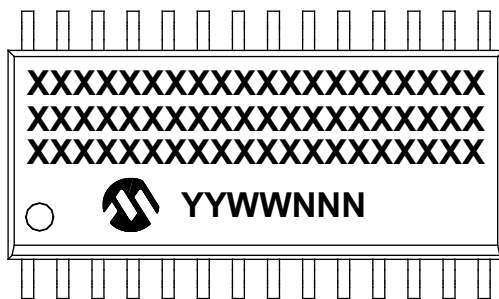
28-Lead SPDIP (.300")



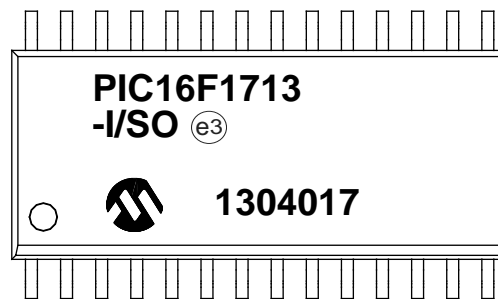
Example



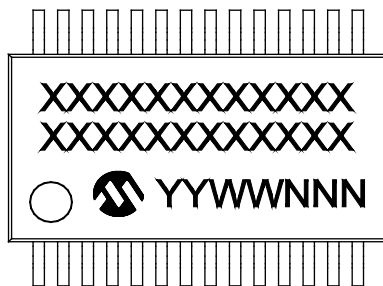
28-Lead SOIC (7.50 mm)



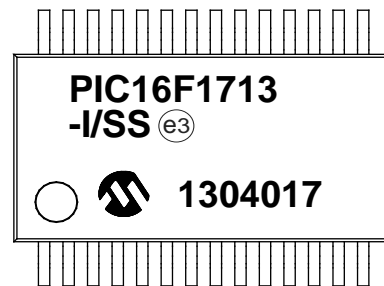
Example



28-Lead SSOP (5.30 mm)



Example



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.