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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1716-i-mv

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3.3.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-10.

|--|

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection is controlled independently. Internal access to the program memory is unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the \overline{CP} bit in Configuration Words. When $\overline{CP} = 0$, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.4** "Write **Protection**" for more information.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 10.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F170X Memory Programming Specification"* (DS41683).

5.12 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON register are updated to indicate the cause of the Reset. Table 5-3 and Table 5-4 show the Reset conditions of these registers.

STKOVF	STKUNF	RWDT	RMCLR	RI	POR	BOR	то	PD	Condition
0	0	1	1	1	0	x	1	1	Power-on Reset
0	0	1	1	1	0	x	0	x	Illegal, TO is set on POR
0	0	1	1	1	0	x	x	0	Illegal, PD is set on POR
0	0	u	1	1	u	0	1	1	Brown-out Reset
u	u	0	u	u	u	u	0	u	WDT Reset
u	u	u	u	u	u	u	0	0	WDT Wake-up from Sleep
u	u	u	u	u	u	u	1	0	Interrupt Wake-up from Sleep
u	u	u	0	u	u	u	u	u	MCLR Reset during normal operation
u	u	u	0	u	u	u	1	0	MCLR Reset during Sleep
u	u	u	u	0	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)

TABLE 5-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

TABLE 5-4: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	1 1000	00 110x
MCLR Reset during normal operation	0000h	u uuuu	uu Ouuu
MCLR Reset during Sleep	0000h	1 Ouuu	uu Ouuu
WDT Reset	0000h	0 uuuu	uu uuuu
WDT Wake-up from Sleep	PC + 1	0 Ouuu	uu uuuu
Brown-out Reset	0000h	1 luuu	00 11u0
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	1 Ouuu	uu uuuu
RESET Instruction Executed	0000h	u uuuu	uu u0uu
Stack Overflow Reset (STVREN = 1)	0000h	u uuuu	lu uuuu
Stack Underflow Reset (STVREN = 1)	0000h	u uuuu	ul uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	83
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>		256	
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	84
PIE2	OSFIE	C2IE	C1IE	_	BCL1IE	TMR6IE	TMR4IE	CCP2IE	85
PIE3	—	NCOIE	COGIE	ZCDIE	CLC4IE	CLC3IE	CLC2IE	CLC1IE	86
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	87
PIR2	OSFIF	C2IF	C1IF	_	BCL1IF	TMR6IF	TMR4IF	CCP2IF	88
PIR3	_	NCOIF	COGIF	ZCDIF	CLC4IF	CLC3IF	CLC2IF	CLC1IF	89

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

u = Bit is unchanged

'1' = Bit is set

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				

REGISTER 13-9: IOCCF: INTERRUPT-ON-CHANGE PORTC FLAG REGISTER

bit 7-0 **IOCCF<7:0>:** Interrupt-on-Change PORTC Flag bits

x = Bit is unknown

'0' = Bit is cleared

1 = An enabled change was detected on the associated pin.

Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.

HS - Bit is set in hardware

-n/n = Value at POR and BOR/Value at all other Resets

0 = No change was detected, or the user cleared the detected change.

REGISTER 13-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4	Unimplemented:	Read as '0'
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1.11.0	
DIT 3	IUCEP: Interrupt-on-Change PORTE Positive Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCEFx bit and IOCIF flag will be set upon detecting an edge.
 - 0 = Interrupt-on-Change disabled for the associated pin.

bit 2-0 Unimplemented: Read as '0'

16.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 16-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10 \text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

- Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
 - 2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.





16.11 Register Definitions: Comparator Control

REGISTER 16-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	U-0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0		
CxON	CxOUT	—	CxPOL	CxZLF	CxSP	CxHYS	CxSYNC		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'			
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all	other Resets		
'1' = Bit is set		'0' = Bit is clea	ared						
bit 7 CxON: Comparator Enable bit 1 = Comparator is enabled 0 = Comparator is disabled and consumes no active power									
bit 6	CxOUT: Comparator Output bit $\frac{\text{If CxPOL} = 1 \text{ (inverted polarity):}}{1 = CxVP < CxVN}$ $0 = CxVP > CxVN$ $\frac{\text{If CxPOL} = 0 \text{ (non-inverted polarity):}}{1 = CxVP > CxVN}$ $0 = CxVP > CxVN$								
bit 5	Unimplemen	ted: Read as '	0'						
bit 4	CxPOL: Comparator Output Polarity Select bit 1 = Comparator output is inverted 0 = Comparator output is not inverted								
bit 3	CxZLF: Comparator Zero Latency Filter Enable bit 1 = Comparator output is filtered 0 = Comparator output is unfiltered								
bit 2	CxSP: Comparator Speed/Power Select bit 1 = Comparator operates in normal power, higher speed mode 0 = Comparator operates in low-power, low-speed mode								
bit 1	CxHYS: Comparator Hysteresis Enable bit 1 = Comparator hysteresis enabled 0 = Comparator hysteresis disabled								
bit 0	 0 = Comparator hysteresis disabled CxSYNC: Comparator Output Synchronous Mode bit 1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source. 0 = Comparator output to Timer1 and I/O pin is asynchronous. 								



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18.4 Output Control

Upon disabling, or immediately after enabling the COG module, the primary COG outputs are inactive and complementary COG outputs are active.

18.4.1 OUTPUT ENABLES

There are no output enable controls in the COG module. Instead, each device pin has an individual output selection control called the PPS register. All four COG outputs are available for selection in the PPS register of every pin.

When a COG output is enabled by PPS selection, the output on the pin has several possibilities, which depend on the steering control, GxEN bit, and shutdown state as shown in Table 18-1

GxEN	COGxSTR bit	Shutdown	Output
х	0	Inactive	Static steering data
x	1	Active	Shutdown override
0	1	Inactive	Inactive state
1	1	Inactive	Active PWM signal

TABLE 18-1: PIN OUTPUT STATES

18.4.2 POLARITY CONTROL

The polarity of each COG output can be selected independently. When the output polarity bit is set, the corresponding output is active low. Clearing the output polarity bit configures the corresponding output as active high. However, polarity affects the outputs in only one of the four shutdown override modes. See Section 18.8, Auto-shutdown Control for more details.

Output polarity is selected with the GxPOLA through GxPOLD bits of the COGxCON1 register (Register 18-2).

18.5 Dead-Band Control

The dead-band control provides for non-overlapping PWM output signals to prevent shoot-through current in the external power switches. Dead time affects the output only in the Half-Bridge mode and when changing direction in the Full-Bridge mode.

The COG contains two dead-band timers. One dead-band timer is used for rising event dead-band control. The other is used for falling event dead-band control. Timer modes are selectable as either:

- Asynchronous delay chain
- Synchronous counter

The dead-band timer mode is selected for the rising_event and falling_event dead-band times with the respective GxRDBS and GxFDBS bits of the COGxCON1 register (Register 18-2).

In Half-Bridge mode, the rising_event dead-band time delays all selected primary outputs from going active for the selected dead time after the rising event. COGxA and COGxC are the primary outputs in Half-Bridge mode.

In Half-Bridge mode, the falling_event dead-band time delays all selected complementary outputs from going active for the selected dead time after the falling event. COGxB and COGxD are the complementary outputs in Half-Bridge mode.

In Full-Bridge mode, the dead-time delay occurs only during direction changes. The modulated output is delayed for the falling_event dead time after a direction change from forward to reverse. The modulated output is delayed for the rising_event dead time after a direction change from reverse to forward.

18.5.1 ASYNCHRONOUS DELAY CHAIN DEAD-BAND DELAY

Asynchronous dead-band delay is determined by the time it takes the input to propagate through a series of delay elements. Each delay element is a nominal five nanoseconds.

Set the COGxDBR register (Register 18-10) value to the desired number of delay elements in the rising_event dead-band time. Set the COGxDBF register (Register 18-11) value to the desired number of delay elements in the falling_event dead-band time. When the value is zero, dead-band delay is disabled.

18.5.2 SYNCHRONOUS COUNTER DEAD-BAND DELAY

Synchronous counter dead band is timed by counting COG_clock periods from zero up to the value in the dead-band count register. Use Equation 18-1 to calculate dead-band times.

Set the COGxDBR count register value to obtain the desired rising_event dead-band time. Set the COGxDBF count register value to obtain the desired falling_event dead-band time. When the value is zero, dead-band delay is disabled.

18.5.3 SYNCHRONOUS COUNTER DEAD-BAND TIME UNCERTAINTY

When the rising and falling events that trigger the dead-band counters come from asynchronous inputs, it creates uncertainty in the synchronous counter dead-band time. The maximum uncertainty is equal to one COG_clock period. Refer to Example 18-1 for more detail.

When event input sources are asynchronous with no phase delay, use the asynchronous delay chain dead-band mode to avoid the dead-band time uncertainty.

18.9 Buffer Updates

Changes to the phase, dead band, and blanking count registers need to occur simultaneously during COG operation to avoid unintended operation that may occur as a result of delays between each register write. This is accomplished with the GxLD bit of the COGxCON0 register and double buffering of the phase, blanking, and dead-band count registers.

Before the COG module is enabled, writing the count registers loads the count buffers without need of the GxLD bit. However, when the COG is enabled, the count buffer updates are suspended after writing the count registers until after the GxLD bit is set. When the GxLD bit is set, the phase, dead-band, and blanking register values are transferred to the corresponding buffers synchronous with COG operation. The GxLD bit is cleared by hardware when the transfer is complete.

18.10 Input and Output Pin Selection

The COG has one selection for an input from a device pin. That one input can be used as rising and falling event source or a fault source. The COG1PPS register is used to select the pin. Refer to Register 12-1 and Register 12-2.

The pin PPS control registers are used to enable the COG outputs. Any combination of outputs to pins is possible including multiple pins for the same output. See the RxyPPS control register and **Section 12.2 "PPS Outputs"** for more details.

18.11 Operation During Sleep

The COG continues to operate in Sleep provided that the COG_clock, rising event, and falling event sources remain active.

The HFINTSOC remains active during Sleep when the COG is enabled and the HFINTOSC is selected as the COG_clock source.

18.12 Configuring the COG

The following steps illustrate how to properly configure the COG to ensure a synchronous start with the rising event input:

- 1. If a pin is to be used for the COG fault or event input, use the COGxPPS register to configure the desired pin.
- 2. Clear all ANSEL register bits associated with pins that are used for COG functions.
- 3. Ensure that the TRIS control bits corresponding to the COG outputs to be used are cleared so that all are configured as inputs. The COG module will disable the output drivers as needed for shutdown.
- 4. Clear the GxEN bit, if not already cleared.
- 5. Set desired dead-band times with the COGxDBR and COGxDBF registers and select the source with the COGxRDBS and COGxFDBS bits of the COGxCON1 register.
- 6. Set desired blanking times with the COGxBLKR and COGxBLKF registers.
- 7. Set desired phase delay with the COGxPHR and COGxPHF registers.
- 8. Select the desired shutdown sources with the COGxASD1 register.
- 9. Setup the following controls in COGxASD0 auto-shutdown register:
 - Select both output override controls to the desired levels (this is necessary, even if not using auto-shutdown because start-up will be from a shutdown state).
 - Set the GxASE bit and clear the GxARSEN bit.
- 10. Select the desired rising and falling event sources with the COGxRIS and COGxFIS registers.
- 11. Select the desired rising and falling event modes with the COGxRSIM and COGxFSIM registers.
- 12. Configure the following controls in the COGxCON1 register:
 - Select the desired clock source
 - Select the desired dead-band timing sources
- 13. Configure the following controls in the COGxSTR register:
 - Set the steering bits of the outputs to be used.
 - Set the static levels.
- 14. Set the polarity controls in the COGxCON1 register.
- 15. Set the GxEN bit.
- 16. Set the pin PPS controls to direct the COG outputs to the desired pins.
- 17. If auto-restart is to be used, set the GxARSEN bit and the GxASE will be cleared automatically. Otherwise, clear the GxASE bit to start the COG.

20.2 Fixed Duty Cycle (FDC) Mode

In Fixed Duty Cycle (FDC) mode, every time the accumulator overflows (NCO_overflow), the output is toggled. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see Figure 20-2.

The FDC mode is selected by clearing the NxPFM bit in the NCOxCON register.

20.3 Pulse Frequency (PF) Mode

In Pulse Frequency (PF) mode, every time the accumulator overflows (NCO_overflow), the output becomes active for one or more clock periods. Once the clock period expires, the output returns to an inactive state. This provides a pulsed output.

The output becomes active on the rising clock edge immediately following the overflow event. For more information, see Figure 20-2.

The value of the active and inactive states depends on the polarity bit, NxPOL in the NCOxCON register.

The PF mode is selected by setting the NxPFM bit in the NCOxCON register.

20.3.1 OUTPUT PULSE WIDTH CONTROL

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the NxPWS<2:0> bits in the NCOxCLK register.

When the selected pulse width is greater than the accumulator overflow time frame, the output of the NCOx operation is indeterminate.

20.4 Output Polarity Control

The last stage in the NCOx module is the output polarity. The NxPOL bit in the NCOxCON register selects the output polarity. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

The NCOx output can be used internally by source code or other peripherals. Accomplish this by reading the NxOUT (read-only) bit of the NCOxCON register.

The NCOx output signal is available to the following peripherals:

- CLC
- CWG

20.5 Interrupts

When the accumulator overflows (NCO_overflow), the NCOx Interrupt Flag bit, NCOxIF, of the PIRx register is set. To enable the interrupt event (NCO_interrupt), the following bits must be set:

- NxEN bit of the NCOxCON register
- NCOxIE bit of the PIEx register
- PEIE bit of the INTCON register
- · GIE bit of the INTCON register

The interrupt must be cleared by software by clearing the NCOxIF bit in the Interrupt Service Routine.

20.6 Effects of a Reset

All of the NCOx registers are cleared to zero as the result of a Reset.

20.7 Operation In Sleep

The NCO module operates independently from the system clock and will continue to run during Sleep, provided that the clock source selected remains active.

The HFINTOSC remains active during Sleep when the NCO module is enabled and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the NCO clock source, when the NCO is enabled, the CPU will go idle during Sleep, but the NCO will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

21.2 ADC Operation

21.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/DONE bit should not be set in the
	same instruction that turns on the ADC.
	Refer to Section 21.2.6 "ADC Conver-
	sion Procedure".

21.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF Interrupt Flag bit
- Update the ADRESH and ADRESL registers with new conversion result

21.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH and ADRESL registers will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

21.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

21.2.5 AUTO-CONVERSION TRIGGER

The Auto-conversion Trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the GO/DONE bit is set by hardware.

The Auto-conversion Trigger source is selected with the TRIGSEL<3:0> bits of the ADCON2 register.

Using the Auto-conversion Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See Table 21-2 for auto-conversion sources. TABLE 21-2: AUTO-CONVERSION SOURCES

Source Peripheral	Signal Name
CCP1	
CCP2	
Timer0	T0_overflow
Timer1	T1_overflow
Timer2	T2_match
Timer4	T4_match
Timer6	T6_match
Comparator C1	sync_C1OUT
Comparator C2	sync_C2OUT
CLC1	LC1_out
CLC2	LC2_out
CLC3	LC3_out
CLC4	LC4_out

26.11 Register Definitions: Timer1 Control

REGISTER 26-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	U-0	R/W-0/u
TMR1C	S<1:0>	T1CKP	S<1:0>	T1OSCEN	T1SYNC	_	TMR10N
bit 7							bit 0
[
Legend:							
R = Readable	bit	W = Writable I	oit	U = Unimplen	nented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkn	own	-n/n = Value a	at POR and BC	R/Value at all	other Resets
'1' = Bit is set '0' = Bit is cleared							
bit 7-6	TMR1CS<1:0 11 = LFINTO 10 = Timer1 of <u>If T10SC</u> <u>External</u> <u>If T10SC</u> Crystal of 01 = Timer1 of 00 = Timer1 of	>: Timer1 Cloc SC clock source is <u>CEN = 0</u> : clock from T1C <u>CEN = 1</u> : scillator on SO clock source is clock source is	k Source Sele pin or oscillat CKI pin (on the SCI/SOSCO system clock instruction clo	ect bits or: e rising edge) pins (Fosc) ock (Fosc/4)			
bit 5-4	T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value						
bit 3	T1OSCEN: LE 1 = Dedicated 0 = Dedicated	P Oscillator En d secondary os d secondary os	able Control b cillator circuit cillator circuit	it enabled disabled			
bit 2	T1SYNC: Timer1 Synchronization Control bit 1 = Do not synchronize asynchronous clock input 0 = Synchronize asynchronous clock input with system clock (Fosc)						
bit 1	Unimplement	ted: Read as ')'				
bit 0	TMR1ON: Tin 1 = Enables ⁻ 0 = Stops Tin	ner1 On bit Timer1 ner1 and clears	Timer1 gate	flip-flop			



30.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

- a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out (Case 1).
- b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high (Case 2).

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD and counts down to zero. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 30-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 30-39).

FIGURE 30-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)



FIGURE 30-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



REGISTER 30-5: SSP1MSK: SSP MASK REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
			MSK	<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimpler	nented bit, read	l as '0'		
u = Bit is unchanged x = I		x = Bit is unkr	nown	-n/n = Value at POR and BOR/Value at all other Resets			
'1' = Bit is set '0' = Bit is cleared							
bit 7-1	MSK<7:1>:	Mask bits					
	1 = The rec 0 = The rec	eived address b eived address b	it n is compar it n is not use	red to SSPADD d to detect I ² C	<n> to detect I² address match</n>	C address mat	tch
bit 0	MSK<0>: MiI2C Slave mo1 = The rec0 = The rec	ask bit for I ² C S ode, 10-bit addre eived address b eived address b	lave mode, 10 ess (SSPM<3 it 0 is compar it 0 is not use	0-bit Address 3:0> = 0111 or red to SSPADD d to detect I ² C	1111): <0> to detect l ² address match	² C address ma	tch

I²C Slave mode, 7-bit address, the bit is ignored

'0' = Bit is cleared

REGISTER 30-6: SSP1ADD: MSSP ADDRESS AND BAUD RATE REGISTER (I²C MODE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
			ADD	<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown -			-n/n = Value at POR and BOR/Value at all other Resets					

Master mode:

1' = Bit is set

bit 7-0 ADD<7:0>: Baud Rate Clock Divider bits SCL pin clock period = ((ADD<7:0> + 1) *4)/Fosc

<u>10-Bit Slave mode – Most Significant Address Byte:</u>

- bit 7-3 **Not used:** Unused for Most Significant Address Byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by I²C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.
- bit 2-1 ADD<2:1>: Two Most Significant bits of 10-bit address
- bit 0 Not used: Unused in this mode. Bit state is a "don't care".

10-Bit Slave mode – Least Significant Address Byte:

bit 7-0 ADD<7:0>: Eight Least Significant bits of 10-bit address

7-Bit Slave mode:

bit 0 Not used: Unused in this mode. Bit state is a "don't care".





TABLE 34-10. CERCUT AND 1/0 THVIING FARAIVIETERS	TABLE 34-10:	CLKOUT	AND I/O	TIMING	PARAMETERS
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Stanuar		conditions (unless otherwise stated)					
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
OS11	TosH2ckL	Fosc↑ to CLKOUT↓ ⁽¹⁾	—	—	70	ns	$3.3V \leq V\text{DD} \leq 5.0V$
OS12	TosH2ckH	Fosc↑ to CLKOUT↑ ⁽¹⁾	_	_	72	ns	$3.3V \leq V\text{DD} \leq 5.0V$
OS13	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT ⁽¹⁾	Tosc + 200 ns	_	_	ns	
OS15	TosH2ioV	Fosc↑ (Q1 cycle) to Port out valid	—	50	70*	ns	$3.3V \le V\text{DD} \le 5.0V$
OS16	TosH2iol	Fosc↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	$3.3V \le V\text{DD} \le 5.0V$
OS17	TioV2osH	Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18*	TioR	Port output rise time ⁽²⁾		40 15	72 32	ns	$\begin{array}{l} VDD = 1.8V \\ 3.3V \leq VDD \leq 5.0V \end{array}$
OS19*	TioF	Port output fall time ⁽²⁾	_	28 15	55 30	ns	$\begin{array}{l} VDD \mbox{ = } 1.8V \\ 3.3V \leq VDD \leq 5.0V \end{array}$
OS20*	Tinp	INT pin input high or low time	25			ns	
OS21*	Tioc	Interrupt-on-change new input level time	25		—	ns	

Standard Operating Conditions	(unless otherwise	stated)
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* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in EXTRC mode where CLKOUT output is 4 x Tosc.

2: Slew rate limited.

FIGURE 34-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 35-103: Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 5.5V, Typical Measured Values, PIC16F1713/6 Only.



FIGURE 35-105: Comparator Offset, NP Mode (CxSP = 1), VDD = 5.5V, Typical Measured Values From -40°C to 125°C, PIC16F1713/6 Only.



FIGURE 35-107: Comparator Response Time Over Voltage, NP Mode (CxSP = 1), Typical Measured Values, PIC16F1713/6 Only.



FIGURE 35-104: Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values at 25°C, PIC16F1713/6 Only.



FIGURE 35-106: Comparator Response Time Over Voltage, NP Mode (CxSP = 1), Typical Measured Values, PIC16LF1713/6 Only.



FIGURE 35-108: Comparator Output Filter Delay Time Over Temp., NP Mode (CxSP = 1), Typical Measured Values, PIC16LF1713/6 Only.

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