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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1716-i-ss

PIC16(L)F1713/6

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3.7.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

FIGURE 3-10: TRADITIONAL DATA MEMORY MAP

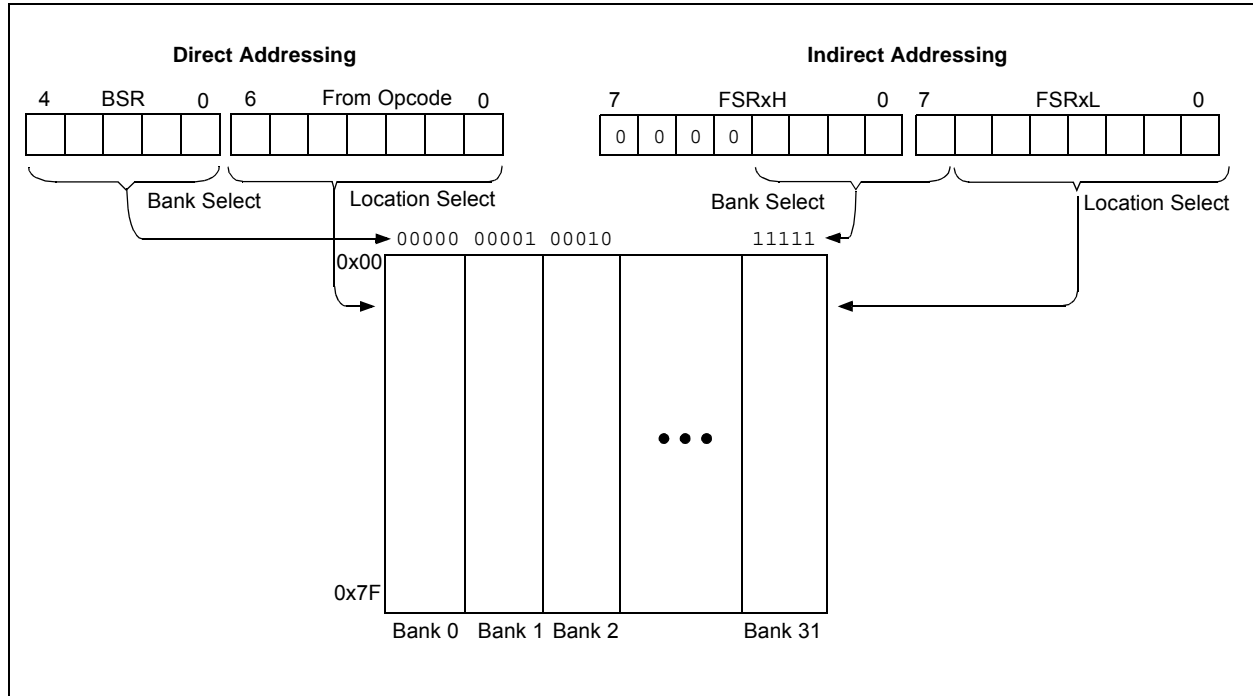
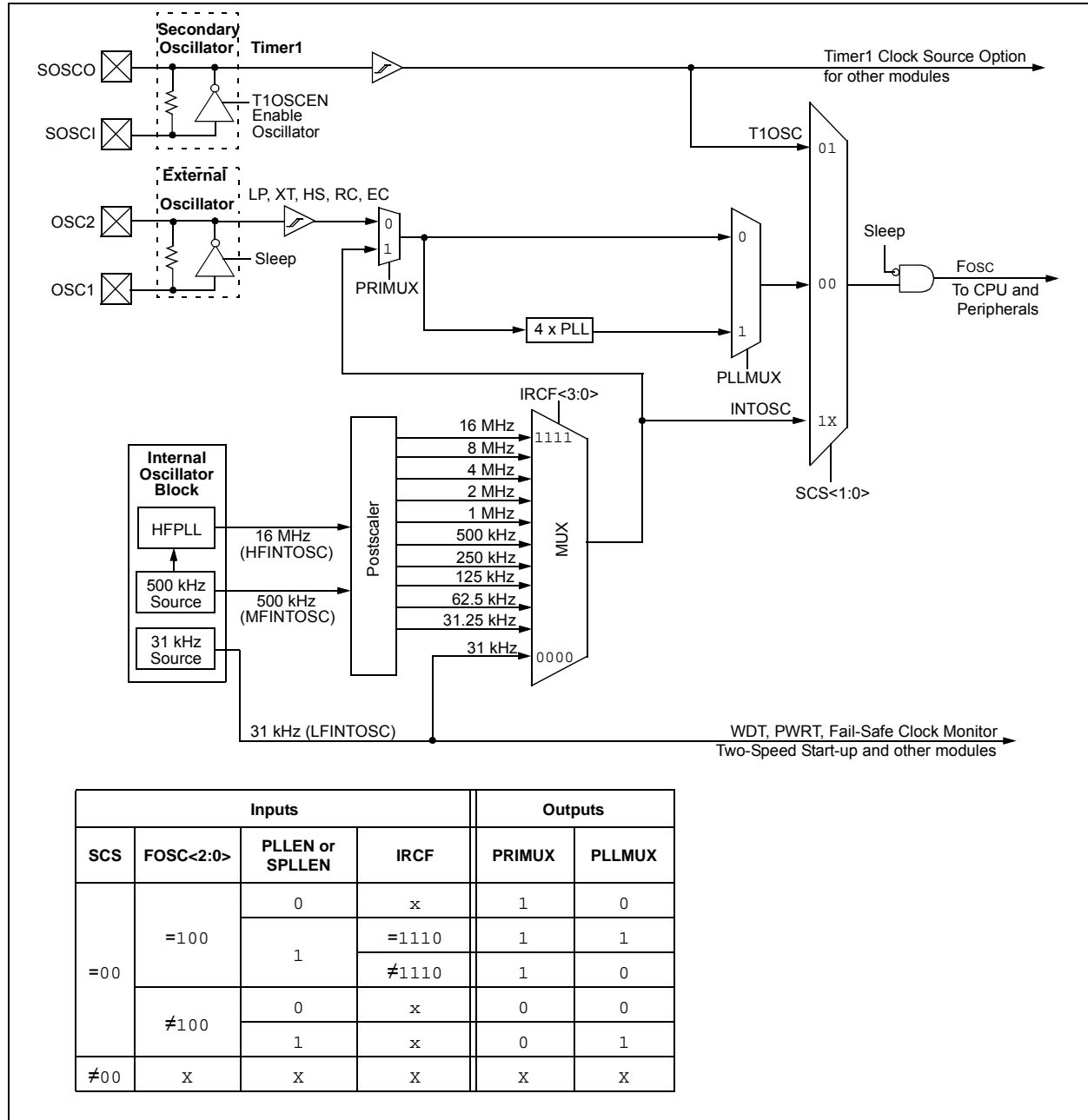


TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	54
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	58
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	19
WDTCON	—	—	WDTPS<4:0>					SWDTEN	98

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

FIGURE 6-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



PIC16(L)F1713/6

REGISTER 6-2: OSCSTAT: OSCILLATOR STATUS REGISTER

R-1/q	R-0/q	R-q/q	R-0/q	R-0/q	R-q/q	R-0/0	R-0/q
SOSCR	PLL R	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Conditional

bit 7 **SOSCR**: Secondary Oscillator Ready bit

If **T1OSCEN** = 1:

1 = Secondary oscillator is ready

0 = Secondary oscillator is not ready

If **T1OSCEN** = 0:

1 = Secondary clock source is always ready

bit 6 **PLL R**: 4x PLL Ready bit

1 = 4x PLL is ready

0 = 4x PLL is not ready

bit 5 **OSTS**: Oscillator Start-up Timer Status bit

1 = Running from the clock defined by the **FOSC<2:0>** bits of the Configuration Words

0 = Running from an internal oscillator (**FOSC<2:0>** = 100)

bit 4 **HFIOFR**: High-Frequency Internal Oscillator Ready bit

1 = HFINTOSC is ready

0 = HFINTOSC is not ready

bit 3 **HFIOFL**: High-Frequency Internal Oscillator Locked bit

1 = HFINTOSC is at least 2% accurate

0 = HFINTOSC is not 2% accurate

bit 2 **MFIOFR**: Medium Frequency Internal Oscillator Ready bit

1 = MFINTOSC is ready

0 = MFINTOSC is not ready

bit 1 **LFIOFR**: Low-Frequency Internal Oscillator Ready bit

1 = LFINTOSC is ready

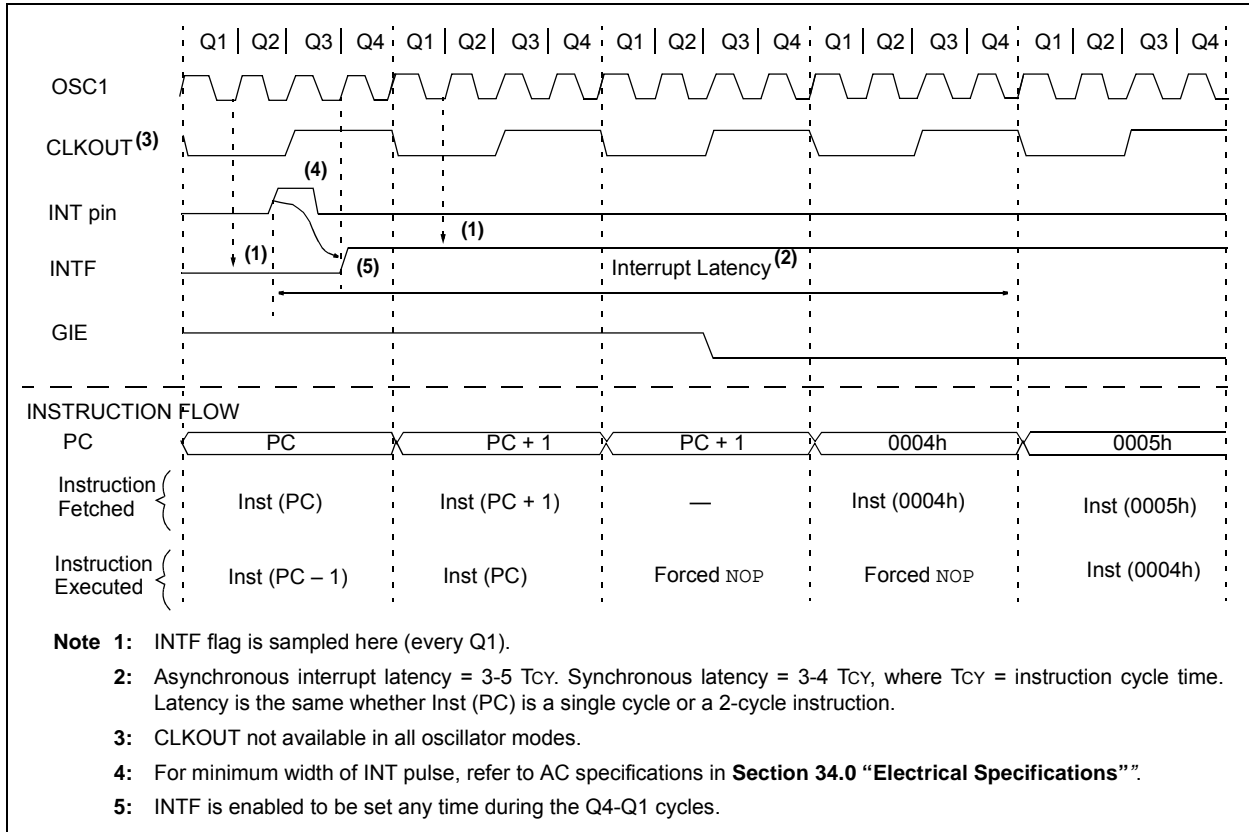
0 = LFINTOSC is not ready

bit 0 **HFIOFS**: High-Frequency Internal Oscillator Stable bit

1 = HFINTOSC is at least 0.5% accurate

0 = HFINTOSC is not 0.5% accurate

FIGURE 7-3: INT PIN INTERRUPT TIMING



REGISTER 10-6: PMCON2: PROGRAM MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
Program Memory Control Register 2							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

Flash Memory Unlock Pattern bits

To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the PMCON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes.

TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	83
PMCON1	— ⁽¹⁾	CFGFS	LWLO	FREE	WRERR	WREN	WR	RD	114
PMCON2	Program Memory Control Register 2								115
PMADRL	PMADRL<7:0>								113
PMADRH	— ⁽¹⁾	PMADRH<6:0>							113
PMDATL	PMDATL<7:0>								113
PMDATH	—	—	PMDATH<5:0>						113

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.

Note 1: Unimplemented, read as '1'.

TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	—	—	CLKOUTEN	BOREN<1:0>		—	47
	7:0	CP	MCLRE	PWRT $\overline{\text{E}}$	WDTE<1:0>		—	FOSC<1:0>		
CONFIG2	13:8	—	—	LVP	DEBUG	LPBOR	BORV	STVREN	PLLEN	49
	7:0	ZCDDIS	—	—	—	—	PPS1WAY	WRT<1:0>		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.

13.0 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-on-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

13.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

13.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

13.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCxF bits.

13.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 13-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW    0xff
XORWF    IOCAF, W
ANDWF    IOCAF, F
```

13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.

14.3 Register Definitions: FVR Control

REGISTER 14-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0		R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY ⁽¹⁾	TSEN ⁽³⁾	TSRNG ⁽³⁾	CDAFVR<1:0>		ADFVR<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	FVREN: Fixed Voltage Reference Enable bit 1 = Fixed Voltage Reference is enabled 0 = Fixed Voltage Reference is disabled
bit 6	FVRRDY: Fixed Voltage Reference Ready Flag bit ⁽¹⁾ 1 = Fixed Voltage Reference output is ready for use 0 = Fixed Voltage Reference output is not ready or not enabled
bit 5	TSEN: Temperature Indicator Enable bit ⁽³⁾ 1 = Temperature Indicator is enabled 0 = Temperature Indicator is disabled
bit 4	TSRNG: Temperature Indicator Range Selection bit ⁽³⁾ 1 = $V_{OUT} = V_{DD} - 4V_T$ (High Range) 0 = $V_{OUT} = V_{DD} - 2V_T$ (Low Range)
bit 3-2	CDAFVR<1:0>: Comparator FVR Buffer Gain Selection bits 11 = Comparator FVR Buffer Gain is 4x, with output $V_{CDAFVR} = 4x V_{FVR}$ ⁽²⁾ 10 = Comparator FVR Buffer Gain is 2x, with output $V_{CDAFVR} = 2x V_{FVR}$ ⁽²⁾ 01 = Comparator FVR Buffer Gain is 1x, with output $V_{CDAFVR} = 1x V_{FVR}$ 00 = Comparator FVR Buffer is off
bit 1-0	ADFVR<1:0>: ADC FVR Buffer Gain Selection bit 11 = ADC FVR Buffer Gain is 4x, with output $V_{ADFVR} = 4x V_{FVR}$ ⁽²⁾ 10 = ADC FVR Buffer Gain is 2x, with output $V_{ADFVR} = 2x V_{FVR}$ ⁽²⁾ 01 = ADC FVR Buffer Gain is 1x, with output $V_{ADFVR} = 1x V_{FVR}$ 00 = ADC FVR Buffer is off

- Note 1:** FVRRDY is always '1' on PIC16(L)F1713/6 only.
Note 2: Fixed Voltage Reference output cannot exceed V_{DD} .
Note 3: See **Section 15.0 "Temperature Indicator Module"** for additional information.

TABLE 14-2: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		151

Legend: Shaded cells are not used with the Fixed Voltage Reference.

17.1 PWMx Pin Configuration

All PWM outputs are multiplexed with the PORT data latch. The user must configure the pins as outputs by clearing the associated TRIS bits.

17.1.1 FUNDAMENTAL OPERATION

The PWM module produces a 10-bit resolution output. Timer2 and PR2 set the period of the PWM. The PWMxDCL and PWMxDCH registers configure the duty cycle. The period is common to all PWM modules, whereas the duty cycle is independently controlled.

Note: The Timer2 postscaler is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

All PWM outputs associated with Timer2 are set when TMR2 is cleared. Each PWMx is cleared when TMR2 is equal to the value specified in the corresponding PWMxDCH (8 MSb) and PWMxDCL<7:6> (2 LSb) registers. When the value is greater than or equal to PR2, the PWM output is never cleared (100% duty cycle).

Note: The PWMxDCH and PWMxDCL registers are double buffered. The buffers are updated when Timer2 matches PR2. Care should be taken to update both registers before the timer match occurs.

17.1.2 PWM OUTPUT POLARITY

The output polarity is inverted by setting the PWMxPOL bit of the PWMxCON register.

17.1.3 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 17-1.

EQUATION 17-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

Note: $TOSC = 1/FOSC$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWM output is active. (Exception: When the PWM duty cycle = 0%, the PWM output will remain inactive.)
- The PWMxDCH and PWMxDCL register values are latched into the buffers.

Note: The Timer2 postscaler has no effect on the PWM operation.

17.1.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDCH and PWMxDCL register pair. The PWMxDCH register contains the eight MSbs and the PWMxDCL<7:6>, the two LSbs. The PWMxDCH and PWMxDCL registers can be written to at any time.

Equation 17-2 is used to calculate the PWM pulse width.

Equation 17-3 is used to calculate the PWM duty cycle ratio.

EQUATION 17-2: PULSE WIDTH

$$Pulse\ Width = (PWMxDCH:PWMxDCL<7:6>) \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

Note: $TOSC = 1/FOSC$

EQUATION 17-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(PWMxDCH:PWMxDCL<7:6>)}{4(PR2 + 1)}$$

The 8-bit timer TMR2 register is concatenated with the two Least Significant bits of $1/FOSC$, adjusted by the Timer2 prescaler to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

17.1.9 SETUP FOR PWM OPERATION USING PWMx PINS

The following steps should be taken when configuring the module for PWM operation using the PWMx pins:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the PR2 register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
 - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin and wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
7. Enable the PWMx pin output driver(s) by clearing the associated TRIS bit(s) and setting the desired pin PPS control bits.
8. Configure the PWM module by loading the PWMxCON register with the appropriate values.

Note 1: In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then move Step 8 to replace Step 4.

2: For operation with other peripherals only, disable PWMx pin outputs.

17.1.10 SETUP FOR PWM OPERATION TO OTHER DEVICE PERIPHERALS

The following steps should be taken when configuring the module for PWM operation to be used by other device peripherals:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the PR2 register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
 - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
 - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
7. Configure the PWM module by loading the PWMxCON register with the appropriate values.

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

18.0 COMPLEMENTARY OUTPUT GENERATOR (COG) MODULE

The primary purpose of the Complementary Output Generator (COG) is to convert a single output PWM signal into a two output complementary PWM signal. The COG can also convert two separate input events into a single or complementary PWM output.

The COG PWM frequency and duty cycle are determined by a rising event input and a falling event input. The rising event and falling event may be the same source. Sources may be synchronous or asynchronous to the COG_clock.

The rate at which the rising event occurs determines the PWM frequency. The time from the rising event input to the falling event input determines the duty cycle.

A selectable clock input is used to generate the phase delay, blanking, and dead-band times. Dead-band time can also be generated with a programmable time delay, which is independent from all clock sources.

Simplified block diagrams of the various COG modes are shown in Figure 18-2 through Figure 18-6.

The COG module has the following features:

- Six modes of operation:
 - Steered PWM mode
 - Synchronous Steered PWM mode
 - Forward Full-Bridge mode
 - Reverse Full-Bridge mode
 - Half-Bridge mode
 - Push-Pull mode
- Selectable COG_clock clock source
- Independently selectable rising event sources
- Independently selectable falling event sources
- Independently selectable edge or level event sensitivity
- Independent output polarity selection
- Phase delay with independent rising and falling delay times
- Dead-band control with:
 - independent rising and falling event dead-band times
 - Synchronous and asynchronous timing
- Blanking control with independent rising and falling event blanking times
- Auto-shutdown control with:
 - Independently selectable shutdown sources
 - Auto-restart enable
 - Auto-shutdown pin override control (high, low, off, and Hi-Z)

18.1 Fundamental Operation

18.1.1 STEERED PWM MODES

In steered PWM mode, the PWM signal derived from the input event sources is output as a single phase PWM which can be steered to any combination of the four COG outputs. Outputs are selected by setting the GxSTRA through GxSTRD bits of the COGxSTR register (Register 18-9). When the steering bits are cleared, then the output data is the static level determined by the GxSDATA through GxSDATD bits of the COGxSTR register. Output steering takes effect on the instruction cycle following the write to the COGxSTR register.

Synchronous steered PWM mode is identical to the steered PWM mode except that changes to the output steering take effect on the first rising event after the COGxSTR register write. Static output data is not synchronized.

Steering mode configurations are shown in Figure 18-2 and Figure 18-3.

Steered PWM and synchronous steered PWM modes are selected by setting the GxMD bits of the COGxCON0 register (Register 18-1) to '000' and '001' respectively.

18.1.2 FULL-BRIDGE MODES

In both Forward and Reverse Full-Bridge modes, two of the four COG outputs are active and the other two are inactive. Of the two active outputs, one is modulated by the PWM input signal and the other is on at 100% duty cycle. When the direction is changed, the dead-band time is inserted to delay the modulated output. This gives the unmodulated driver time to shut down, thereby, preventing shoot-through current in the series connected power devices.

In Forward Full-Bridge mode, the PWM input modulates the COGxD output and drives the COGA output at 100%.

In Reverse Full-Bridge mode, the PWM input modulates the COGxB output and drives the COGxC output at 100%.

The full-bridge configuration is shown in Figure 18-4. Typical full-bridge waveforms are shown in Figure 18-12 and Figure 18-13.

Full-Bridge Forward and Full-Bridge Reverse modes are selected by setting the GxMD bits of the COGxCON0 register to '010' and '011', respectively.

FIGURE 21-4: ANALOG INPUT MODEL

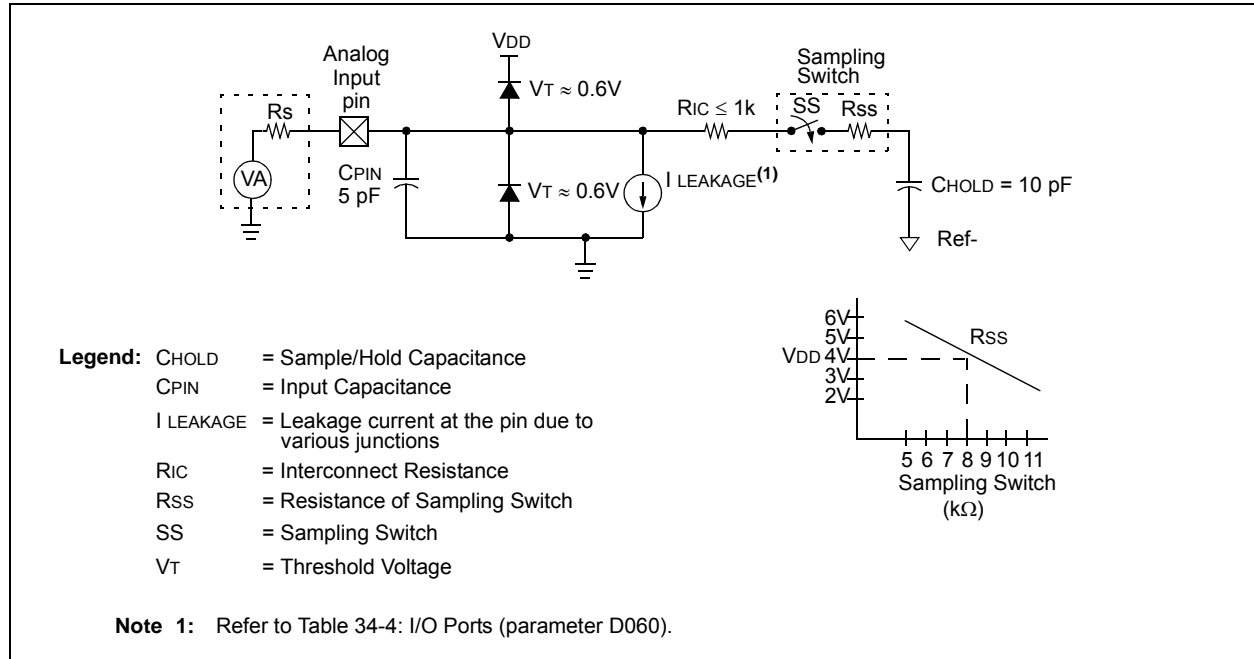
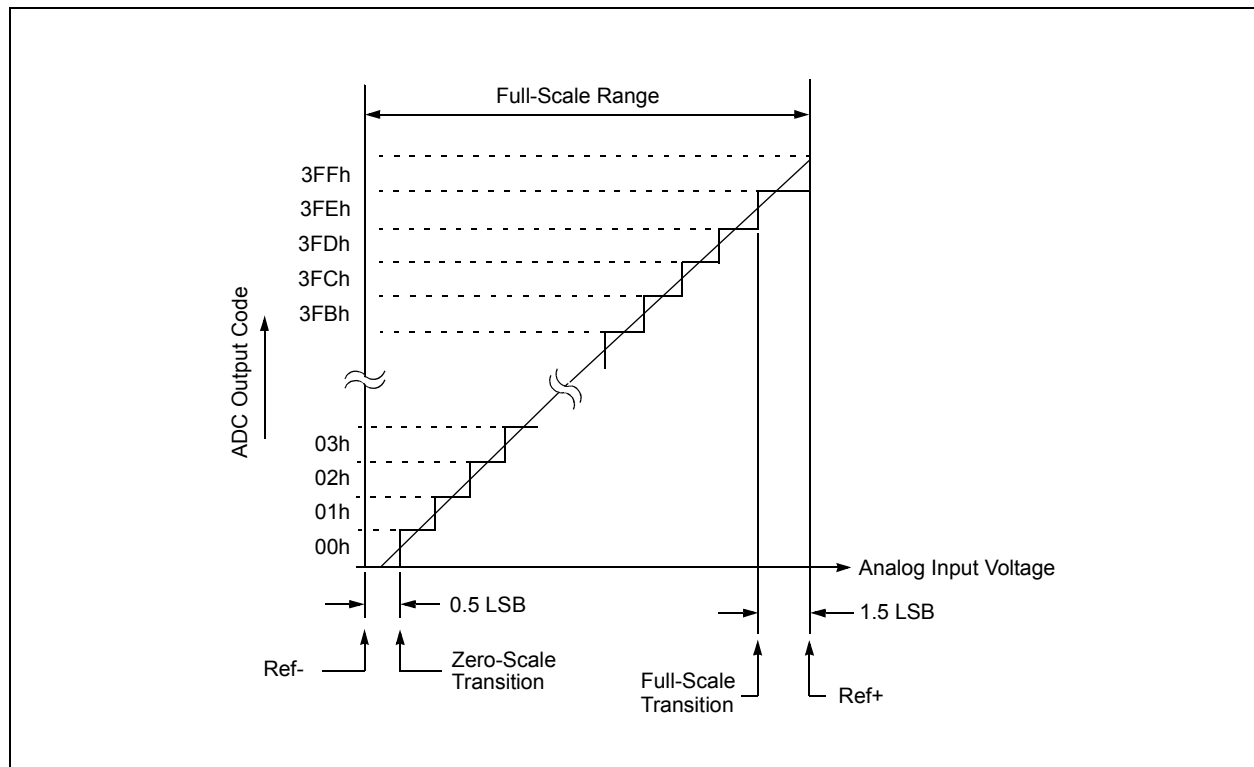


FIGURE 21-5: ADC TRANSFER FUNCTION



29.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains two standard Capture/Compare/PWM modules (CCP1 and CCP2).

The Capture and Compare functions are identical for all CCP modules.

Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.

2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

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29.1 Capture Mode

The Capture mode function described in this section is available and identical for all CCP modules.

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCPx pin, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

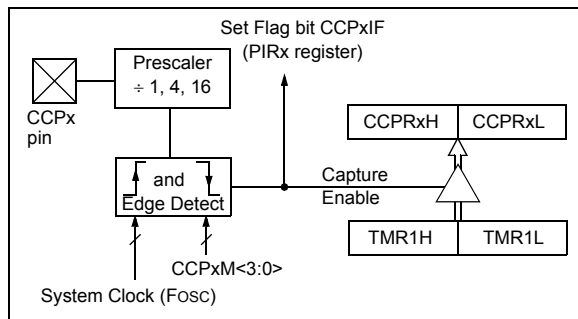
Figure 29-1 shows a simplified diagram of the capture operation.

29.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 29-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



29.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See **Section 26.0 “Timer1 Module with Gate Control”** for more information on configuring Timer1.

29.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIRx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

29.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. Example 29-1 demonstrates the code to perform this function.

EXAMPLE 29-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCPxCON    ;Set Bank bits to point
                    ;to CCPxCON
CLRWF  CCPxCON      ;Turn CCP module off
MOVLW  NEW_CAPT_PS  ;Load the W reg with
                    ;the new prescaler
                    ;move value and CCP ON
MOVWF  CCPxCON      ;Load CCPxCON with this
                    ;value
```


FIGURE 30-3: MSSP BLOCK DIAGRAM (I²C SLAVE MODE)

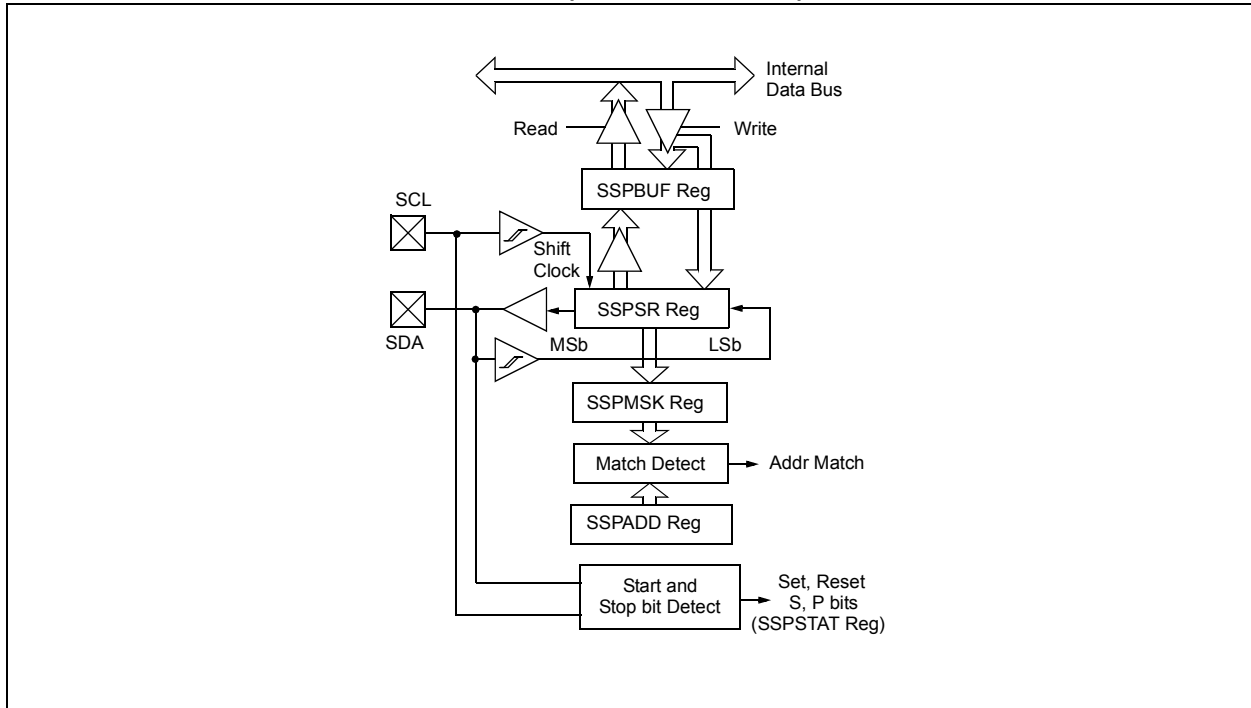
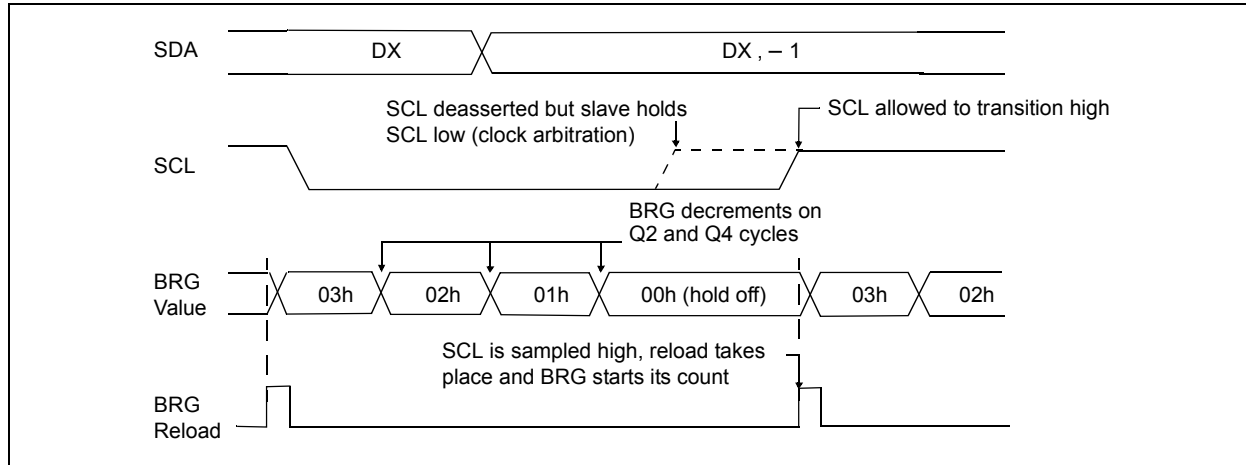


FIGURE 30-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



30.6.3 WCOL STATUS FLAG

If the user writes the SSPBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPBUF was attempted while the module was not idle.

Note: Because queuing of events is not allowed, writing to the lower five bits of SSPCON2 is disabled until the Start condition is complete.

Start condition and causes the S bit of the SSPSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPCON2 register will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

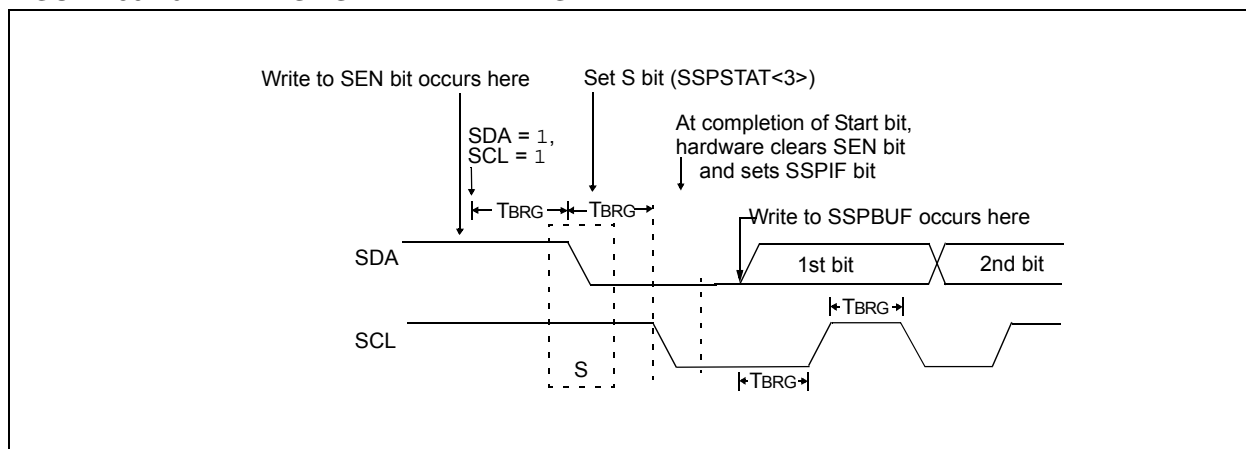
Note 1: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.

2: The Philips I²C specification states that a bus collision cannot occur on a Start.

30.6.4 I²C MASTER MODE START CONDITION TIMING

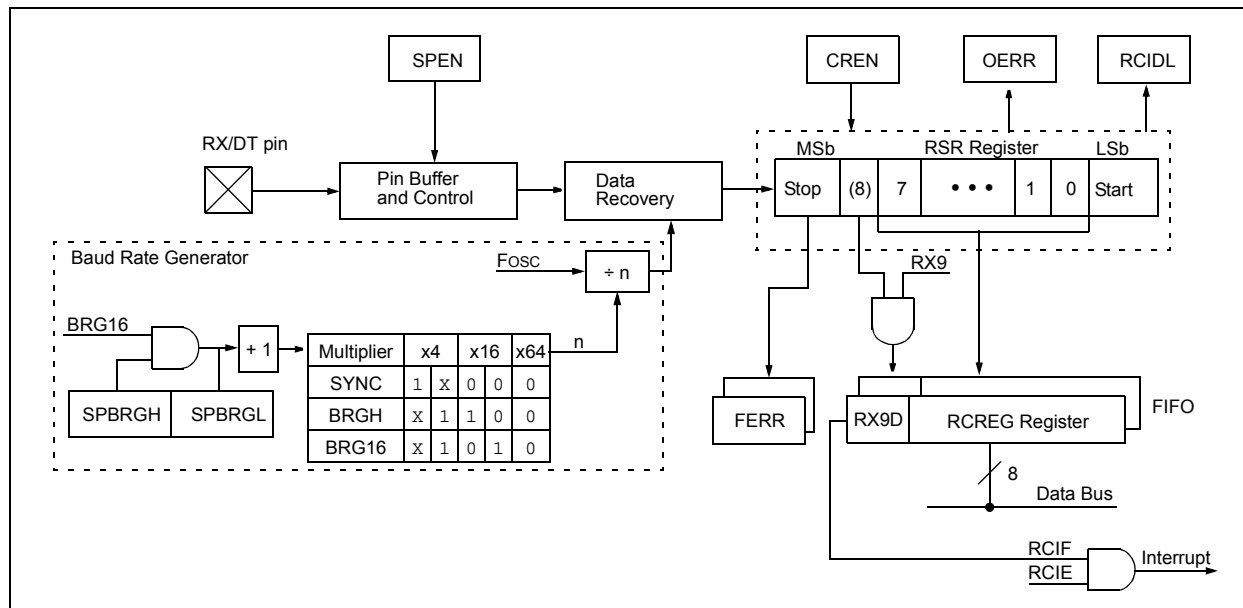
To initiate a Start condition (Figure 30-26), the user sets the Start Enable bit, SEN bit of the SSPCON2 register. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the

FIGURE 30-26: FIRST START BIT TIMING



PIC16(L)F1713/6

FIGURE 31-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 31-1, Register 31-2 and Register 31-3, respectively.

The RX and CK input pins are selected with the RXPPS and CKPPS registers, respectively. TX, CK, and DT output pins are selected with each pin's RxyPPS register. Since the RX input is coupled with the DT output in Synchronous mode, it is the user's responsibility to select the same pin for both of these functions when operating in Synchronous mode. The EUSART control logic will control the data direction drivers automatically.

FIGURE 31-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)

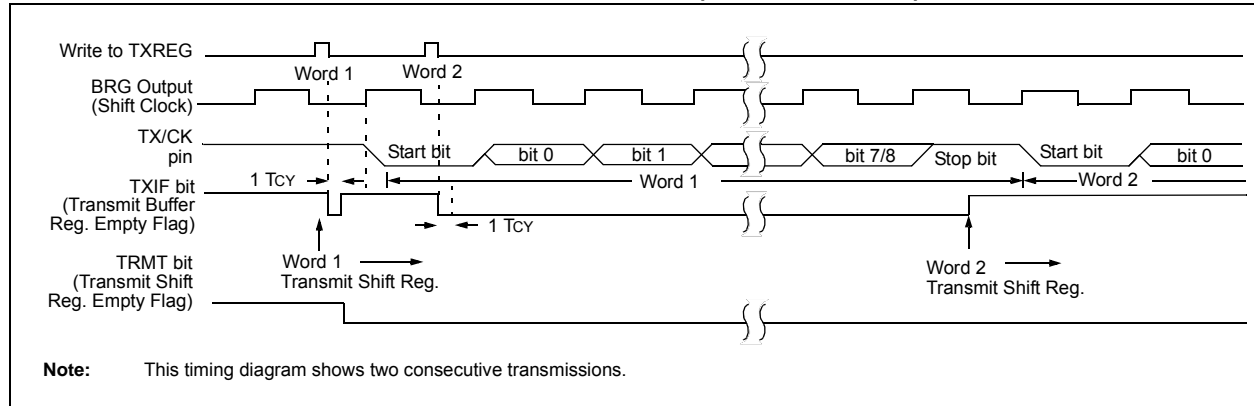


TABLE 31-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

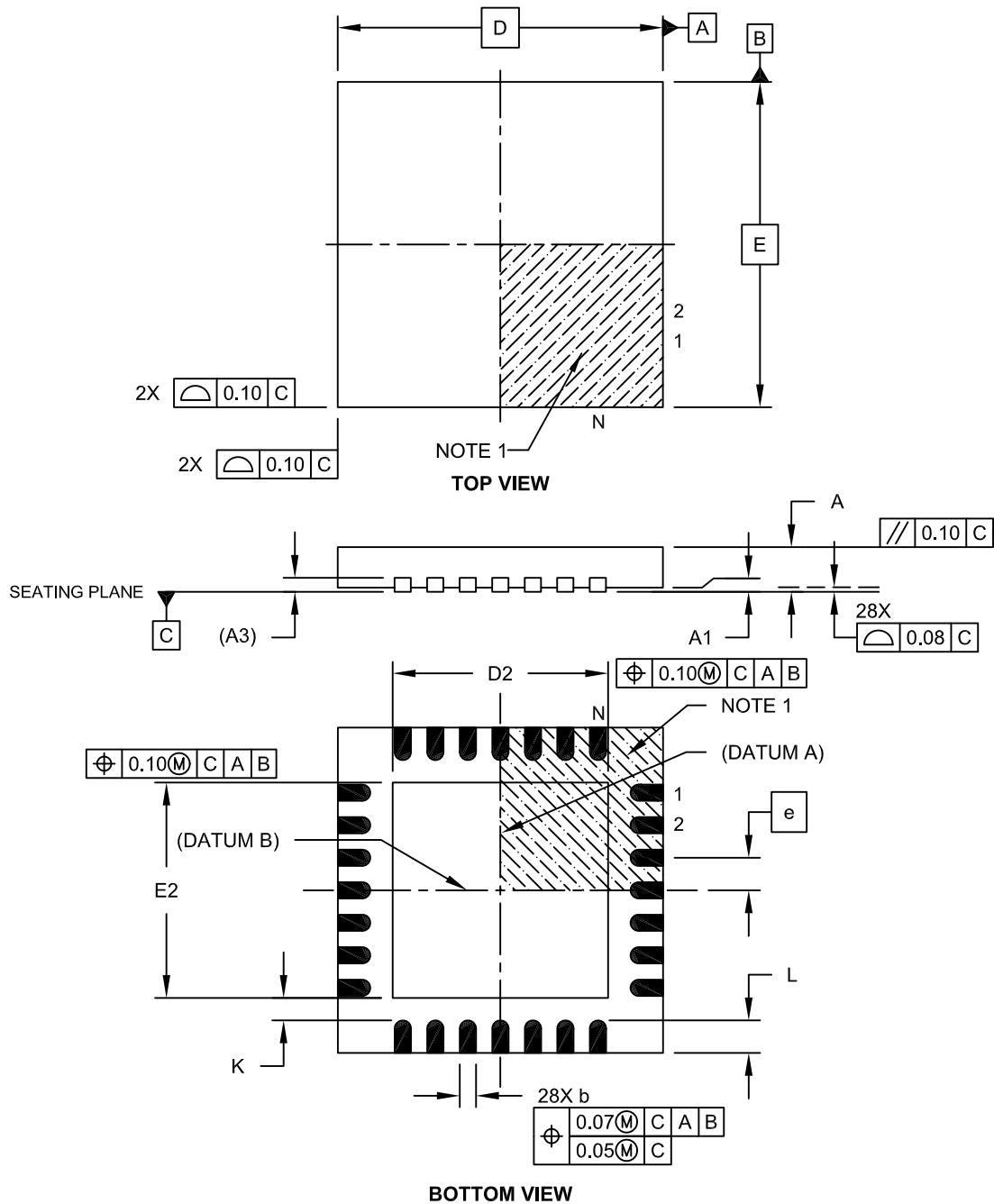
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	349
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	83
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	84
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	87
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	348
RxyPPS	—	—	—	RxyPPS<4:0>					137
SP1BRGL	SP1BRG<7:0>								350*
SP1BRGH	SP1BRG<15:8>								350*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	125
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	130
TX1REG	EUSART Transmit Data Register								339*
TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	347

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous transmission.

* Page provides register information.

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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