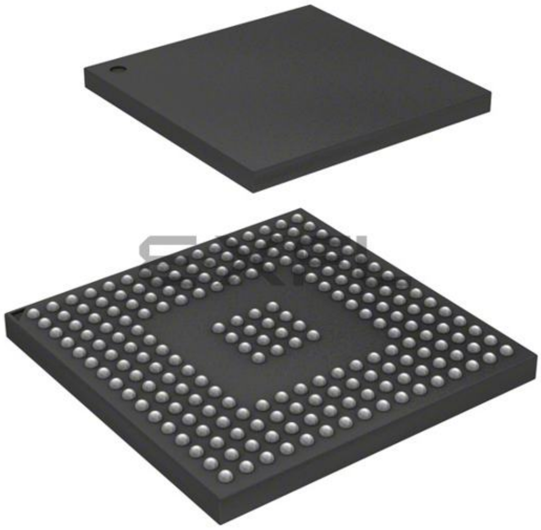

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z1
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	144
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5517gavmg80

Table of Contents

List of Tables

List of Figures

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PD6	54	PD6 TXD_A eMIOS14	GPIO SCI_A Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	98	122	F14
PD7	55	PD7 RXD_A eMIOS15	GPIO SCI_A Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	97	121	F15
PD8	56	PD8 TXD_B SCL_A	GPIO SCI_B Transmit I^2C Serial Clock Line	I/O O I/O	V_{DDE1}	SH	—	—	94	118	G13
PD9	57	PD9 RXD_B SDA_A	GPIO SCI_B Receive I^2C Serial Data Line	I/O I I/O	V_{DDE1}	SH	—	—	93	117	F16
PD10	58	PD10 PCS_B2 CNTX_F NMI0	GPIO DSPI_B Peripheral Chip Select CAN_F Transmit NMI Input for Z1 Core	I/O O O I	V_{DDE1}	SH	—	—	92	116	G14
PD11	59	PD11 PCS_B1 CNRX_F NMI1	GPIO DSPI_B Peripheral Chip Select CAN_F Receive NMI Input for Z0 Core	I/O O I I	V_{DDE1}	SH	—	—	91	115	G15
PD12	60	PD12 PCS_B0 eMIOS9	GPIO DSPI_B Peripheral Chip Select eMIOS Channel	I/O I/O O	V_{DDE1}	SH	—	—	90	114	H14
PD13	61	PD13 SCK_B eMIOS8	GPIO DSPI_B Clock eMIOS Channel	I/O I/O O	V_{DDE1}	SH	—	—	89	113	H15
PD14	62	PD14 SOUT_B eMIOS7	GPIO DSPI_B Data Output eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	88	110	J14
PD15	63	PD15 SIN_B eMIOS6	GPIO DSPI_B Data Input eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	87	107	K14
Port E (16)											
PE0	64	PE0 PCS_A2 eMIOS5 MLBCLK	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Clock	I/O O O I	V_{DDE1}	SH	—	—	86	106	K16
PE1	65	PE1 PCS_A1 eMIOS4 MLBSI / MLBSIG	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Signal In (5-pin) / MLB Bi-directional Signal (3-pin)	I/O O O I I/O	V_{DDE1}	MH	—	—	85	103	L14
PE2	66	PE2 PCS_A0 eMIOS3 MLBDI / MLBDAT	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Data In (5-pin) / MLB Bi-directional Data (3-pin)	I/O I/O O I I/O	V_{DDE1}	MH	—	—	84	101	L15

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PE3	67	PE3 SCK_A eMIOS2 MLBSO / MLBSIG_BUFEN	GPIO DSPI_A Clock eMIOS Channel MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin)	I/O I/O O O O	V_{DDE1}	MH	—	—	83	100	M13
PE4	68	PE4 SOUT_A eMIOS1 MLBDO / MLBDAT_BUFEN	GPIO DSPI_A Data Out eMIOS Channel MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin)	I/O O O O O	V_{DDE1}	MH	—	—	82	98	N14
PE5	69	PE5 SIN_A eMIOS0 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS	GPIO DSPI_A Data In eMIOS Channel MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data	I/O I O O O O	V_{DDE1}	MH	—	—	81	97	M15
PE6	70	PE6 CLKOUT	GPIO System Clock Output	I/O O	V_{DDE3}	MH	—	—	67	83	P13
PE7	71	PE7	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H13
PE8	72	PE8	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H16
PE9	72	PE9	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	J13
PE10	74	PE10	GPIO	I/O	V_{DDE1}	SH	—	—	—	112	J16
PE11	75	PE11	GPIO	I/O	V_{DDE1}	SH	—	—	—	111	J15
PE12	76	PE12	GPIO	I/O	V_{DDE1}	SH	—	—	—	109	K13
PE13	77	PE13	GPIO	I/O	V_{DDE1}	SH	—	—	—	108	L13
PE14	78	PE14	GPIO	I/O	V_{DDE1}	SH	—	—	—	102	L16
PE15	79	PE15	GPIO	I/O	V_{DDE1}	SH	—	—	—	99	M14
Port F (16)											
PF0	80	PF0 RD_$\overline{WR}$ EVTI[8]	GPIO EBI Read/Write Nexus Event In	I/O I/O I	V_{DDE3}	MH	—	—	66	82	N12
PF1	81	PF1 $\overline{TA}$ MLBCLK EVTO[8]	GPIO EBI Transfer Acknowledge MLB Clock Nexus Event Out	I/O I/O I O	V_{DDE3}	MH	—	—	65	81	P12
PF2	82	PF2 AD8 ADDR8 MLBSI / MLBSIG $\overline{MSEO}$[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal In (5-pin) / MLB Bi-Directional Signal (3-pin) Nexus Message Start/End Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	64	80	R12

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{\text{CS1}}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{\text{CS0}}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{\text{TS}}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF13	93	PF13 $\overline{\text{OE}}$ RXD_D	GPIO EBI Output Enable SCI_D Receive	I/O O I	V_{DDE2}	MH	—	—	49	59	R6
PF14	94	PF14 $\overline{\text{WE0}}$ $\overline{\text{BDIP}}$ CNTX_D	GPIO EBI Write Enable EBI Burst Data In Progress CAN_D Transmit	I/O O O O	V_{DDE2}	MH	—	—	45	55	P6
PF15	95	PF15 $\overline{\text{WE1}}$ $\overline{\text{TEA}}$ CNRX_D	GPIO EBI Write Enable EBI Transfer Error Acknowledge CAN_D Receive	I/O O I/O I	V_{DDE2}	MH	—	—	44	54	N6
Port G (16)											
PG0	96	PG0 AD16 eMIOS16	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	43	51	P5
PG1	97	PG1 AD17 eMIOS17 SIN_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial In	I/O I/O I/O I	V_{DDE2}	MH	—	—	42	50	T4
PG2	98	PG2 AD18 eMIOS18 SOUT_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Out	I/O I/O I/O O	V_{DDE2}	MH	—	—	41	49	R4
PG3	99	PG3 AD19 eMIOS19 SCK_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Clock	I/O I/O I/O I/O	V_{DDE2}	MH	—	—	40	48	P4
PG4	100	PG4 AD20 eMIOS20 PCS_C0	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Peripheral Chip Select	I/O I/O I/O I/O	V_{DDE2}	MH	—	—	39	47	T3
PG5	101	PG5 AD21 eMIOS21	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	38	46	R3
PG6	102	PG6 AD22 eMIOS22	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	37	45	T2
PG7	103	PG7 AD23 eMIOS23 RXD_C	GPIO EBI Muxed Address/Data eMIOS Channel SCI_C Receive	I/O I/O I/O I	V_{DDE2}	MH	—	—	36	44	R1
PG8	104	PG8 AD24 PCS_A4	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	35	43	P2

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V_{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V_{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V_{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V_{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V_{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input[7] eMIOS Channel I^{2}C_A Serial Clock	I/O I O I/O	V_{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input[7] eMIOS Channel I^{2}C_A Serial Data	I/O I O I/O	V_{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 $\overline{CS3}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 $\overline{CS2}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input[7] SCI_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input[7] SCI_E Receive eQADC External Mux Address	I/O I I O	V_{DDE2}	A + SH	—	—	19	24	J3

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PH6	118	PH6 AN21 TXD_F	GPIO eQADC Analog Input[7] SCI_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	18	23	J2
PH7	119	PH7 AN20 RXD_F	GPIO eQADC Analog Input[7] SCI_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	17	22	J1
PH8	120	PH8 AN19 CNTX_E MA0	GPIO eQADC Analog Input[7] CAN_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	14	17	H1
PH9	121	PH9 AN18/ANT CNRX_E	GPIO eQADC Analog Input[7] CAN_E Receive	I/O I I	V_{DDE2}	A + SH	—	—	13	14	G2
PH10	122	PH10 AN17/ANS CNRX_F	GPIO eQADC Analog Input[7] CAN_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	12	12	F4
PH11	123	PH11 AN16/ANR CNTX_F	GPIO eQADC Analog Input[7] CAN_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	11	11	F3
PH12	124	PH12 PCS_D5	GPIO DSPI_D Peripheral Chip Select	I/O O	V_{DDE2}	SH	—	—	—	—	F2
PH13	125	PH13	GPIO	I/O	V_{DDE2}	SH	—	—	—	—	F1
PH14	126	PH14 $\overline{WE2}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	53	T5
PH15	127	PH15 $\overline{WE3}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	52	R5
Port J (16)											
PJ0	128	PJ0 AD0	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N11
PJ1	129	PJ1 AD1	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	P11
PJ2	130	PJ2 AD2	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N10
PJ3	131	PJ3 AD3	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	R10
PJ4	132	PJ4 AD4	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	75	P10
PJ5	133	PJ5 AD5	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	73	T9
PJ6	134	PJ6 AD6	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	69	P9
PJ7	135	PJ7 AD7	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	67	R8

[3] V_{RL} is shorted to V_{SSA} in the 144LQFP and 176 LQFP packages.
[4] V_{PP} requires 5V for program/erase operations, but may be 0-5V otherwise. V_{PP} should not go high or low when the device is in Sleep mode.
[5] Voltage generated from internal voltage regulator and no external connection or load allowed except the required bypass capacitors.
[6] V_{FLASH} is shorted to V_{DD33} in the package.

1.5 Pinout – 208 PBGA

208 PBGA Ball Map
(as viewed from top through the package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{DD}	V_{DDA}	PA8	V_{SSA}	PA13	PK1	PB12	PB2	PB6	PB10	PB15	PC3	PC7	PC10	V_{DDE1}	V_{DD}	A
B	REF BYPC	V_{DD}	V_{RH}	V_{RL}	PA12	PK0	PB13	PB3	PB7	PB11	PC0	PC4	PC8	PC11	V_{DD}	PC12	B
C	PA7	PA6	V_{SS}	PA9	PA11	PA15	PB0	PB4	PB8	PB14	PC1	PC5	PC9	V_{SS}	PC13	PC14	C
D	PA5	PA4	PA3	V_{SS}	PA10	PA14	PB1	PB5	PB9	V_{DDE1}	PC2	PC6	V_{SS}	PC15	PD0	PD1	D
E	PA2	PA1	PA0	RESET									V_{DDE1}	PD2	PD3	PD4	E
F	PH13	PH12	PH11	PH10									PD5	PD6	PD7	PD9	F
G	PJ15	PH9	PJ14	PJ13			V_{SS}	V_{SS}	V_{SS}	V_{SS}			PD8	PD10	PD11	V_{DDE1}	G
H	PH8	PJ12	PJ11	V_{DDE2}			V_{SS}	V_{SS}	V_{SS}	V_{SS}			PE7	PD12	PD13	PE8	H
J	PH7	PH6	PH5	PJ10			V_{SS}	V_{SS}	V_{SS}	V_{SS}			PE9	PD14	PE11	PE10	J
K	PJ9	PJ8	PH4	PH3			V_{SS}	V_{SS}	V_{SS}	V_{SS}			PE12	PD15	V_{DDE1}	PE0	K
L	PH2	PH1	PH0	V_{DDE2}									PE13	PE1	PE2	PE14	L
M	PG15	PG14	PG13	PG12									PE3	PE15	PE5	V_{SSSYN}	M
N	PG11	PG10	PG9	V_{SS}	V_{DDE2}	PF15	PF12	PF8	V_{DDE3}	PJ2	PJ0	PF0	V_{SS}	PE4	V_{DD33}	EXTAL	N
P	V_{DDE2}	PG8	V_{SS}	PG3	PG0	PF14	PF11	PF7	PJ6	PJ4	PJ1	PF1	PE6	V_{SS}	V_{PP}	XTAL	P
R	PG7	V_{DD}	PG5	PG2	PH15	PF13	PF10	PJ7	PF5	PJ3	TEST	PF2	TDI	TCK	V_{DD}	V_{DDSYN}	R
T	V_{DD}	PG6	PG4	PG1	PH14	V_{DDR}	PF9	PF6	PJ5	PF4	V_{DDE3}	PF3	JCOMP	TDO	TMS	V_{DD}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. MPC5510 Pinout – 208 PBGA

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \qquad \textit{Eqn. 5}$$

where:

$$T_J = \text{junction temperature } (^{o}C) \qquad \textit{Eqn. 6}$$

$$T_B = \text{board temperature at the package perimeter } (^{o}C/W) \qquad \textit{Eqn. 7}$$

$$R_{\theta JB} = \text{junction to board thermal resistance } (^{o}C/W) \text{ per JESD51-8} \qquad \textit{Eqn. 8}$$

$$P_D = \text{power dissipation in the package (W)} \qquad \textit{Eqn. 9}$$

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 10}$$

where:

$$R_{\theta JA} = \text{junction to ambient thermal resistance } (^{o}C/W) \qquad \textit{Eqn. 11}$$

$$R_{\theta JC} = \text{junction to case thermal resistance } (^{o}C/W) \qquad \textit{Eqn. 12}$$

$$R_{\theta CA} = \text{case to ambient thermal resistance } (^{o}C/W) \qquad \textit{Eqn. 13}$$

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

Table 6. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
21	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 100	100	mV
22	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} - V_{SSA}$	– 100	100	mV
23	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
24	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	– 100	100	mV
25	Slew rate on VDDA, VDDR, and VDDE power supply pins[9]	Vramp	1	100	V/ms
26	Capactive Supply Load VDD VDD33 VDDSYN	Vload	 800 200 200	 — —	nF

1 Please refer to Section 2.2.1, "General Notes for Specifications at Maximum Junction Temperature" for more details about the relation between ambient temperature T_A and device junction temperature T_J.

2 M parts can't go above 66 MHz.

3 V_{PP} can drop to 0 volts during read-only operations and before entry to Sleep mode, to reduce power consumption.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 If V_{DDE1} is below V_{DDA} than the analog input limits (spec #9 (Analog (AE/A) Input Voltage) in Table 6) will be based on the V_{DDE1} voltage level.

6 Absolute value of current, measured at V_{IL} and V_{IH}.

7 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH.

8 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: A and AE.

9 This applies to the ramp up rate from 0.3 volts to 3.0 volts.

2.5 Operating Current Specifications

Table 7. Operating Currents

Num	Characteristic	Symbol	Typ[1] 25C Ambient	Typ[1] 70C Ambient	Max[1] -40–145C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{PP} + I_{DDA} + I_{DDR}$					
	$I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3}$					
1	$V_{DDE(1,2,3)}$ Current	I_{DDE}				
	$V_{DDE(1,2,3)}$ @ 3.0V - 5.5V					
	Static[2], or when in SLEEP or STOP		1	3	30	µA
	Dynamic[3]		Note [3]	Note [3]	Note [3]	mA
2	V_{PP} Current	I_{PP}				
	V_{PP} @ 0V (All modes)		1	1	1	µA
	V_{PP} @ 5.25V					
	SLEEP mode		15	20	30	µA
	STOP mode		15	20	30	µA
	RUN mode		1	1	25	mA
3	V_{DDA} Current	I_{DDA}				
	V_{DDA} @ 4.5V - 5.25V					
	RUN mode[4]		5	5	10	mA
	SLEEP/STOP[5] mode with 32KIRC		12	16	26	µA
	SLEEP/STOP[5] mode with 32KOSC		12	16	28	µA
	SLEEP/STOP[5] mode with 16MIRC		111	165	225	µA
4	V_{DDR} Current	I_{DDR}				
	V_{DDR} @ 4.5V - 5.25V					
	SLEEP mode		20	25	360	µA
	with XOSC[6] (additonal)		500	600	900	µA
	with RTC/API (additonal)		1	1	3	µA
	each 8K RAM block (additional)		0.8	7	45	µA
	STOP mode		170	600	1500	µA
	with XOSC[6] (additonal)		500	600	900	µA
	RUN mode (Using 16 MHz IRC)		30	35	40	mA
	RUN mode (Maximum @ 48 MHz)[7]		50	75	90	mA
	RUN mode (Maximum @ 66 MHz)[8]		105	110	120	mA
	RUN mode (Maximum @ 80MHz)[9]		120	130	135	mA

1 Typ - Nominal voltage levels and functional activity. Max - Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 8 for more information.

4 RUN mode is a typical application with the ADC, 16MIRC, 32KIRC running.

5 SLEEP/STOP mode means that only the listed peripherals are on. All others are diabled.

6 XOSC: optionally enabled in SLEEP and STOP modes (oscillator remains running from crystal but XOSC clock output disabled).

7 RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripherals enabled, both cores running, and running a typical application using both SRAM and flash.

[8] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal; all peripheral and cores enabled and running a typical application using both SRAM and flash. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature.

[9] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripheral and cores enabled and running a typical application using both SRAM and flash. Only for 208 MAPBGA and only 120C junction or lower. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature

2.12 Pad AC Specifications

Table 18. Pad AC Specifications (VDDE = 3.0V - 5.5V)[1]

Num	Pad Type	SRC	Out Delay[2, 3] (ns)	Rise/Fall[3, 4] (ns)	Load Drive (pF)
1	Slow (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9500	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at VDDE = 3.0V to 5.5V, T_A = TL to TH.

2 This parameter is supplied for reference and is not tested. Add a maximum of one system clock to the output delay for delay with respect to system clock.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

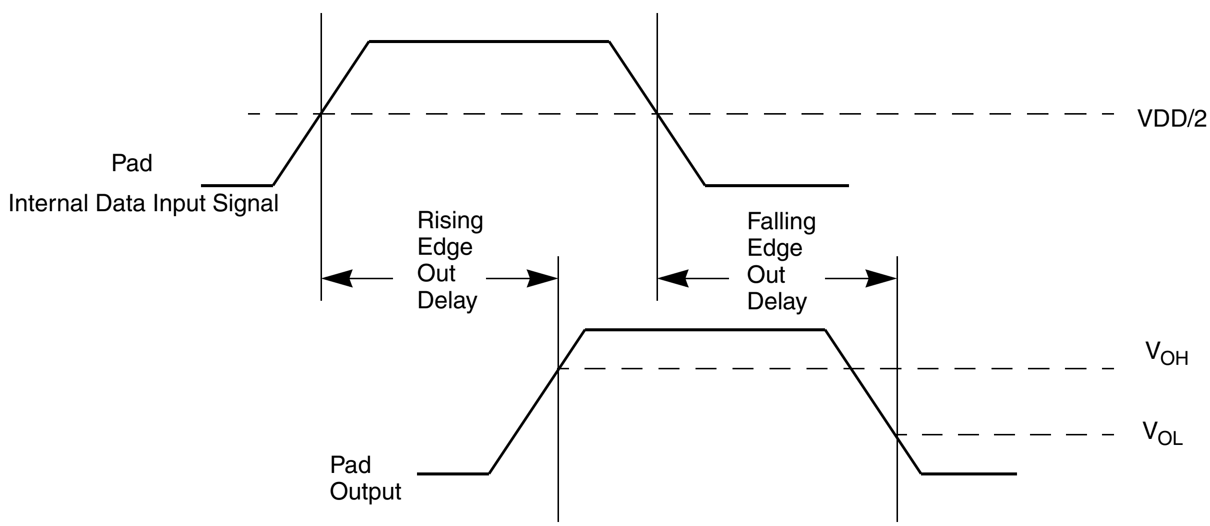

Figure 5. Pad Output Delay

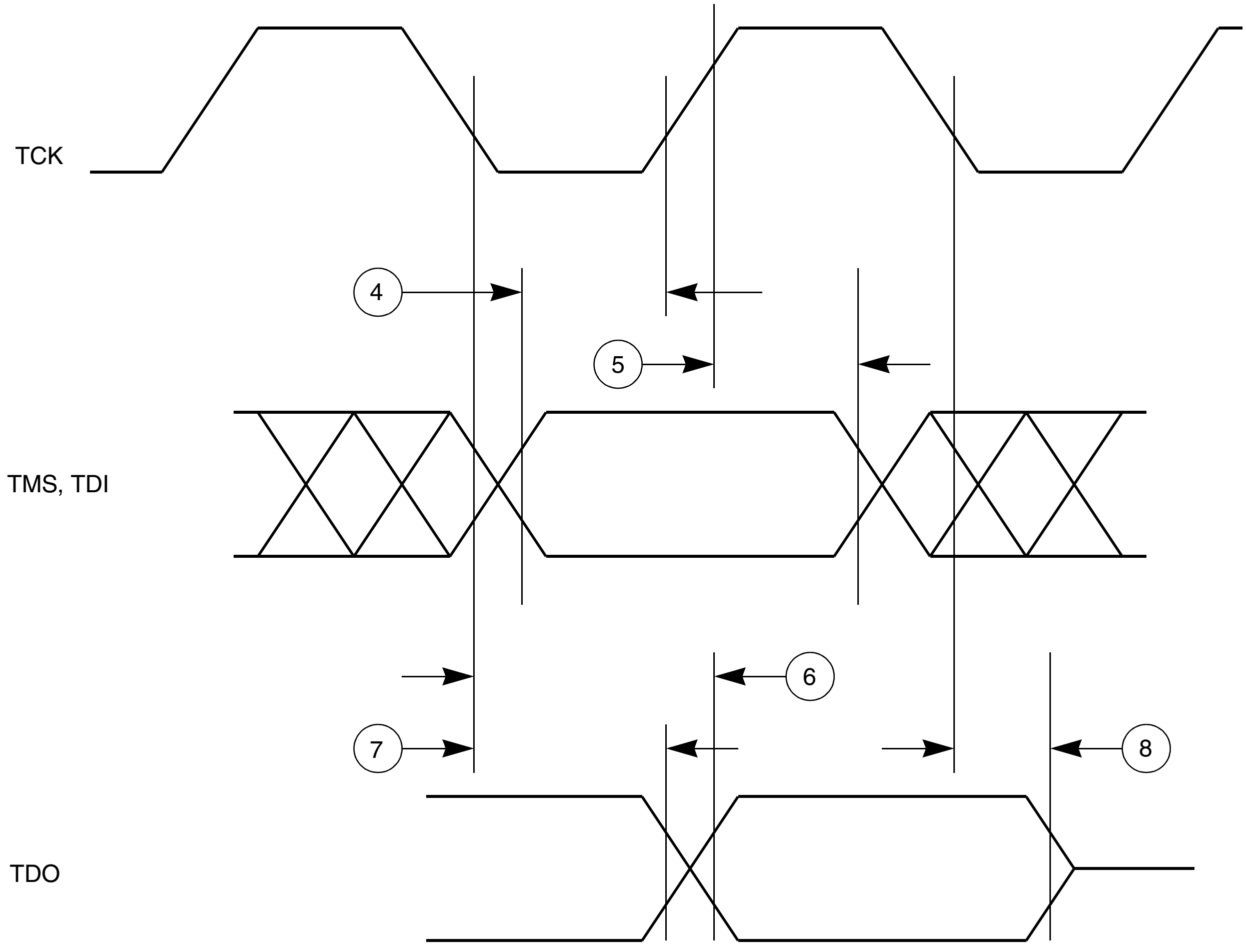

Figure 9. JTAG Test Access Port Timing

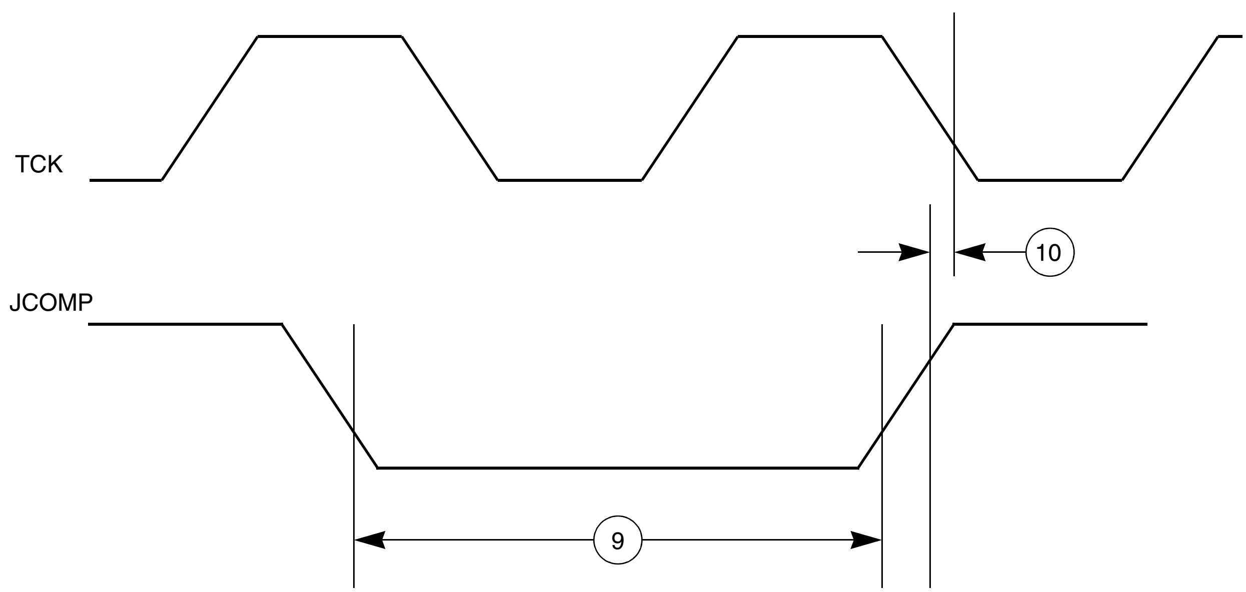

Figure 10. JTAG JCOMP Timing

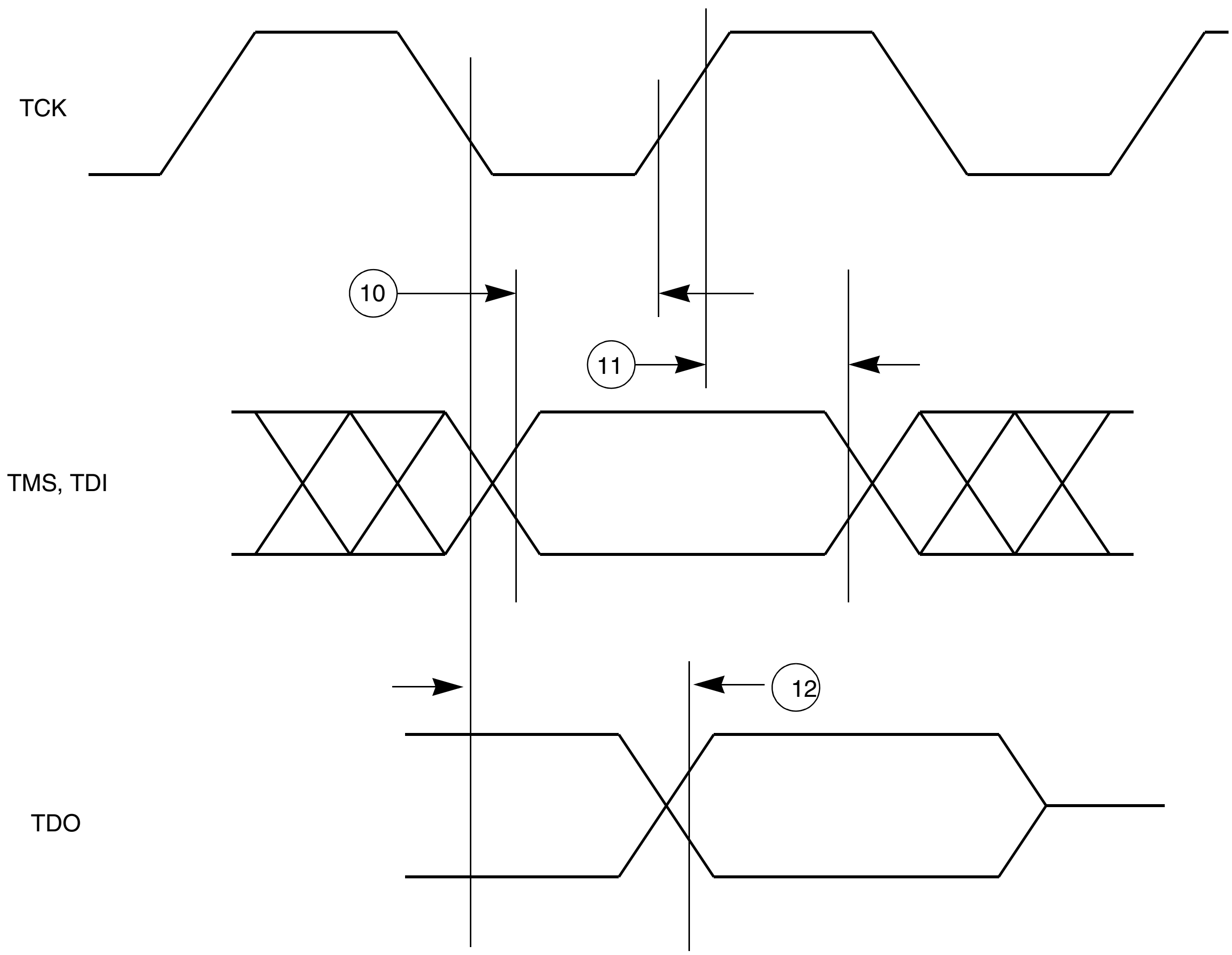

Figure 13. Nexus TDI, TMS, TDO Timing

2.13.7 Deserial Serial Peripheral Interface (DSPI)

Table 25. DSPI Timing[1]

Num	Characteristic	Symbol	66 MHz		Unit
			Min	Max	
1	SCK Cycle TIme[2,3]	t_{SCK}	60	—	ns
2	PCS to SCK Delay[4]	t_{CSC}	20	—	ns
3	After SCK Delay[5]	t_{ASC}	20	—	ns
4	SCK Duty Cycle	t_{SDC}	$t_{SCK}/2$ –2ns	$t_{SCK}/2$ + 2ns	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT driven)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	4	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	5	—	ns
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 35 5 5 35	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[6] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –4 10 26 –4	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA=0) Master (MTFE = 1, CPHA=1)	t_{SUO}	 — — — —	 15 35 30 15	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –15 5.5 0 –15	 — — — —	 ns ns ns ns

1 DSPI timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.
2 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.
3 The actual minimum SCK Cycle Time is limited by pad performance.
4 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]
5 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]
6 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

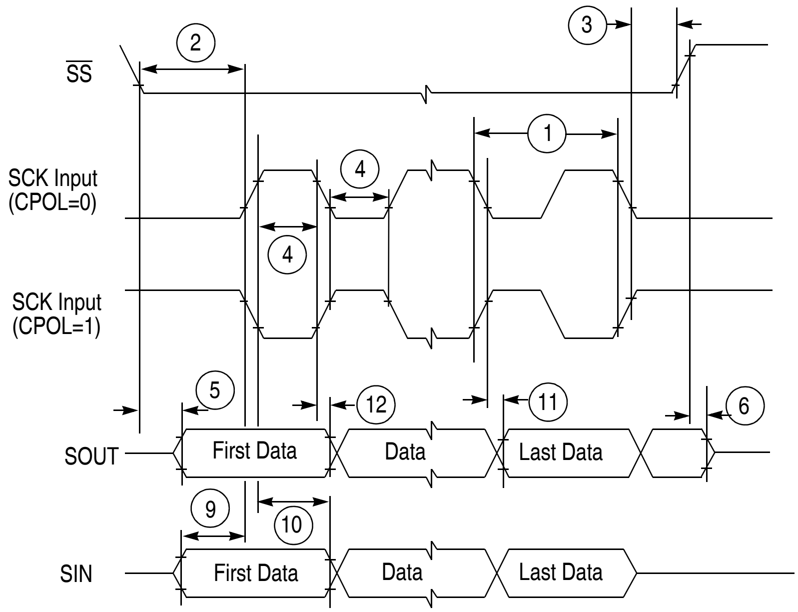

Figure 20. DSPI Classic SPI Timing — Slave, CPHA = 0

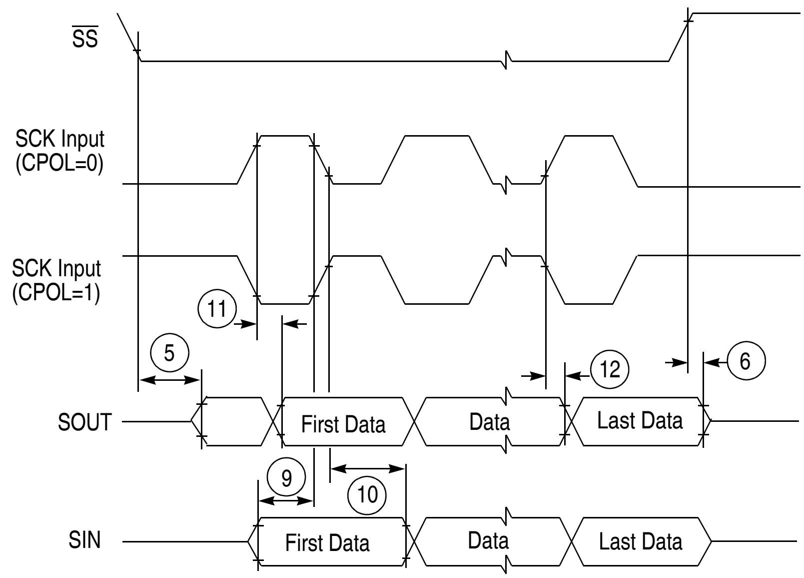

Figure 21. DSPI Classic SPI Timing — Slave, CPHA = 1

3 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/powerpc. The following table lists the package case number per device. Use these numbers in the web page's "keyword" search engine to find the latest package outline drawings.

Table 26. Package Information

Package	Package Case Number
144 LQFP	98ASS23177W
176 LQFP	98ASS23479W
208 MAPBGA	98ARS23882W

4 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/powerpc.

How to Reach Us:

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Document Number: MPC5510
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