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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0, e200z1
Core Size	32-Bit Dual-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5514ebvlq66

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1 Pin Assignments and Reset States

1.1 Signal Properties and Multiplexing Summary

Table 1 shows the signal properties for each pin on the MPC5510. For all port pins, which have an associated pad configuration register (SIU_PCR*n* register) to control its pin properties, the "Supported Pin Functions" column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, Function1, Function2 and Function3. If fewer than three functions plus GPIO are supported by a given pin, then the unused functions begin with Function3, then Function2, then Function1. Note that the GPIO number is the same number as the corresponding pad configuration register (SIU_PCR*n*) number.

Table 1. MPC5510 Signal Properties

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
Port A (16)											
PA0	0	PA0 AN0	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	9	9	E3
PA1	1	PA1 AN1	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	8	8	E2
PA2	2	PA2 AN2	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	7	7	E1
PA3	3	PA3 AN3	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	6	6	D3
PA4	4	PA4 AN4	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	5	5	D2
PA5	5	PA5 AN5	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	4	4	D1
PA6	6	PA6 AN6	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	3	3	C2
PA7	7	PA7 AN7	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	2	2	C1
PA8	8	PA8 AN8/ANW	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	143	175	A3
PA9	9	PA9 AN9/ANX	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	142	174	C4
PA10	10	PA10 AN10/ANY	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	140	172	D5
PA11	11	PA11 AN11/ANZ	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	139	171	C5
PA12	12	PA12 AN12	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	138	170	B5
PA13	13	PA13 AN13	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	137	169	A5
PA14	14	PA14 AN14 EXTAL32[6]	GPI eQADC Analog Input 32 kHz Crystal Oscillator Input	I I I	V_{DDA}	AE + IH	—	—	136	167	D6

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V_{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V_{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX $\overline{TS}$	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V_{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V_{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{TS}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V_{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V_{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V_{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V_{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V_{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Clock	I/O I O I/O	V_{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Data	I/O I O I/O	V_{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 $\overline{CS3}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 $\overline{CS2}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input[7] SCI_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input[7] SCI_E Receive eQADC External Mux Address	I/O I I O	V_{DDE2}	A + SH	—	—	19	24	J3

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PH6	118	PH6 AN21 TXD_F	GPIO eQADC Analog Input[7] SCI_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	18	23	J2
PH7	119	PH7 AN20 RXD_F	GPIO eQADC Analog Input[7] SCI_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	17	22	J1
PH8	120	PH8 AN19 CNTX_E MA0	GPIO eQADC Analog Input[7] CAN_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	14	17	H1
PH9	121	PH9 AN18/ANT CNRX_E	GPIO eQADC Analog Input[7] CAN_E Receive	I/O I I	V_{DDE2}	A + SH	—	—	13	14	G2
PH10	122	PH10 AN17/ANS CNRX_F	GPIO eQADC Analog Input[7] CAN_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	12	12	F4
PH11	123	PH11 AN16/ANR CNTX_F	GPIO eQADC Analog Input[7] CAN_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	11	11	F3
PH12	124	PH12 PCS_D5	GPIO DSPI_D Peripheral Chip Select	I/O O	V_{DDE2}	SH	—	—	—	—	F2
PH13	125	PH13	GPIO	I/O	V_{DDE2}	SH	—	—	—	—	F1
PH14	126	PH14 $\overline{WE2}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	53	T5
PH15	127	PH15 $\overline{WE3}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	52	R5
Port J (16)											
PJ0	128	PJ0 AD0	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N11
PJ1	129	PJ1 AD1	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	P11
PJ2	130	PJ2 AD2	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N10
PJ3	131	PJ3 AD3	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	R10
PJ4	132	PJ4 AD4	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	75	P10
PJ5	133	PJ5 AD5	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	73	T9
PJ6	134	PJ6 AD6	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	69	P9
PJ7	135	PJ7 AD7	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	67	R8

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PJ8	136	PJ8 PCS_D4	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	27	K2
PJ9	137	PJ9 PCS_D3	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	26	K1
PJ10	138	PJ10 PCS_D2	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	25	J4
PJ11	139	PJ11 PCS_D1	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	19	H3
PJ12	140	PJ12 PCS_D0	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	18	H2
PJ13	141	PJ13 SCK_D	GPIO DSPI_D Clock	I/O I/O	V_{DDE2}	SH	—	—	—	16	G4
PJ14	142	PJ14 SOUT_D	GPIO DSPI_D Serial Out	I/O O	V_{DDE2}	SH	—	—	—	15	G3
PJ15	143	PJ15 SIN_D	GPIO DSPI_D Serial In	I/O I	V_{DDE2}	SH	—	—	—	13	G1
Port K (2)											
PK0	144	PK0 EXTAL32	GPIO 32 kHz Crystal Oscillator Input	I I	V_{DDA}	AE + IH	—	—	—	168	B6
PK1	145	PK1 XTAL32	GPIO 32 kHz Crystal Oscillator Output	I O	V_{DDA}	AE + IH	—	—	—	166	A6
Miscellaneous Pins (9)											
EXTAL	—	EXTAL EXTCLK	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	AE	EXTAL		75	91	N16
XTAL	—	XTAL	Main Crystal Oscillator Output	O	V_{DDSYN}	AE	XTAL		74	90	P16
TMS	—	TMS	JTAG Test Mode Select Input	I	V_{DDE3}	SH	TMS (Pull Up)		72	88	T15
TCK	—	TCK	JTAG Test Clock Input	I	V_{DDE3}	IH	TCK (Pull Down)		71	87	R14
TDO	—	TDO	JTAG Test Data Output	O	V_{DDE3}	MH	TDO (Pull Up[9])		70	86	T14
TDI	—	TDI	JTAG Test Data Input	I	V_{DDE3}	IH	TDI (Pull Up)		69	85	R13
JCOMP	—	JCOMP	JTAG Compliancy	I	V_{DDE3}	IH	JCOMP (Pull Down)		68	84	T13
TEST[10]	—	TEST	Test Mode Select	I	V_{DDE3}	IH	TEST		62	78	R11
$\overline{\text{RESET}}$	—	$\overline{\text{RESET}}$	External Reset	I/O	V_{DDE2}	SH	$\overline{\text{RESET}}$ (Pull Up)		10	10	E4

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

2 This column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, function 1, function 2, and function 3. The unused functions by a given pin begin with function 3, then function 2, then function 1.

3 These are nominal voltages. Each segment provides the power and ground for the given set of I/O pins.

4 Pad types: SH - Bi-directional slow speed pad with input hysteresis; MH - Bi-directional medium speed pad with input hysteresis; IH - Input only pad with input hysteresis; AE/A - Analog pad.

5 A dash for the function in this column denotes the input and output buffer are turned off.

1.3 Pinout – 144 LQFP

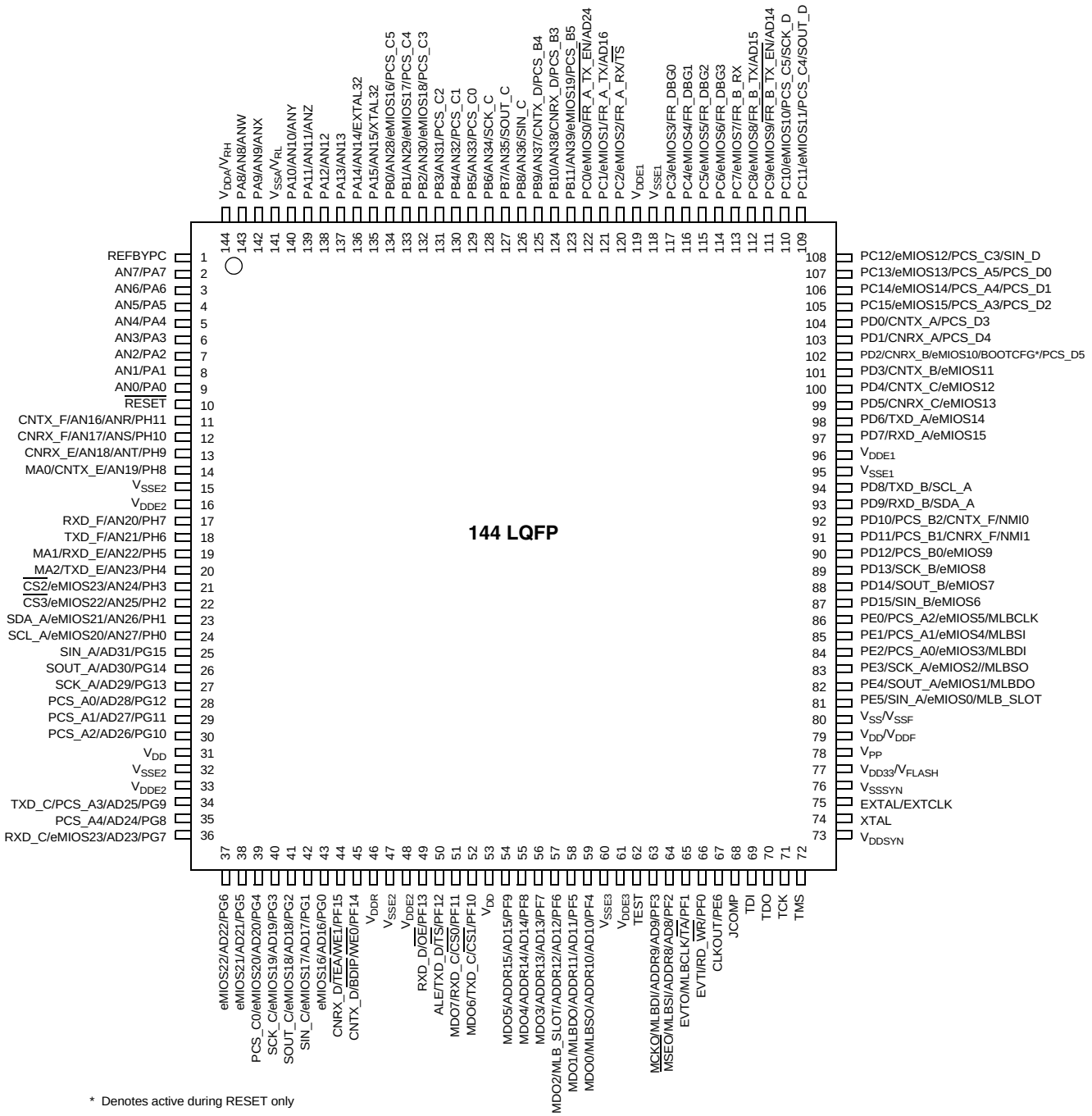

Figure 2. MPC5510 Pinout – 144 LQFP

1.4 Pinout – 176 LQFP

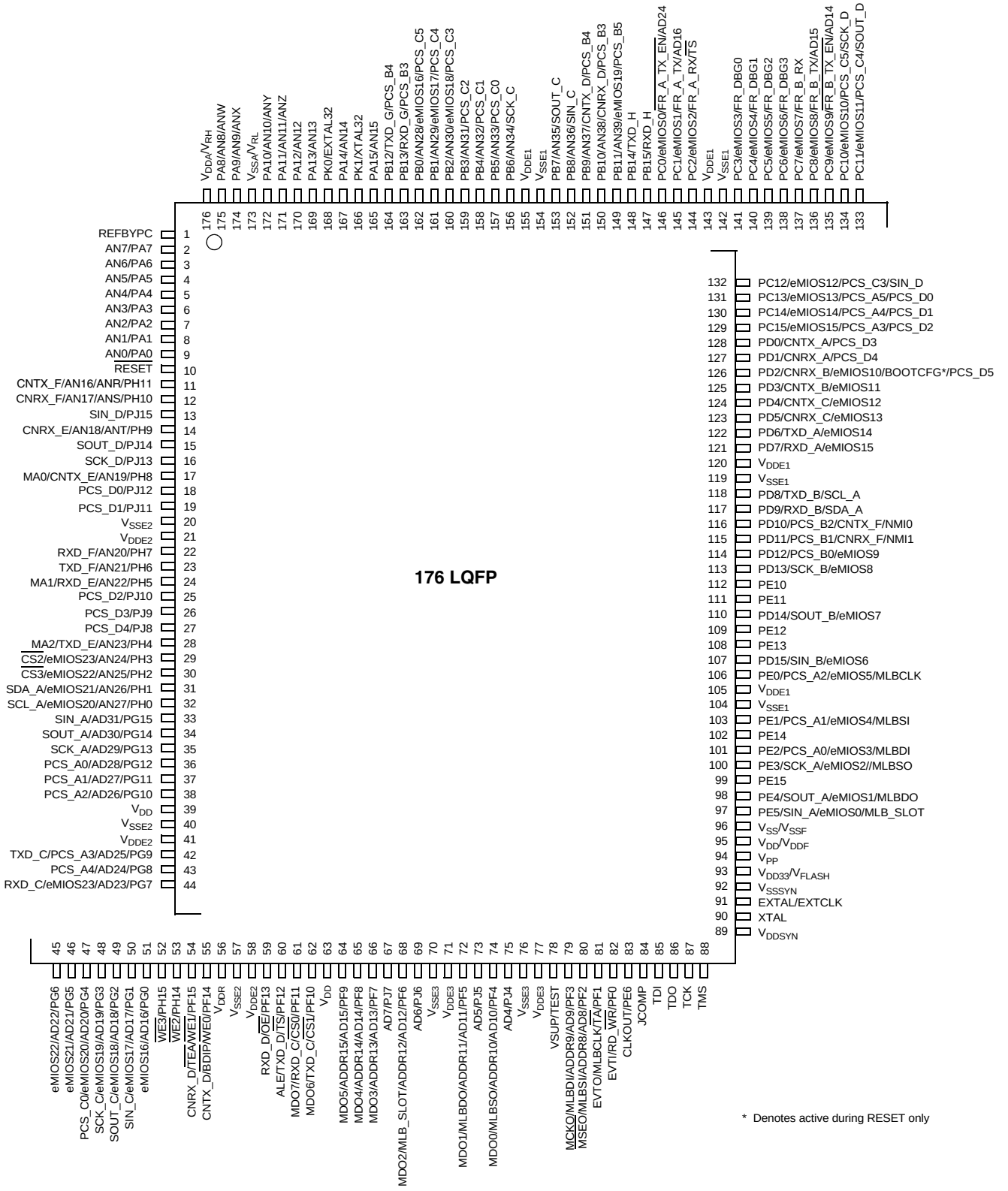

Figure 3. MPC5510 Pinout – 176 LQFP

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	5.0V Voltage Regulator Reference Voltage	V_{DDR}	– 0.3	6.5	V
2	5.0V Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	– 0.3	6.5	V
3	5.0V Flash Program/Erase Voltage	V_{PP}	– 0.3	6.5	V
4	3.3V – 5.0V External I/O Supply Voltage [3]	V_{DDE1}[4] V_{DDE2}[4] V_{DDE3}[4]	– 0.3 – 0.3 – 0.3	6.5 6.5 6.5	V
5	DC Input Voltage [5]	V_{IN}	–1.0[6]	6.5[7]	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 0.3	5.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 5.5	5.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 0.3	0.3	V
9	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	$- V_{DDA}$	0.3	V
10	Maximum DC Digital Input Current [8] (per pin, applies to all digital MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
11	Maximum DC Analog Input Current [9] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
12	Storage Temperature Range	T_{STG}	– 55.0	150.0	°C
13	Maximum Solder Temperature [10]	T_{SDR}	—	260.0	°C
14	Moisture Sensitivity Level [11]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn–in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 AC signal over and undershoot of the input voltages of up to +/– 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

6 Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

7 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25mA.

9 Total injection current for all analog input pins must not exceed 15mA.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 4. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	176 LQFP	144 LQFP
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	44	38	43
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	27	31	34
3	Junction to Ambient [1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	35	30	34
4	Junction to Ambient [1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	24	25	28
5	Junction to Board [4]	$R_{\theta JB}$	°C/W	16	20	22
6	Junction to Case [5]	$R_{\theta JC}$	°C/W	8	6	7
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	°C/W	2	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package } (^oC) \quad \textit{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance } (^oC/W) \quad \textit{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \textit{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 5}$$

where:

T_J = junction temperature (^oC) *Eqn. 6*

T_B = board temperature at the package perimeter ($^oC/W$) *Eqn. 7*

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8 *Eqn. 8*

P_D = power dissipation in the package (W) *Eqn. 9*

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 10}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$) *Eqn. 11*

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$) *Eqn. 12*

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$) *Eqn. 13*

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

2.4 DC Electrical Specifications

Table 6. DC Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1a	**C parts** Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 105 85	 °C °C
1b	**V parts** Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 120 105	 °C °C
1c	**M parts**[2] Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 145 125	 °C °C
2	5.0V Voltage Regulator Reference Voltage	V_{DDR}	4.5	5.25	V
3	5.0V Analog Supply Voltage	V_{DDA}	4.5	5.25	V
4	5.0V Flash Program/Erase Voltage [3]	V_{PP}	4.5	5.25	V
5	3.3V – 5.0V External I/O Supply Voltage	V_{DDE1}[4,5] V_{DDE2}[4] V_{DDE3}[4]	3.0 3.0 3.0	5.5 5.5 5.5	V
6	Pad (SH/MH/IH) Input High Voltage	V_{IH}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
7	Pad (SH/MH/IH) Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
8	Pad (SH/MH/IH) Input Hysteresis	V_{HYS}	$0.1 \times V_{DDE}$	$0.2 \times V_{DDE}$	V
9	Analog (AE/A) Input Voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$ see note[5]	V
10	Slow/Medium I/O Output High Voltage I_{OH} = –1.0 mA I_{OH} = –0.2 mA	V_{OH}	 $0.80 \times V_{DDE}$ $0.95 \times V_{DDE}$	 —	V
11	Slow/Medium I/O Output Low Voltage I_{OL} = 1.0 mA I_{OH} = 0.2 mA	V_{OL}	—	 $0.20 \times V_{DDE}$ $0.05 \times V_{DDE}$	V
12	Input Capacitance (Digital Pins: Pad type MH,SH, IH with no A or AE)	C_{IN}	—	7	pF
13	Input Capacitance (Analog Pins: Pad type A, AE, and AE+IH)	C_{IN_A}	—	10	pF
14	Input Capacitance (Shared digital and analog pins: A with SH or MH)	C_{IN_M}	—	12	pF
15	Slow/Medium I/O Weak Pull Up/Down Absolute Current [6]	I_{ACT}	10	170	µA
16	I/O Input Leakage Current [7]	I_{INACT_D}	– 1.5	1.5	µA
17	DC Injection Current (per pin)	I_{IC}	– 2.0	2.0	mA
18	Analog Input Current, Channel Off [8] (Analog pins AE and AE+IH)	I_{INACT_A}	– 200	200	nA
19	Analog Input Current (Shared digital and analog pins: A with SH or MH)	I_{INACT_AD}	–1.5	1.5	µA
20	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 100	100	mV

Table 6. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
21	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 100	100	mV
22	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} - V_{SSA}$	– 100	100	mV
23	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
24	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	– 100	100	mV
25	Slew rate on VDDA, VDDR, and VDDE power supply pins[9]	Vramp	1	100	V/ms
26	Capactive Supply Load VDD VDD33 VDDSYN	Vload	 800 200 200	 — —	nF

1 Please refer to Section 2.2.1, “General Notes for Specifications at Maximum Junction Temperature” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

2 M parts can’t go above 66 MHz.

3 V_{PP} can drop to 0 volts during read-only operations and before entry to Sleep mode, to reduce power consumption.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 If V_{DDE1} is below V_{DDA} than the analog input limits (spec #9 (Analog (AE/A) Input Voltage) in Table 6) will be based on the V_{DDE1} voltage level.

6 Absolute value of current, measured at V_{IL} and V_{IH}.

7 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH.

8 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: A and AE.

9 This applies to the ramp up rate from 0.3 volts to 3.0 volts.

2.12 Pad AC Specifications

Table 18. Pad AC Specifications (VDDE = 3.0V - 5.5V)[1]

Num	Pad Type	SRC	Out Delay[2, 3] (ns)	Rise/Fall[3, 4] (ns)	Load Drive (pF)
1	Slow (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9500	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at VDDE = 3.0V to 5.5V, T_A = TL to TH.

2 This parameter is supplied for reference and is not tested. Add a maximum of one system clock to the output delay for delay with respect to system clock.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

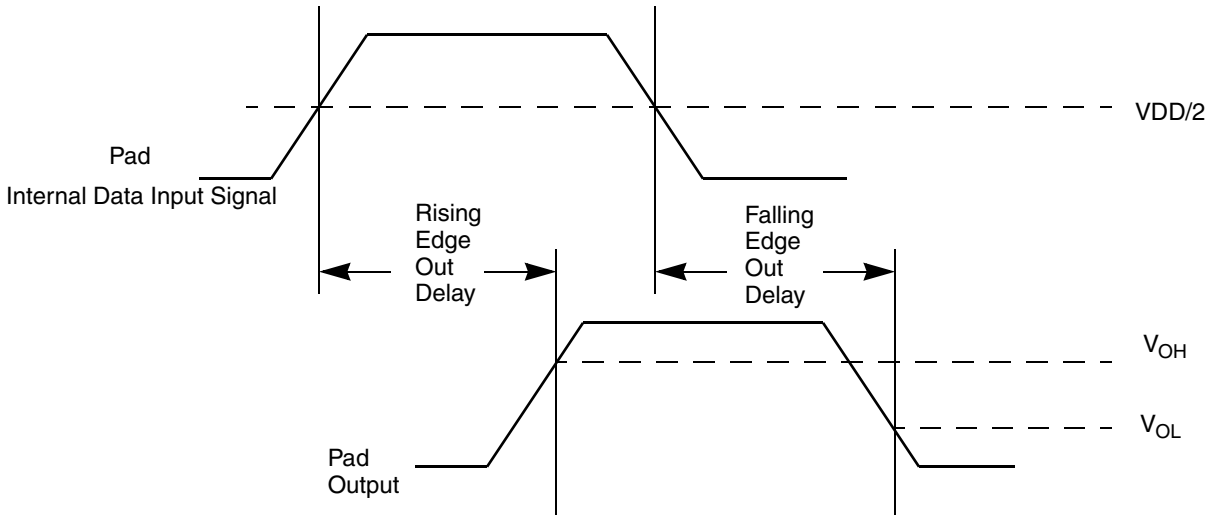

Figure 5. Pad Output Delay

2.13 AC Timing

2.13.1 Reset and Boot Configuration Pins

Table 19. Reset and Boot Configuration Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

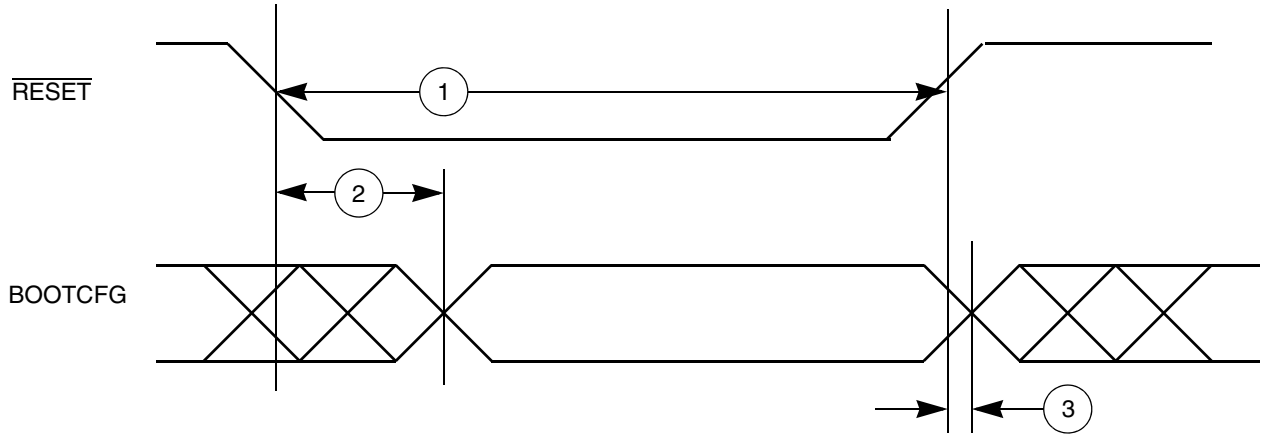

Figure 6. Reset and Boot Configuration Timing

2.13.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 20. IRQ/NMI Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

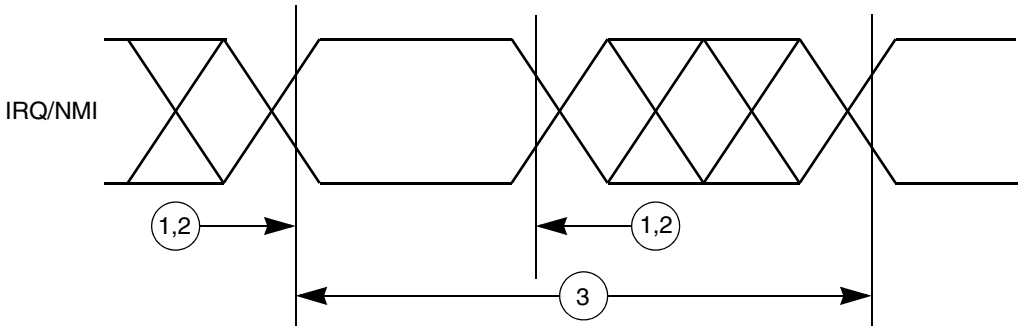

Figure 7. IRQ and NMI Timing

2.13.3 JTAG (IEEE 1149.1) Interface

Table 21. JTAG Interface Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at VDDE/2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	20	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

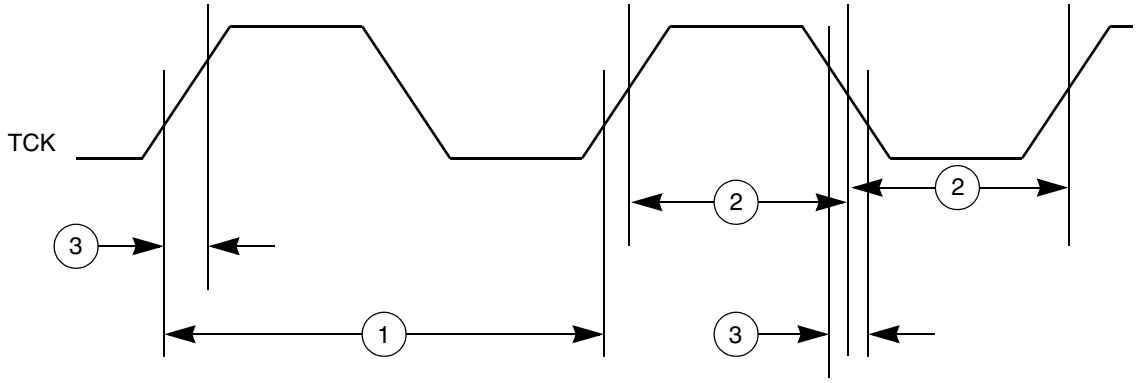

Figure 8. JTAG Test Clock Input Timing

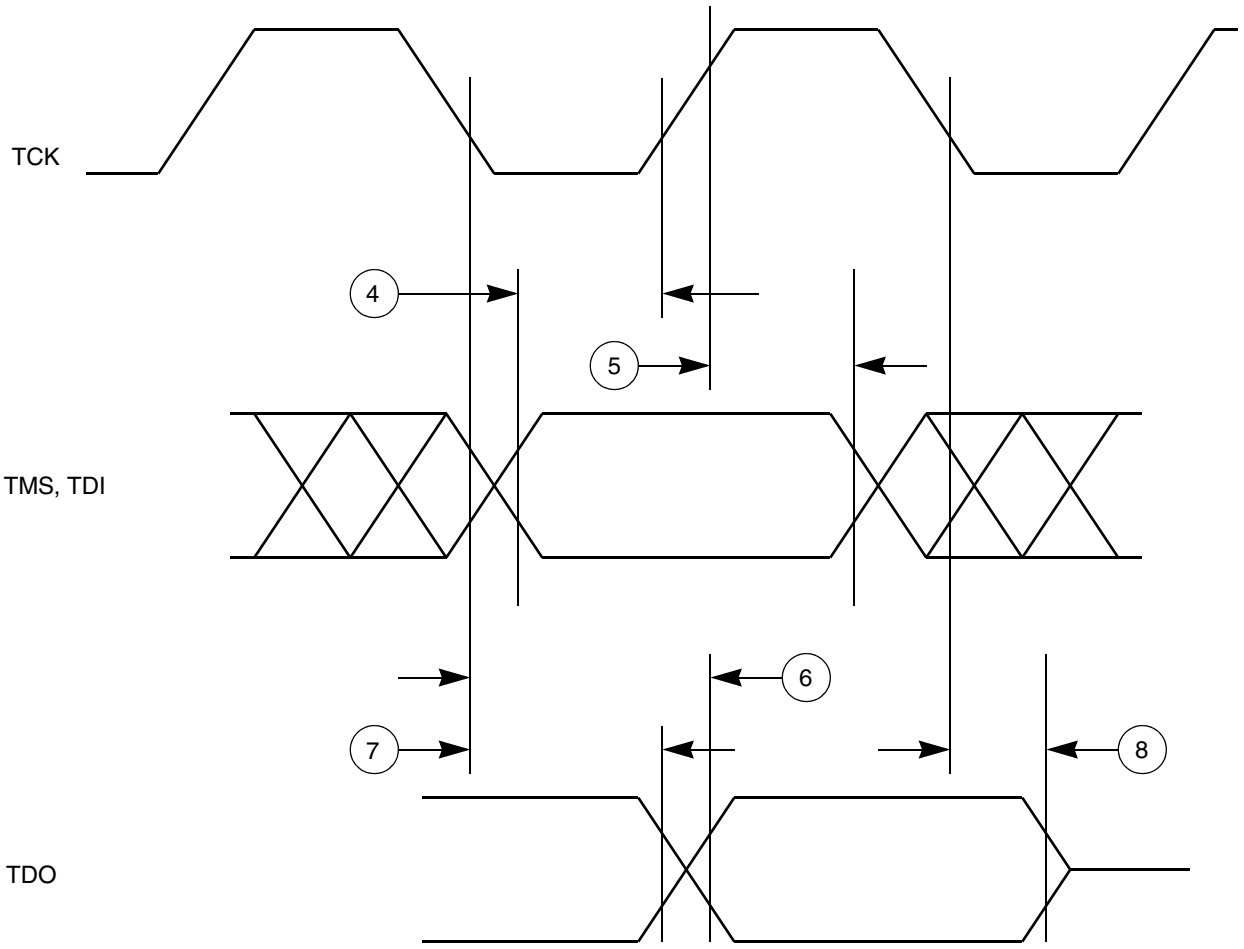

Figure 9. JTAG Test Access Port Timing

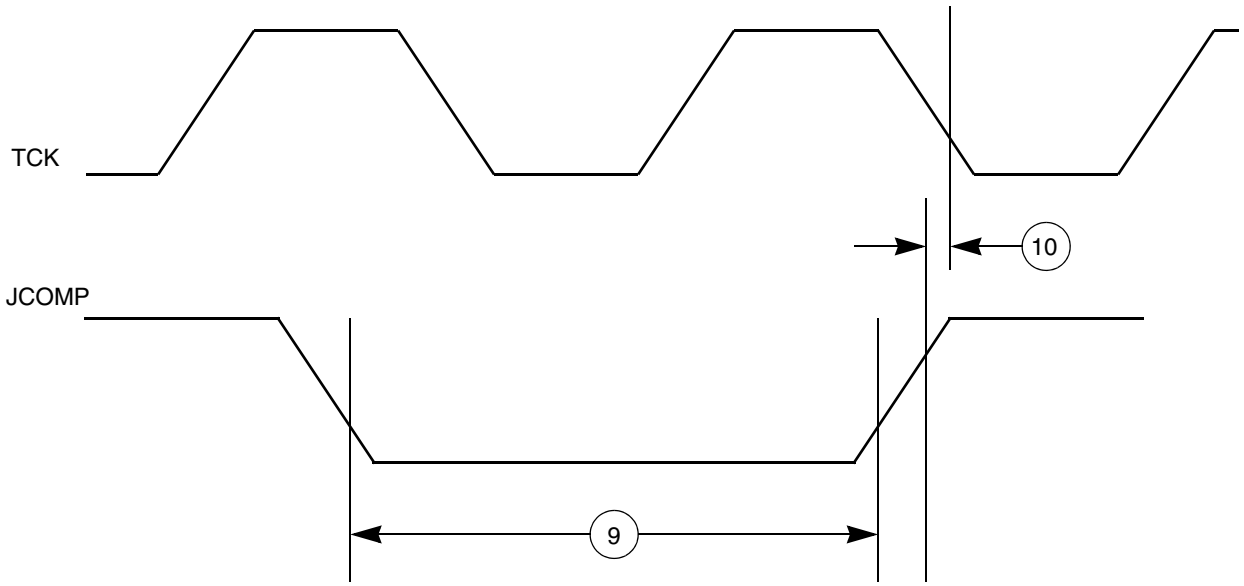

Figure 10. JTAG JCOMP Timing

2.13.4 Nexus Debug Interface

Table 22. Nexus Debug Port Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	40	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–2	4.0	ns
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–2	4.0	ns
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–2	4.0	ns
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
8	TCK Cycle Time[3]	t_{TCYC}	40	—	ns
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	4	—	ns
12	TCK Low to TDO Data Valid	t_{JOV}	0	8	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster that the TCK frequency.

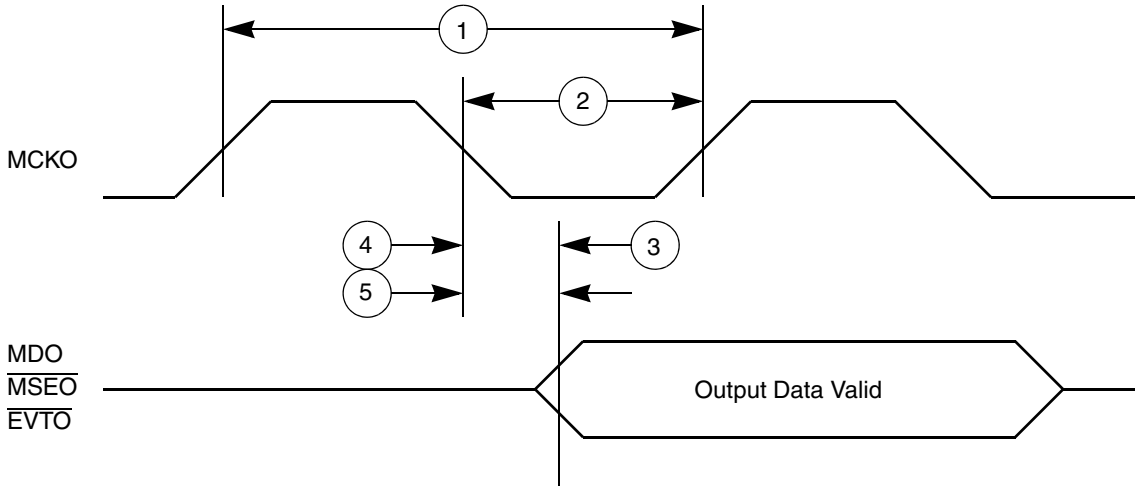

Figure 12. Nexus Output Timing

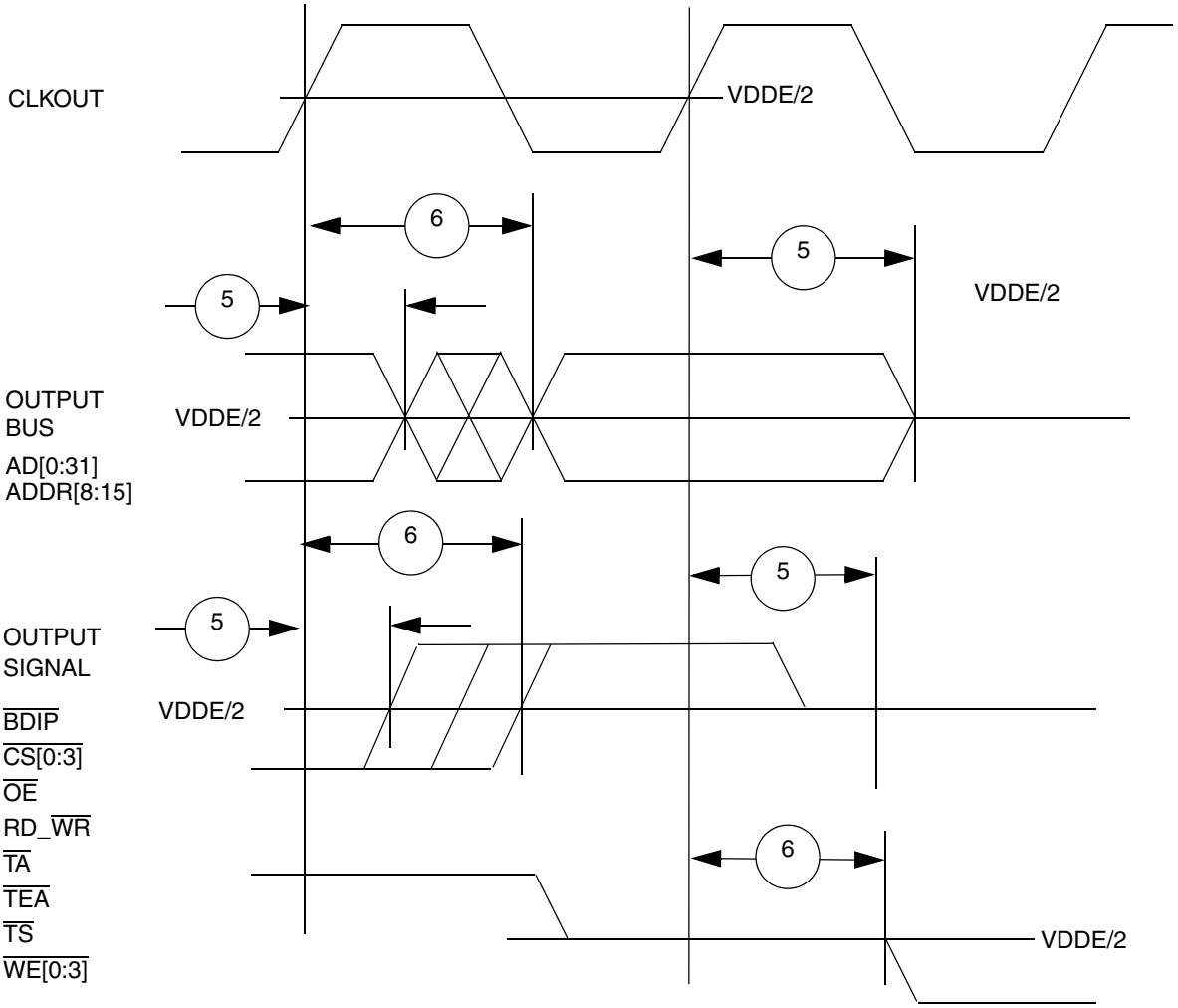

Figure 15. Synchronous Output Timing