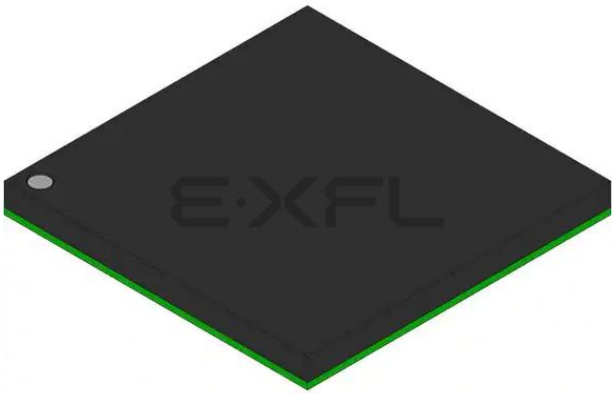

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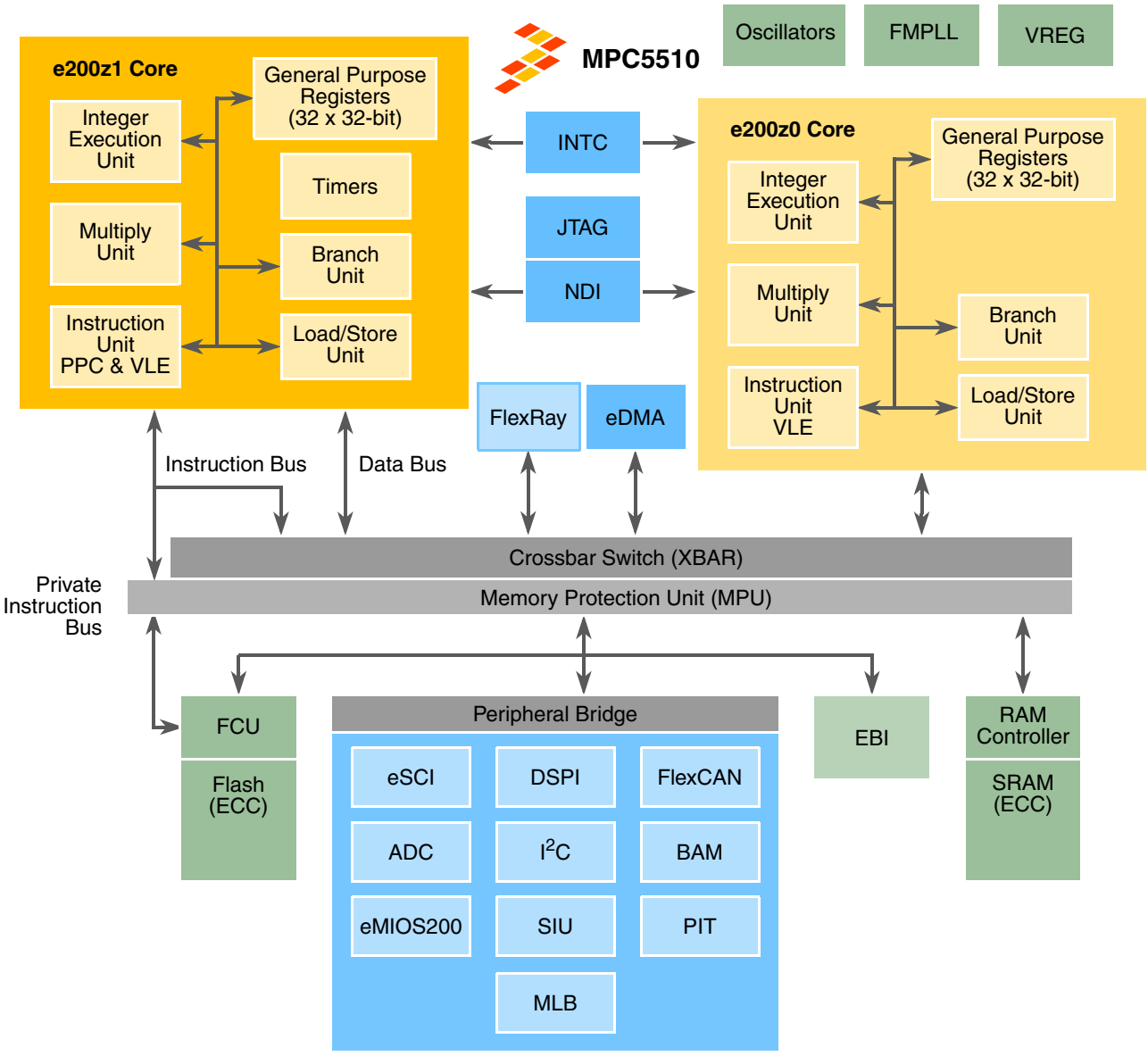
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0, e200z1
Core Size	32-Bit Dual-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	144
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5516eacmg48



LEGEND

ADC	– Analog to Digital Converter modules	**FlexRay**	– Dual Channel FlexRay controller
BAM	– Boot Assist Module	**FMPLL**	– Frequency Modulated Phase Locked Loop module
EBI	– External Bus Interface module	**I^2C**	– Inter IC Controller modules
ECC	– Error Correction Code	**INTC**	– Interrupt Controller module
DSPI	– Serial Peripherals Interface controller module	**JTAG**	– Joint Test Action Group interface
eDMA	– enhanced Direct Memory Controller module	**MLB**	– Media Local Bus emulation logic
eMIOS200	– Timed Input Output module	**NDI**	– Nexus Debug Interface module
eSCI	– Serial Communications Interface modules	**PIT**	– Periodic Interrupt Timer module
FCU	– Flash Controller Unit	**SIU**	– System Integration module
FlexCAN	– Controller Area Network controller modules	**VREG**	– Voltage Regulator

Figure 1. MPC5510 Family Block Diagram

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V_{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V_{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX $\overline{TS}$	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V_{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V_{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PE3	67	PE3 SCK_A eMIOS2 MLBSO / MLBSIG_BUFEN	GPIO DSPI_A Clock eMIOS Channel MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin)	I/O I/O O O O	V_{DDE1}	MH	—	—	83	100	M13
PE4	68	PE4 SOUT_A eMIOS1 MLBDO / MLBDAT_BUFEN	GPIO DSPI_A Data Out eMIOS Channel MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin)	I/O O O O O	V_{DDE1}	MH	—	—	82	98	N14
PE5	69	PE5 SIN_A eMIOS0 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS	GPIO DSPI_A Data In eMIOS Channel MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data	I/O I O O O O	V_{DDE1}	MH	—	—	81	97	M15
PE6	70	PE6 CLKOUT	GPIO System Clock Output	I/O O	V_{DDE3}	MH	—	—	67	83	P13
PE7	71	PE7	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H13
PE8	72	PE8	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H16
PE9	72	PE9	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	J13
PE10	74	PE10	GPIO	I/O	V_{DDE1}	SH	—	—	—	112	J16
PE11	75	PE11	GPIO	I/O	V_{DDE1}	SH	—	—	—	111	J15
PE12	76	PE12	GPIO	I/O	V_{DDE1}	SH	—	—	—	109	K13
PE13	77	PE13	GPIO	I/O	V_{DDE1}	SH	—	—	—	108	L13
PE14	78	PE14	GPIO	I/O	V_{DDE1}	SH	—	—	—	102	L16
PE15	79	PE15	GPIO	I/O	V_{DDE1}	SH	—	—	—	99	M14
Port F (16)											
PF0	80	PF0 RD_$\overline{WR}$ EVTI[8]	GPIO EBI Read/Write Nexus Event In	I/O I/O I	V_{DDE3}	MH	—	—	66	82	N12
PF1	81	PF1 $\overline{TA}$ MLBCLK EVTO[8]	GPIO EBI Transfer Acknowledge MLB Clock Nexus Event Out	I/O I/O I O	V_{DDE3}	MH	—	—	65	81	P12
PF2	82	PF2 AD8 ADDR8 MLBSI / MLBSIG $\overline{MSEO}$[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal In (5-pin) / MLB Bi-Directional Signal (3-pin) Nexus Message Start/End Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	64	80	R12

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{TS}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF13	93	PF13 $\overline{OE}$ RXD_D	GPIO EBI Output Enable SCI_D Receive	I/O O I	V_{DDE2}	MH	—	—	49	59	R6
PF14	94	PF14 $\overline{WE0}$ $\overline{BDIP}$ CNTX_D	GPIO EBI Write Enable EBI Burst Data In Progress CAN_D Transmit	I/O O O O	V_{DDE2}	MH	—	—	45	55	P6
PF15	95	PF15 $\overline{WE1}$ $\overline{TEA}$ CNRX_D	GPIO EBI Write Enable EBI Transfer Error Acknowledge CAN_D Receive	I/O O I/O I	V_{DDE2}	MH	—	—	44	54	N6
Port G (16)											
PG0	96	PG0 AD16 eMIOS16	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	43	51	P5
PG1	97	PG1 AD17 eMIOS17 SIN_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial In	I/O I/O I/O I	V_{DDE2}	MH	—	—	42	50	T4
PG2	98	PG2 AD18 eMIOS18 SOUT_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Out	I/O I/O I/O O	V_{DDE2}	MH	—	—	41	49	R4
PG3	99	PG3 AD19 eMIOS19 SCK_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Clock	I/O I/O I/O I/O	V_{DDE2}	MH	—	—	40	48	P4
PG4	100	PG4 AD20 eMIOS20 PCS_C0	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Peripheral Chip Select	I/O I/O I/O I/O	V_{DDE2}	MH	—	—	39	47	T3
PG5	101	PG5 AD21 eMIOS21	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	38	46	R3
PG6	102	PG6 AD22 eMIOS22	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V_{DDE2}	MH	—	—	37	45	T2
PG7	103	PG7 AD23 eMIOS23 RXD_C	GPIO EBI Muxed Address/Data eMIOS Channel SCI_C Receive	I/O I/O I/O I	V_{DDE2}	MH	—	—	36	44	R1
PG8	104	PG8 AD24 PCS_A4	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	35	43	P2

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V_{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V_{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V_{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V_{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V_{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Clock	I/O I O I/O	V_{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Data	I/O I O I/O	V_{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 $\overline{CS3}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 $\overline{CS2}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input[7] SCI_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input[7] SCI_E Receive eQADC External Mux Address	I/O I I O	V_{DDE2}	A + SH	—	—	19	24	J3

3 V_{RL} is shorted to V_{SSA} in the 144LQFP and 176 LQFP packages.

4 V_{PP} requires 5V for program/erase operations, but may be 0-5V otherwise. V_{PP} should not go high or low when the device is in Sleep mode.

5 Voltage generated from internal voltage regulator and no external connection or load allowed except the required bypass capacitors.

6 V_{FLASH} is shorted to V_{DD33} in the package.

1.4 Pinout – 176 LQFP

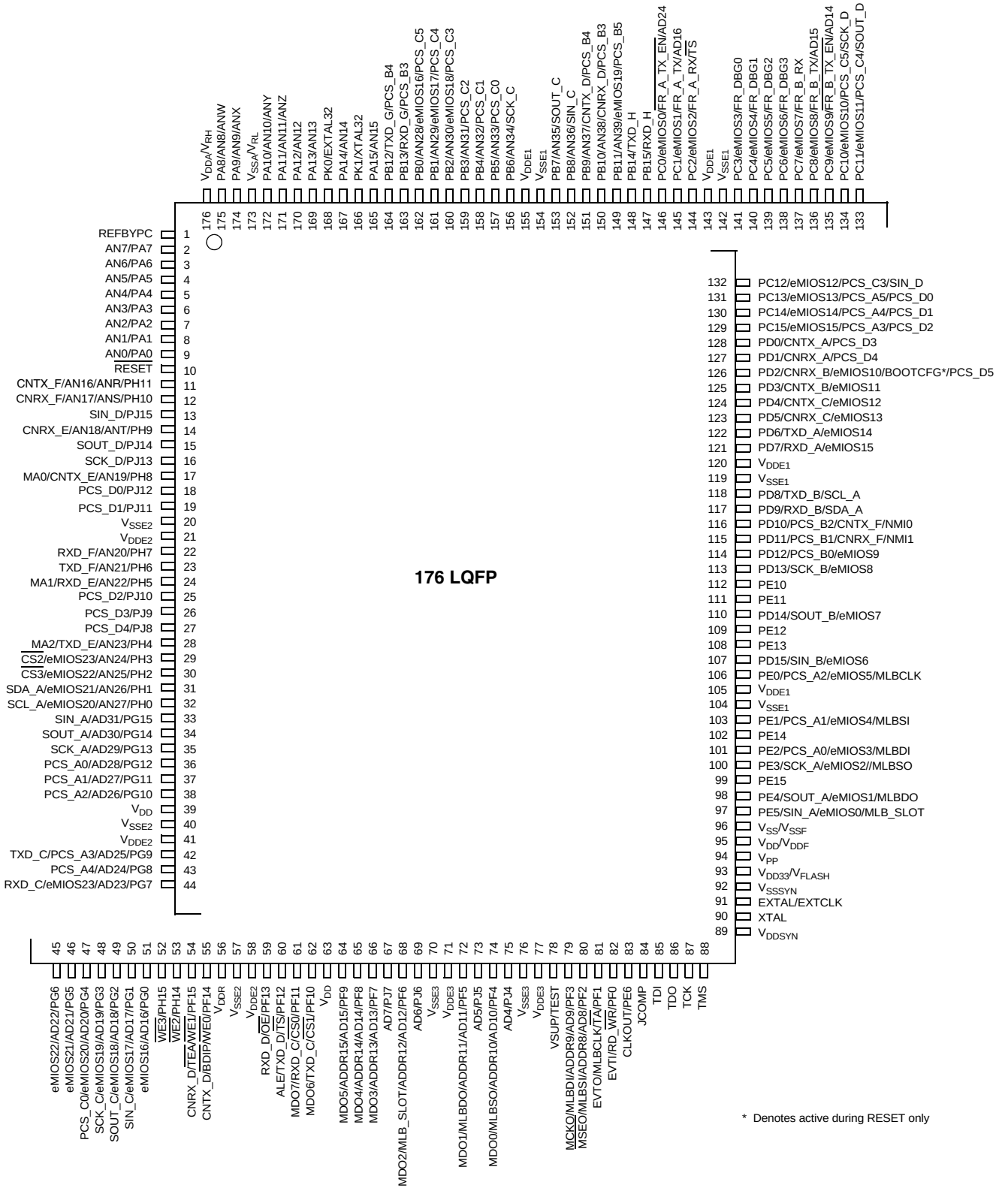


Figure 3. MPC5510 Pinout – 176 LQFP

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	5.0V Voltage Regulator Reference Voltage	V_{DDR}	– 0.3	6.5	V
2	5.0V Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	– 0.3	6.5	V
3	5.0V Flash Program/Erase Voltage	V_{PP}	– 0.3	6.5	V
4	3.3V – 5.0V External I/O Supply Voltage [3]	V_{DDE1}[4] V_{DDE2}[4] V_{DDE3}[4]	– 0.3 – 0.3 – 0.3	6.5 6.5 6.5	V
5	DC Input Voltage [5]	V_{IN}	–1.0[6]	6.5[7]	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 0.3	5.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 5.5	5.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 0.3	0.3	V
9	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	$- V_{DDA}$	0.3	V
10	Maximum DC Digital Input Current [8] (per pin, applies to all digital MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
11	Maximum DC Analog Input Current [9] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
12	Storage Temperature Range	T_{STG}	– 55.0	150.0	°C
13	Maximum Solder Temperature [10]	T_{SDR}	—	260.0	°C
14	Moisture Sensitivity Level [11]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn–in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 AC signal over and undershoot of the input voltages of up to +/– 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

6 Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

7 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25mA.

9 Total injection current for all analog input pins must not exceed 15mA.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 4. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	176 LQFP	144 LQFP
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	44	38	43
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	27	31	34
3	Junction to Ambient [1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	35	30	34
4	Junction to Ambient [1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	24	25	28
5	Junction to Board [4]	$R_{\theta JB}$	°C/W	16	20	22
6	Junction to Case [5]	$R_{\theta JC}$	°C/W	8	6	7
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	°C/W	2	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package } (^oC) \quad \textit{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance } (^oC/W) \quad \textit{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \textit{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 5}$$

where:

T_J = junction temperature (^oC) *Eqn. 6*

T_B = board temperature at the package perimeter ($^oC/W$) *Eqn. 7*

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8 *Eqn. 8*

P_D = power dissipation in the package (W) *Eqn. 9*

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 10}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$) *Eqn. 11*

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$) *Eqn. 12*

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$) *Eqn. 13*

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

2.5 Operating Current Specifications

Table 7. Operating Currents

Num	Characteristic	Symbol	Typ[1] 25C Ambient	Typ[1] 70C Ambient	Max[1] -40–145C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{PP} + I_{DDA} + I_{DDR}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3}$					
1	$V_{DDE(1,2,3)}$ Current $V_{DDE(1,2,3)}$ @ 3.0V - 5.5V Static[2], or when in SLEEP or STOP Dynamic[3]	I_{DDE}	 1 Note [3]	 3 Note [3]	 30 Note [3]	 µA mA
2	V_{PP} Current V_{PP} @ 0V (All modes) V_{PP} @ 5.25V SLEEP mode STOP mode RUN mode	I_{PP}	 1 15 15 1	 1 20 20 1	 1 30 30 25	 µA µA µA mA
3	V_{DDA} Current V_{DDA} @ 4.5V - 5.25V RUN mode[4] SLEEP/STOP[5] mode with 32KIRC SLEEP/STOP[5] mode with 32KOSC SLEEP/STOP[5] mode with 16MIRC	I_{DDA}	 5 12 12 111	 5 16 16 165	 10 26 28 225	 mA µA µA µA
4	V_{DDR} Current V_{DDR} @ 4.5V - 5.25V SLEEP mode with XOSC[6] (additonal) with RTC/API (additonal) each 8K RAM block (additional) STOP mode with XOSC[6] (additonal) RUN mode (Using 16 MHz IRC) RUN mode (Maximum @ 48 MHz)[7] RUN mode (Maximum @ 66 MHz)[8] RUN mode (Maximum @ 80MHz)[9]	I_{DDR}	 20 500 1 0.8 170 500 30 50 105 120	 25 600 1 7 600 600 35 75 110 130	 360 900 3 45 1500 900 40 90 120 135	 µA µA µA µA µA µA mA mA mA mA

1 Typ - Nominal voltage levels and functional activity. Max - Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 8 for more information.

4 RUN mode is a typical application with the ADC, 16MIRC, 32KIRC running.

5 SLEEP/STOP mode means that only the listed peripherals are on. All others are diabled.

6 XOSC: optionally enabled in SLEEP and STOP modes (oscillator remains running from crystal but XOSC clock output disabled).

7 RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripherals enabled, both cores running, and running a typical application using both SRAM and flash.

[8] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal; all peripheral and cores enabled and running a typical application using both SRAM and flash. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature.

[9] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripheral and cores enabled and running a typical application using both SRAM and flash. Only for 208 MAPBGA and only 120C junction or lower. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature

Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut}	12.8	16	22.3	MHz
2	Frequency after loading factory trim[2]	F_t	15.1	16	16.9	MHz
3	Application trim resolution[3]	T_s	—	—	± 0.5	%
4	Application frequency trim step[3]	F_s	—	300	—	kHz
5	Start up time	S_t	—	—	500	ns

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut32}	20.8	32.0	43.2	kHz
2	Frequency after loading factory trim[2]	F_{t32}	26	32.0	38	kHz
3	Application trim resolution[3]	T_{s32}	—	—	± 2	%
4	Application frequency trim step[3]	F_{s32}	—	1	—	kHz
5	Start up time	S_{t32}	—	—	100	µs

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

2.11 Flash Memory Electrical Characteristics

Table 16. Flash Program and Erase Specifications[1]

Num	Characteristic	Symbol	Min	Typ	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time [4]	$T_{dwprogram}$	—	10	—	500	µs
2	Page (128 bits) Program Time [4]	$T_{pprogram}$	—	15	44	500	µs
3	16 Kbyte Block Pre-program and Erase Time	$T_{16kpperase}$	—	325	525	5000	ms
4	64 Kbyte Block Pre-program and Erase Time	$T_{64kpperase}$	—	525	675	5000	ms
5	128 Kbyte Block Pre-program and Erase Time	$T_{128kpperase}$	—	675	1800	7500	ms
6	Minimum operating frequency for program and erase operations	—	25	—	—	—	MHz
7	Wait States Relative to System Frequency PFCRPn[RWSC] = 0b000; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b001; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b010; PFCRPn[WWSC] = 0b01	T_{rwsc}	 — — —	 — — —	 — — —	 25 50 80	MHz
8	Recovery Time Stop mode exit or STOP bit negated Sleep mode exit (with CRP_RECPTR[FASTREC]=1) [5]	$T_{recover}$	 — —	 — —	 — —	 20 120	 µs µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, nomial supply values and operation at 25 °C.

3 The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 This does not include software overhead.

5 If CRP_RECPTR[FASTREC]=0, then hardware will wait 2340 system clocks before exiting from Sleep mode to account for the flash recovery time. The default system clock source after Sleep is the 16MIRC. A nominal frequency of 16MHz equates to a hardware wait of 146µs.

Table 17. Flash EEPROM Module Life (Full Temperature Range)

Num	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of Program/Erase cycles per block over the operating temperature range (T_J) 16 Kbyte and 64 Kbyte blocks 128 Kbyte blocks	P/E	 100,000 1000	 — 100,000	cycles
2	Data retention Blocks with 0 – 1,000 P/E cycles Blocks with 1,001 – 100,000 P/E cycles	Retention	 20 5	—	years

1 Typical endurance is evaluated at 25C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619 “Typical Endurance for Nonvolatile Memory.”

2.12 Pad AC Specifications

Table 18. Pad AC Specifications (VDDE = 3.0V - 5.5V)[1]

Num	Pad Type	SRC	Out Delay[2, 3] (ns)	Rise/Fall[3, 4] (ns)	Load Drive (pF)
1	Slow (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9500	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at VDDE = 3.0V to 5.5V, T_A = TL to TH.

2 This parameter is supplied for reference and is not tested. Add a maximum of one system clock to the output delay for delay with respect to system clock.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

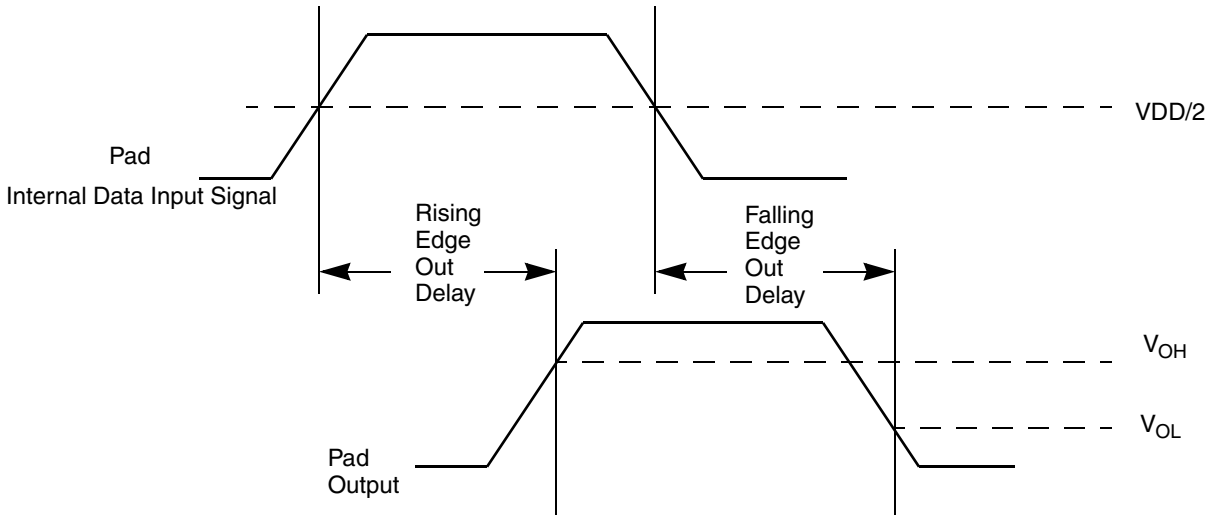


Figure 5. Pad Output Delay

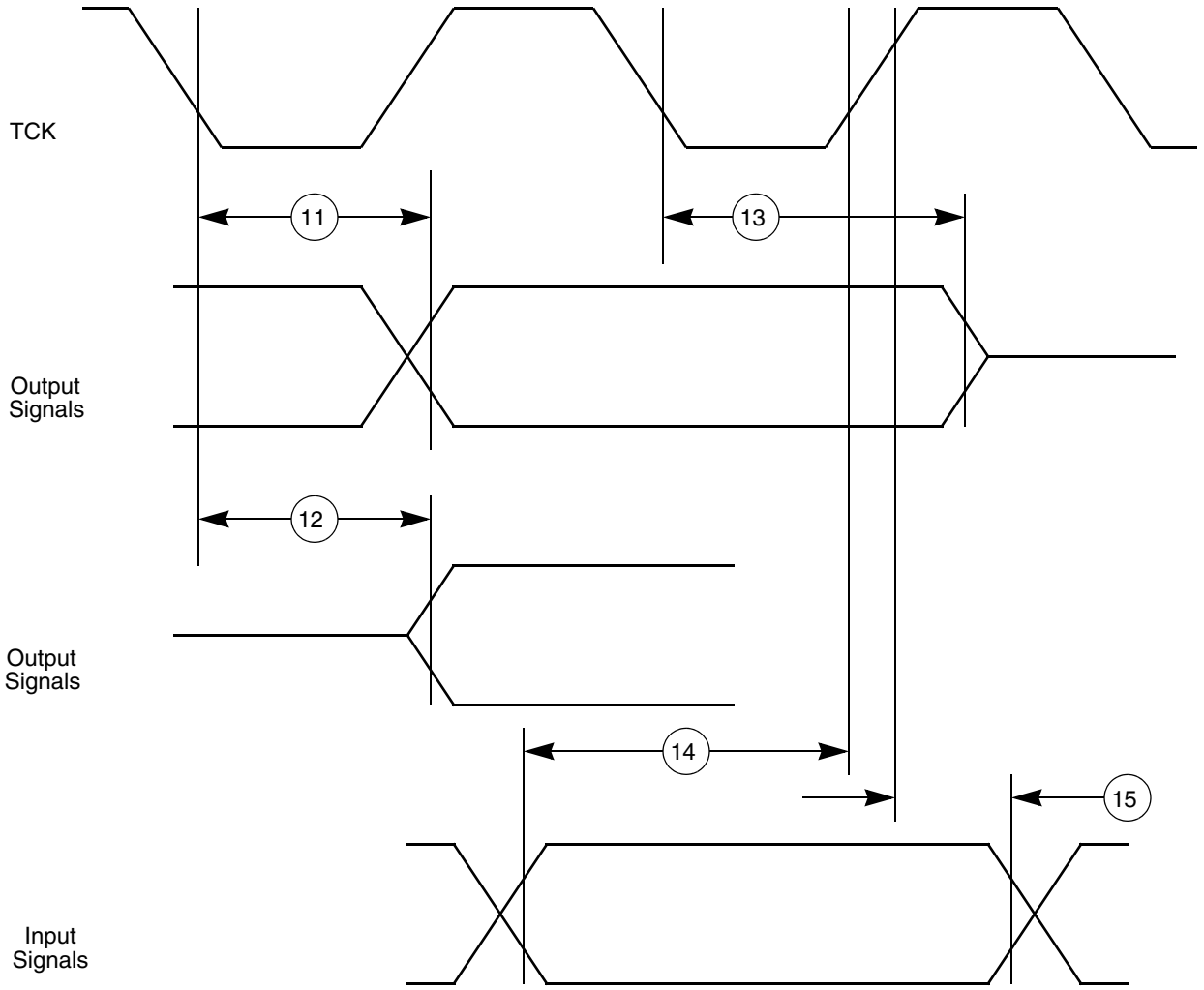


Figure 11. JTAG Boundary Scan Timing

2.13.4 Nexus Debug Interface

Table 22. Nexus Debug Port Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	40	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–2	4.0	ns
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–2	4.0	ns
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–2	4.0	ns
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
8	TCK Cycle Time[3]	t_{TCYC}	40	—	ns
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	4	—	ns
12	TCK Low to TDO Data Valid	t_{JOV}	0	8	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster that the TCK frequency.

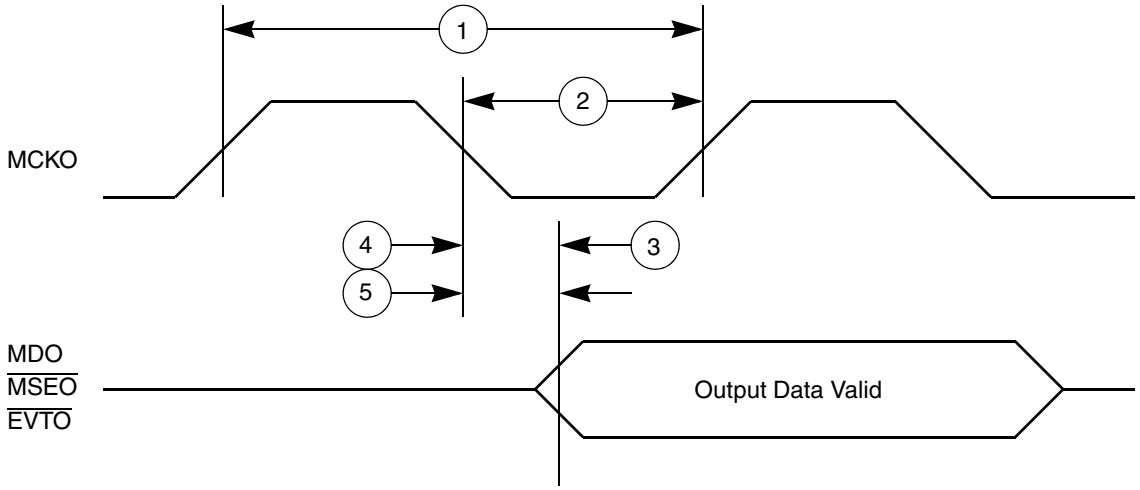


Figure 12. Nexus Output Timing

2.13.5 External Bus Interface (EBI)

Table 23. External Bus Operation Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	CLKOUT Period[2]	T_C	40.0	—	ns
2	CLKOUT duty cycle	t_{CDC}	45%	55%	T_C
3	CLKOUT rise time	t_{CRT}	—	—[3]	ns
4	CLKOUT fall time	t_{CFT}	—	—[3]	ns
5	CLKOUT Positive Edge to Output Signal Invalid or High Z (Hold Time)	t_{COH}	2.0	—	ns
6	CLKOUT Positive Edge to Output Signal Valid (Output Delay)	t_{COV}	—	10.0	ns
7	Input Signal Valid to CLKOUT Posedge (Setup Time)	t_{CIS}	20.0	—	ns
8	CLKOUT Posedge to Input Signal Invalid (Hold Time)	t_{CIH}	0	—	ns
9	ALE Pulse Width High Time	t_{ALEPWH}	20	—	ns
10	ALE Fall to AD Invalid	t_{ALEAD}	2	—	ns

1 EBI timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 50pF with SIU_PCR*n*[SRC] = 0b11.

2 Initialize SIU_ECCR[EBDF] to meet maximum external bus frequency.

3 Refer to Medium High Voltage (MH) pad AC specification in Table 18.

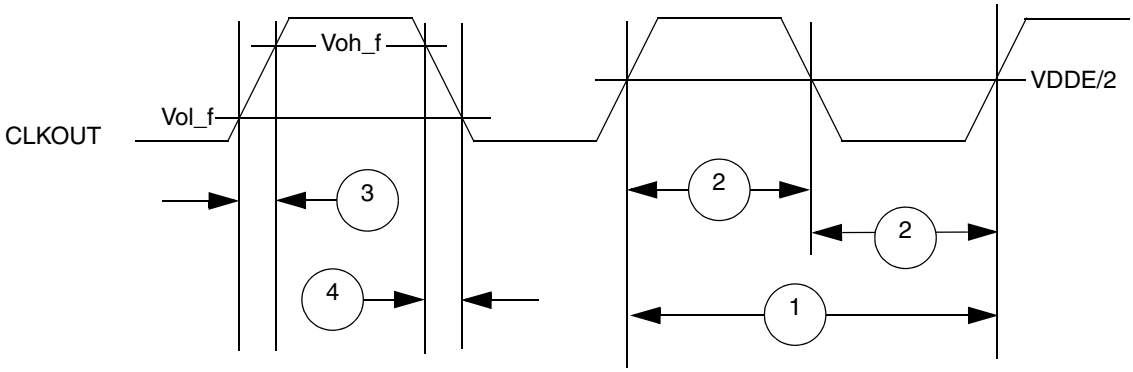


Figure 14. CLKOUT Timing

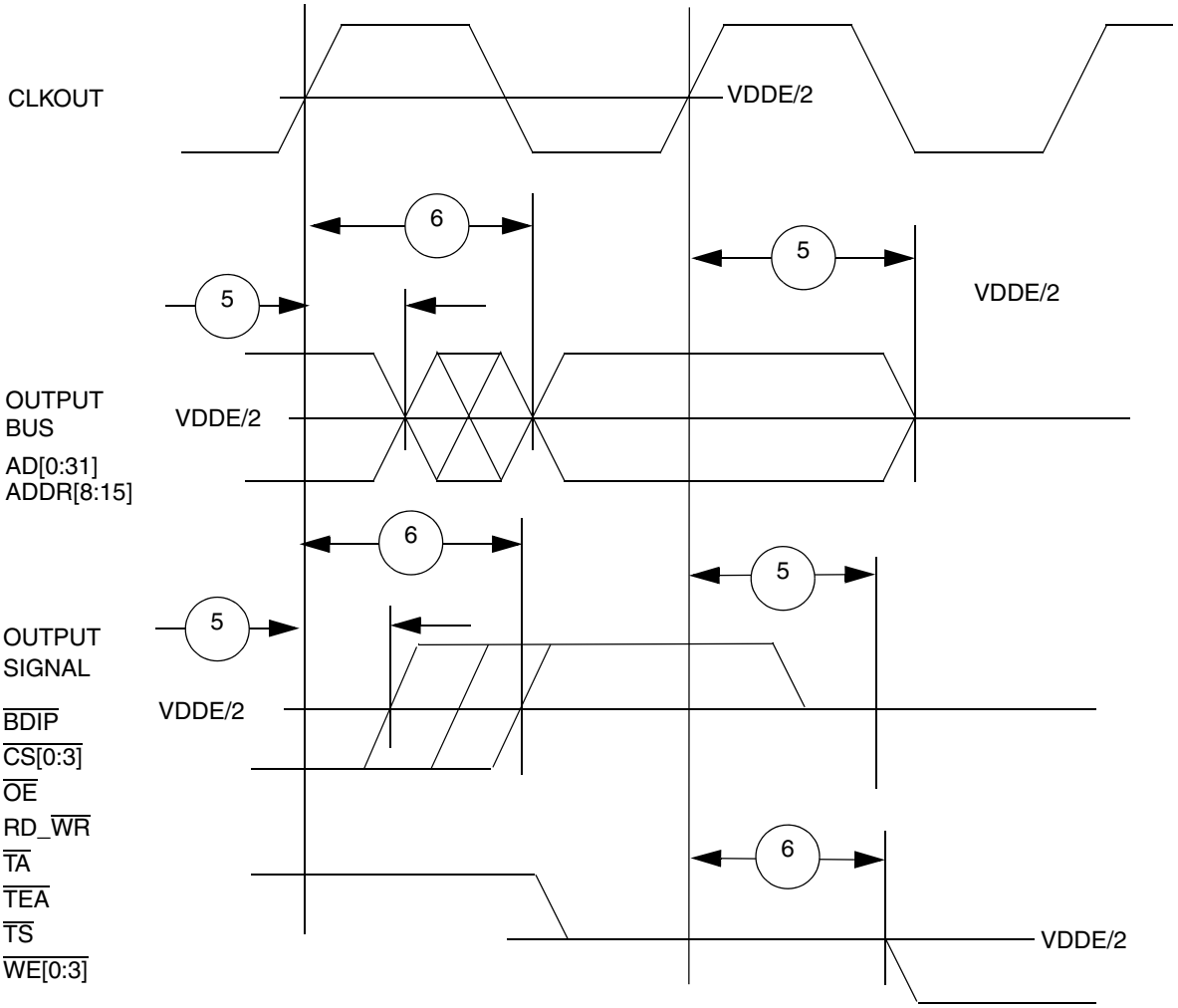


Figure 15. Synchronous Output Timing