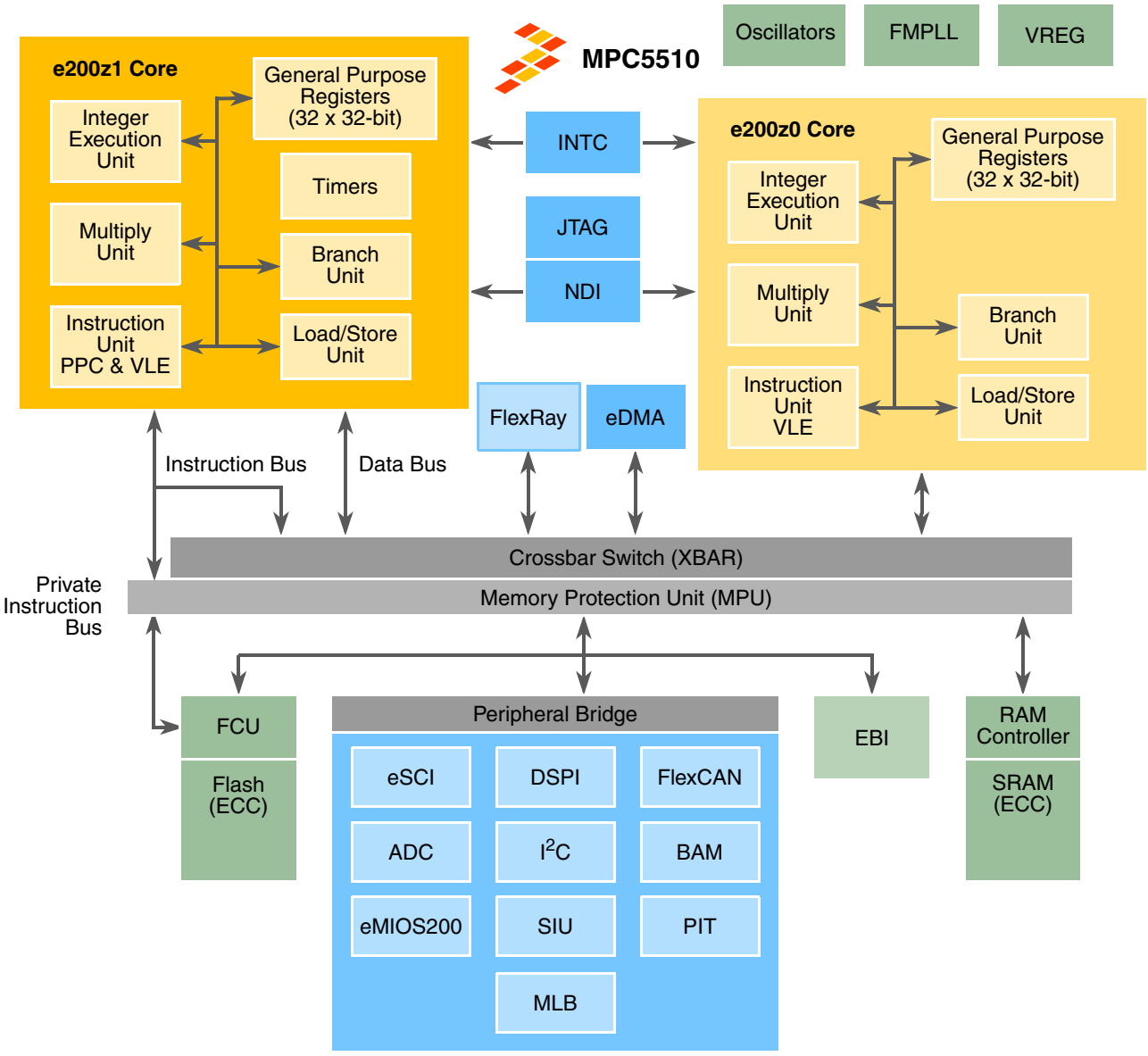
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0, e200z1
Core Size	32-Bit Dual-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	137
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5517eavlu66



LEGEND

ADC	– Analog to Digital Converter modules	**FlexRay**	– Dual Channel FlexRay controller
BAM	– Boot Assist Module	**FMPLL**	– Frequency Modulated Phase Locked Loop module
EBI	– External Bus Interface module	**I^2C**	– Inter IC Controller modules
ECC	– Error Correction Code	**INTC**	– Interrupt Controller module
DSPI	– Serial Peripherals Interface controller module	**JTAG**	– Joint Test Action Group interface
eDMA	– enhanced Direct Memory Controller module	**MLB**	– Media Local Bus emulation logic
eMIOS200	– Timed Input Output module	**NDI**	– Nexus Debug Interface module
eSCI	– Serial Communications Interface modules	**PIT**	– Periodic Interrupt Timer module
FCU	– Flash Controller Unit	**SIU**	– System Integration module
FlexCAN	– Controller Area Network controller modules	**VREG**	– Voltage Regulator

Figure 1. MPC5510 Family Block Diagram

1 Pin Assignments and Reset States

1.1 Signal Properties and Multiplexing Summary

Table 1 shows the signal properties for each pin on the MPC5510. For all port pins, which have an associated pad configuration register (SIU_PCR*n* register) to control its pin properties, the "Supported Pin Functions" column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, Function1, Function2 and Function3. If fewer than three functions plus GPIO are supported by a given pin, then the unused functions begin with Function3, then Function2, then Function1. Note that the GPIO number is the same number as the corresponding pad configuration register (SIU_PCR*n*) number.

Table 1. MPC5510 Signal Properties

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
Port A (16)											
PA0	0	PA0 AN0	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	9	9	E3
PA1	1	PA1 AN1	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	8	8	E2
PA2	2	PA2 AN2	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	7	7	E1
PA3	3	PA3 AN3	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	6	6	D3
PA4	4	PA4 AN4	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	5	5	D2
PA5	5	PA5 AN5	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	4	4	D1
PA6	6	PA6 AN6	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	3	3	C2
PA7	7	PA7 AN7	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	2	2	C1
PA8	8	PA8 AN8/ANW	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	143	175	A3
PA9	9	PA9 AN9/ANX	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	142	174	C4
PA10	10	PA10 AN10/ANY	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	140	172	D5
PA11	11	PA11 AN11/ANZ	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	139	171	C5
PA12	12	PA12 AN12	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	138	170	B5
PA13	13	PA13 AN13	GPI eQADC Analog Input	I I	V_{DDA}	AE + IH	—	—	137	169	A5
PA14	14	PA14 AN14 EXTAL32[6]	GPI eQADC Analog Input 32 kHz Crystal Oscillator Input	I I I	V_{DDA}	AE + IH	—	—	136	167	D6

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PC10	42	PC10 eMIOS10 PCS_C5 SCK_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Clock	I/O I/O O I/O	V_{DDE1}	SH	—	—	110	134	A14
PC11	43	PC11 eMIOS11 PCS_C4 SOUT_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial Out	I/O I/O O O	V_{DDE1}	SH	—	—	109	133	B14
PC12	44	PC12 eMIOS12 PSC_C3 SIN_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial In	I/O I/O O I	V_{DDE1}	SH	—	—	108	132	B16
PC13	45	PC13 eMIOS13 PCS_A5 PCS_D0	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	107	131	C15
PC14	46	PC14 eMIOS14 PCS_A4 PCS_D1	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	106	130	C16
PC15	47	PC15 eMIOS15 PCS_A3 PCS_D2	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	105	129	D14
Port D (16)											
PD0	48	PD0 CNTX_A PCS_D3	GPIO CAN_A Transmit DSPI_D Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	104	128	D15
PD1	49	PD1 CNRX_A PCS_D4	GPIO CAN_A Receive DSPI_D Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	103	127	D16
PD2	50	PD2 CNRX_B eMIOS10 BOOTCFG PCS_D5	GPIO CAN_B Receive eMIOS Channel Boot Configuration DSPI_D Peripheral Chip Select	I/O I O I O	V_{DDE1}	SH	BOOTCFG (Pulldown)	GPI (Pulldown)	102	126	E14
PD3	51	PD3 CNTX_B eMIOS11	GPIO CAN_B Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	101	125	E15
PD4	52	PD4 CNTX_C eMIOS12	GPIO CAN_C Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	100	124	E16
PD5	53	PD5 CNRX_C eMIOS13	GPIO CAN_C Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	99	123	F13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PE3	67	PE3 SCK_A eMIOS2 MLBSO / MLBSIG_BUFEN	GPIO DSPI_A Clock eMIOS Channel MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin)	I/O I/O O O O	V_{DDE1}	MH	—	—	83	100	M13
PE4	68	PE4 SOUT_A eMIOS1 MLBDO / MLBDAT_BUFEN	GPIO DSPI_A Data Out eMIOS Channel MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin)	I/O O O O O	V_{DDE1}	MH	—	—	82	98	N14
PE5	69	PE5 SIN_A eMIOS0 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS	GPIO DSPI_A Data In eMIOS Channel MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data	I/O I O O O O	V_{DDE1}	MH	—	—	81	97	M15
PE6	70	PE6 CLKOUT	GPIO System Clock Output	I/O O	V_{DDE3}	MH	—	—	67	83	P13
PE7	71	PE7	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H13
PE8	72	PE8	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H16
PE9	72	PE9	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	J13
PE10	74	PE10	GPIO	I/O	V_{DDE1}	SH	—	—	—	112	J16
PE11	75	PE11	GPIO	I/O	V_{DDE1}	SH	—	—	—	111	J15
PE12	76	PE12	GPIO	I/O	V_{DDE1}	SH	—	—	—	109	K13
PE13	77	PE13	GPIO	I/O	V_{DDE1}	SH	—	—	—	108	L13
PE14	78	PE14	GPIO	I/O	V_{DDE1}	SH	—	—	—	102	L16
PE15	79	PE15	GPIO	I/O	V_{DDE1}	SH	—	—	—	99	M14
Port F (16)											
PF0	80	PF0 RD_$\overline{WR}$ EVTI[8]	GPIO EBI Read/Write Nexus Event In	I/O I/O I	V_{DDE3}	MH	—	—	66	82	N12
PF1	81	PF1 $\overline{TA}$ MLBCLK EVTO[8]	GPIO EBI Transfer Acknowledge MLB Clock Nexus Event Out	I/O I/O I O	V_{DDE3}	MH	—	—	65	81	P12
PF2	82	PF2 AD8 ADDR8 MLBSI / MLBSIG $\overline{MSEO}$[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal In (5-pin) / MLB Bi-Directional Signal (3-pin) Nexus Message Start/End Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	64	80	R12

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{TS}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	5.0V Voltage Regulator Reference Voltage	V_{DDR}	– 0.3	6.5	V
2	5.0V Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	– 0.3	6.5	V
3	5.0V Flash Program/Erase Voltage	V_{PP}	– 0.3	6.5	V
4	3.3V – 5.0V External I/O Supply Voltage [3]	V_{DDE1}[4] V_{DDE2}[4] V_{DDE3}[4]	– 0.3 – 0.3 – 0.3	6.5 6.5 6.5	V
5	DC Input Voltage [5]	V_{IN}	–1.0[6]	6.5[7]	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 0.3	5.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 5.5	5.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 0.3	0.3	V
9	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	$- V_{DDA}$	0.3	V
10	Maximum DC Digital Input Current [8] (per pin, applies to all digital MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
11	Maximum DC Analog Input Current [9] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
12	Storage Temperature Range	T_{STG}	– 55.0	150.0	°C
13	Maximum Solder Temperature [10]	T_{SDR}	—	260.0	°C
14	Moisture Sensitivity Level [11]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn–in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 AC signal over and undershoot of the input voltages of up to +/– 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

6 Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

7 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25mA.

9 Total injection current for all analog input pins must not exceed 15mA.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 4. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	176 LQFP	144 LQFP
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	44	38	43
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	27	31	34
3	Junction to Ambient [1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	35	30	34
4	Junction to Ambient [1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	24	25	28
5	Junction to Board [4]	$R_{\theta JB}$	°C/W	16	20	22
6	Junction to Case [5]	$R_{\theta JC}$	°C/W	8	6	7
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	°C/W	2	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package } (^oC) \quad \textit{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance } (^oC/W) \quad \textit{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \textit{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

2.3 ESD Characteristics

Table 5. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut}	12.8	16	22.3	MHz
2	Frequency after loading factory trim[2]	F_t	15.1	16	16.9	MHz
3	Application trim resolution[3]	T_s	—	—	± 0.5	%
4	Application frequency trim step[3]	F_s	—	300	—	kHz
5	Start up time	S_t	—	—	500	ns

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut32}	20.8	32.0	43.2	kHz
2	Frequency after loading factory trim[2]	F_{t32}	26	32.0	38	kHz
3	Application trim resolution[3]	T_{s32}	—	—	± 2	%
4	Application frequency trim step[3]	F_{s32}	—	1	—	kHz
5	Start up time	S_{t32}	—	—	100	µs

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

2.9 FMPLL Electrical Characteristics

Table 14. FMPLL Electrical Specifications [1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	System frequency[2] -40 °C ≤ T_J ≤ 120 °C -40 °C ≤ T_J ≤ 145 °C	f_{sys}	 375 375	 80000 [3] 66000	kHz
2	PLL Reference Frequency (output of predivider)	f_{pllref}	4	10	MHz
3	VCO Frequency[4]	f_{vco}	250	500	MHz
4	PLL Frequency [5] -40 °C ≤ T_J ≤ 120 °C -40 °C ≤ T_J ≤ 145 °C	f_{pll}	 3 3	 80 [3] 66	MHz
5	Loss of Reference Frequency [6]	f_{LOR}	100	1000	kHz
6	Self Clocked Mode Frequency [7]	f_{SCM}	13	35	MHz
7	PLL Lock Time [8]	t_{lpll}	—	750	µs
8	Frequency un-LOCK Range	f_{UL}	– 4.0	4.0	% f_{sys}
9	Frequency LOCK Range	f_{LCK}	– 2.0	2.0	% f_{sys}
10	CLKOUT Cycle-to-cycle Jitter,[9, 10]	C_{jitter}	– 5	5	% f_{clkout}
10a	CLKOUT Jitter at 10 µs period [9,10, 11]	C_{jitter}	– 0.05	0.05	% f_{clkout}
11	Frequency Modulation Depth 1% Setting [12,13] (f_{sys}Max must not be exceeded)	C_{mod}	0.5	2	%f_{sys}
12	Frequency Modulation Depth 2% Setting [12,13] (f_{sys}Max must not be exceeded)	C_{mod}	1	3	%f_{sys}

1 V_{DDSYN} = 3.0V to 3.6 V, V_{SSSYN} = 0 V, TA = TL to TH

2 The maximum value is without frequency modulation turned on. If frequency modulation is turned on, the maximum value (average frequency) must be de-rated by the percentage of modulation enabled.

3 80 MHz is only available in the 208 pin package.

4 Optimum performance is achieved with the highest VCO frequency feasible based on the highest ERFD that results in the desired PLL frequency.

5 The VCO frequency range is higher than the maximum allowable PLL frequency. The synthesizer control register 2's enchanced reduced frequency divider (FMPLL_SYNCR2[ERFD]) in enhanced operation mode must be programmed to divide the VCO frequency within the PLL frequency range.

6 Loss of reference frequency is the reference frequency detected by the PLL which then transitions into self clocked mode.

7 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}.

8 This specification applies to the period required for the PLL to relock after changing the enhanced multiplication factor divider (EMFD) bits in the synthesizer control register 1 (SYNCR1) in enhanced operation mode.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider set to divide-by-2.

10 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

11 The PLL % jitter reduces with more cycles. 10 µs was picked for a reference point for LIN (100 Kbits), slower speeds will have even less % jitter.

12 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

13 These depth ranges are obtained by filtering the raw cycle-to-cycle clock frequency data to eliminate the presence of the the normal clock jitter riding on top of the FM waveform. The allowable modulation rates are 400 kHz to 1 MHz.

2.11 Flash Memory Electrical Characteristics

Table 16. Flash Program and Erase Specifications[1]

Num	Characteristic	Symbol	Min	Typ	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time [4]	$T_{dwprogram}$	—	10	—	500	µs
2	Page (128 bits) Program Time [4]	$T_{pprogram}$	—	15	44	500	µs
3	16 Kbyte Block Pre-program and Erase Time	$T_{16kpperase}$	—	325	525	5000	ms
4	64 Kbyte Block Pre-program and Erase Time	$T_{64kpperase}$	—	525	675	5000	ms
5	128 Kbyte Block Pre-program and Erase Time	$T_{128kpperase}$	—	675	1800	7500	ms
6	Minimum operating frequency for program and erase operations	—	25	—	—	—	MHz
7	Wait States Relative to System Frequency PFCRPn[RWSC] = 0b000; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b001; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b010; PFCRPn[WWSC] = 0b01	T_{rwsc}	 — — —	 — — —	 — — —	 25 50 80	MHz
8	Recovery Time Stop mode exit or STOP bit negated Sleep mode exit (with CRP_RECPTR[FASTREC]=1) [5]	$T_{recover}$	 — —	 — —	 — —	 20 120	 µs µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, nomial supply values and operation at 25 °C.

3 The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 This does not include software overhead.

5 If CRP_RECPTR[FASTREC]=0, then hardware will wait 2340 system clocks before exiting from Sleep mode to account for the flash recovery time. The default system clock source after Sleep is the 16MIRC. A nominal frequency of 16MHz equates to a hardware wait of 146µs.

Table 17. Flash EEPROM Module Life (Full Temperature Range)

Num	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of Program/Erase cycles per block over the operating temperature range (T_J) 16 Kbyte and 64 Kbyte blocks 128 Kbyte blocks	P/E	 100,000 1000	 — 100,000	cycles
2	Data retention Blocks with 0 – 1,000 P/E cycles Blocks with 1,001 – 100,000 P/E cycles	Retention	 20 5	—	years

1 Typical endurance is evaluated at 25C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619 “Typical Endurance for Nonvolatile Memory.”

2.12 Pad AC Specifications

Table 18. Pad AC Specifications (VDDE = 3.0V - 5.5V)[1]

Num	Pad Type	SRC	Out Delay[2, 3] (ns)	Rise/Fall[3, 4] (ns)	Load Drive (pF)
1	Slow (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
4	Pull Up/Down (3.6V max)	—	—	7500	50
5	Pull Up/Down (5.5V max)	—	—	9500	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at VDDE = 3.0V to 5.5V, T_A = TL to TH.

2 This parameter is supplied for reference and is not tested. Add a maximum of one system clock to the output delay for delay with respect to system clock.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

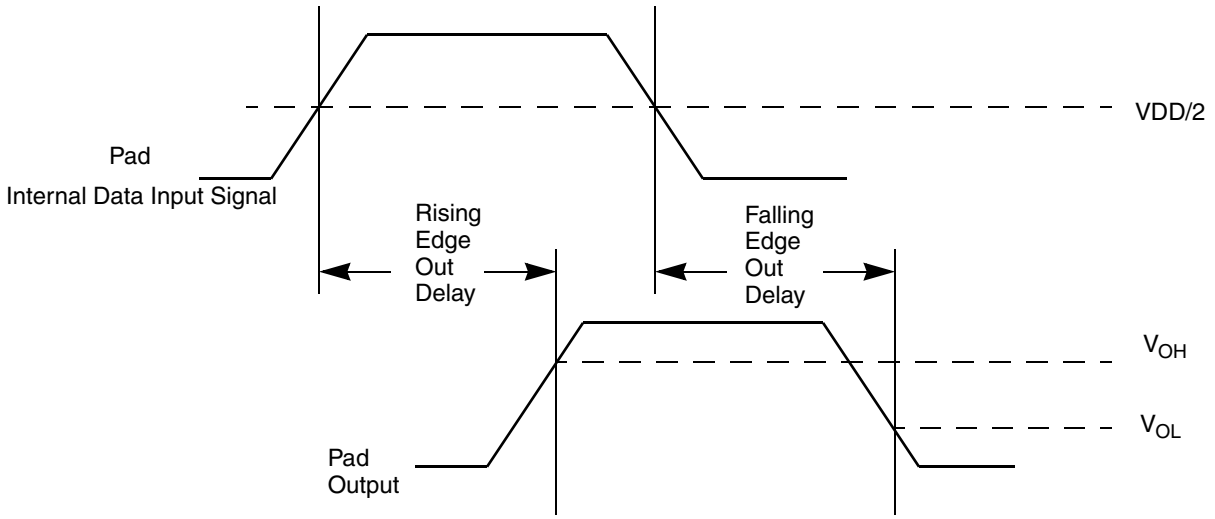


Figure 5. Pad Output Delay

2.13 AC Timing

2.13.1 Reset and Boot Configuration Pins

Table 19. Reset and Boot Configuration Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

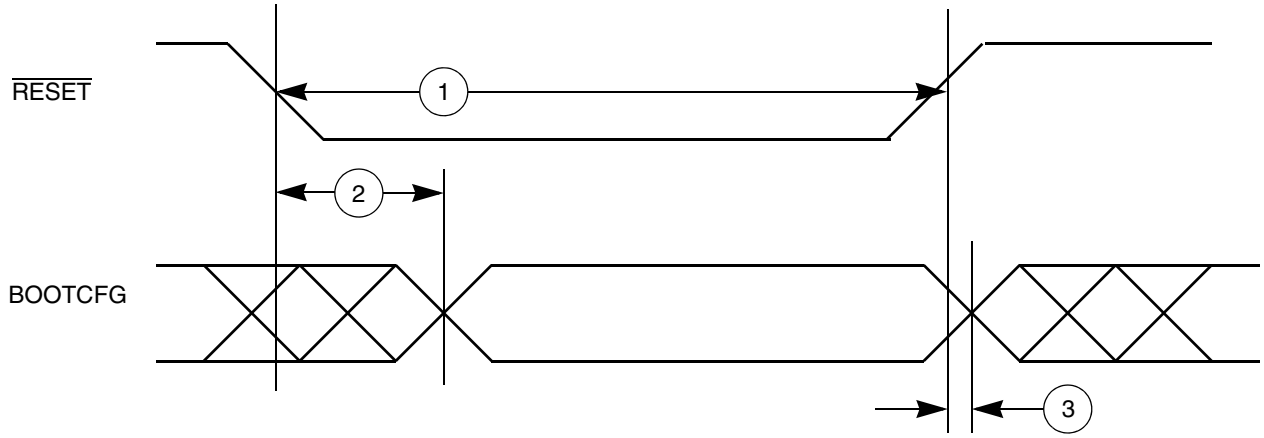


Figure 6. Reset and Boot Configuration Timing

2.13.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 20. IRQ/NMI Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

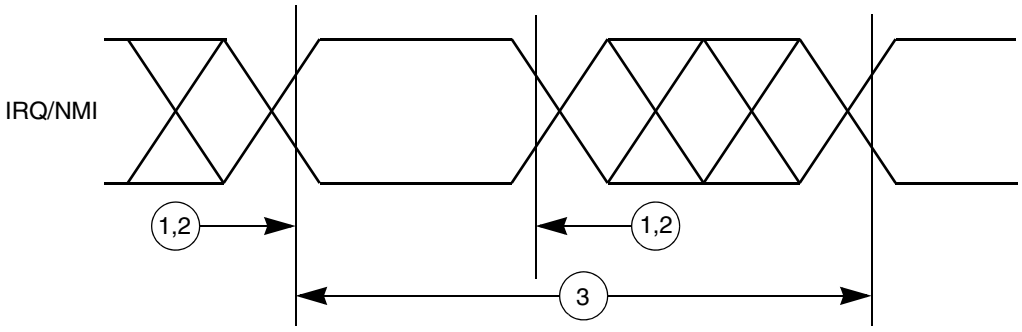


Figure 7. IRQ and NMI Timing

2.13.3 JTAG (IEEE 1149.1) Interface

Table 21. JTAG Interface Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at VDDE/2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	20	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

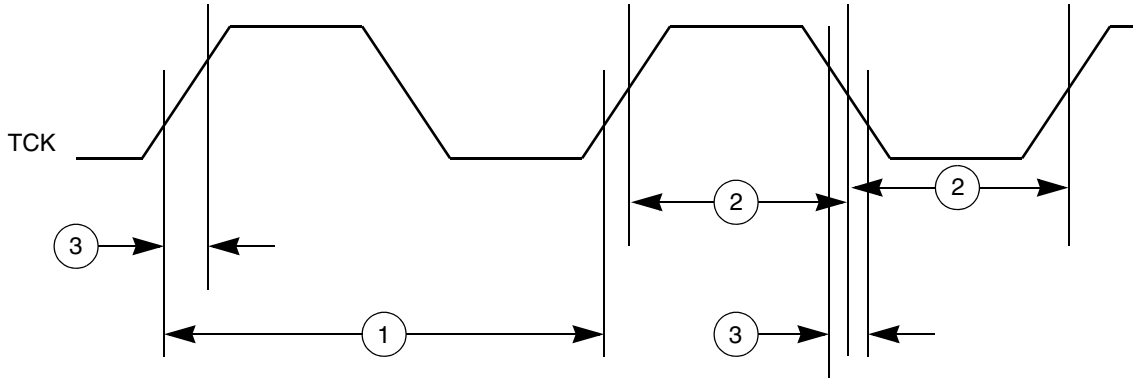


Figure 8. JTAG Test Clock Input Timing

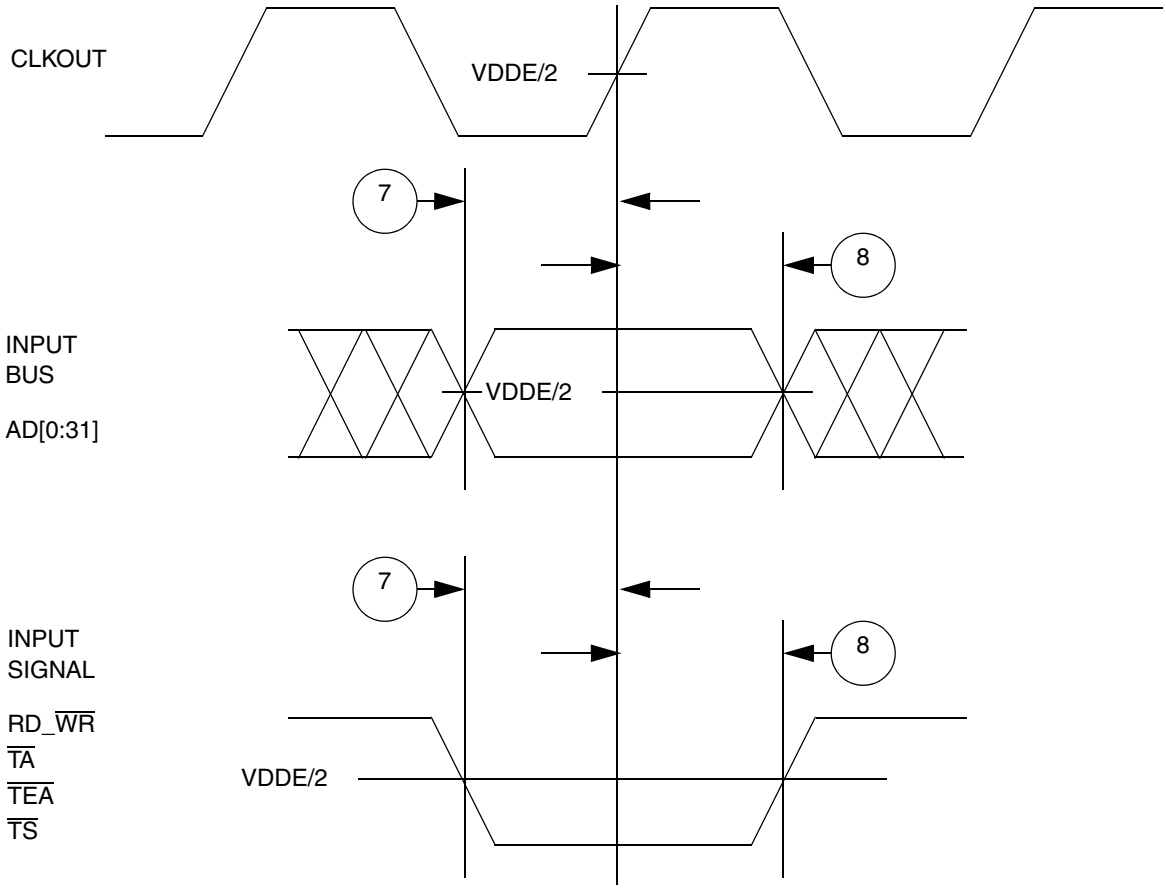


Figure 16. Synchronous Input Timing

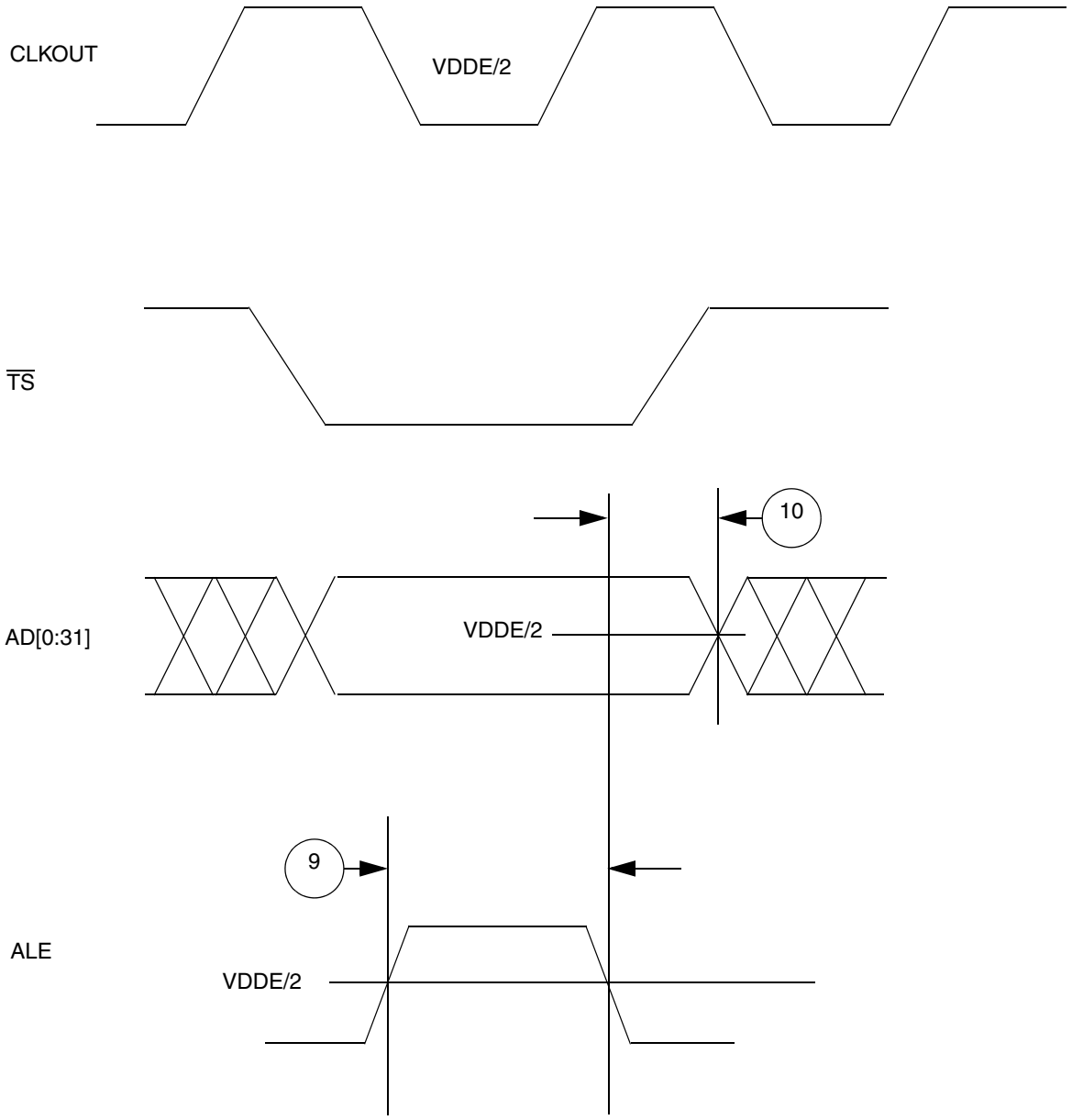


Figure 17. Address Latch Enable (ALE) Timing

2.13.6 Enhanced Modular I/O Subsystem (eMIOS)

Table 24. eMIOS Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1	—	t_{CYC}

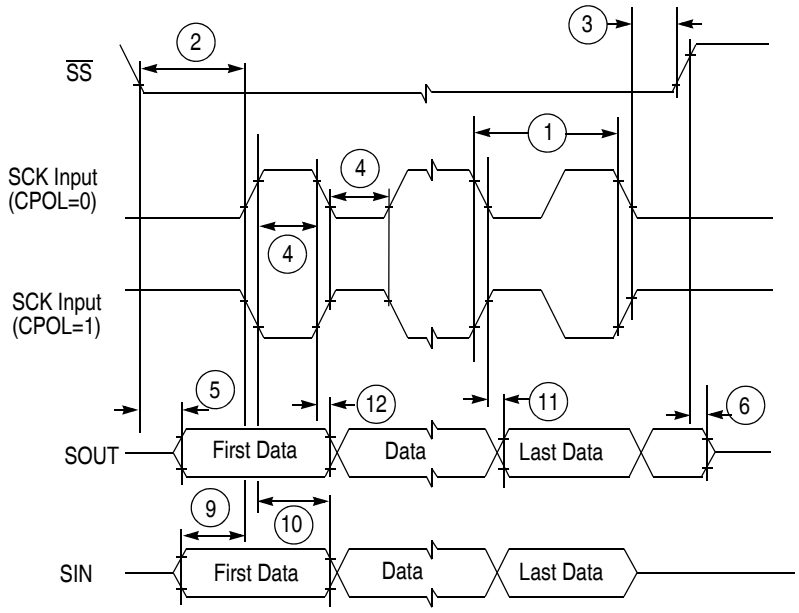


Figure 20. DSPI Classic SPI Timing — Slave, CPHA = 0

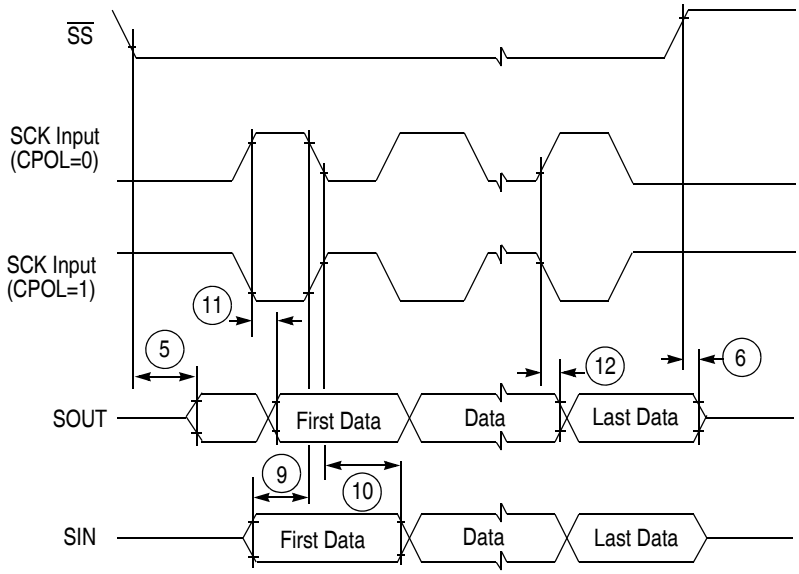


Figure 21. DSPI Classic SPI Timing — Slave, CPHA = 1

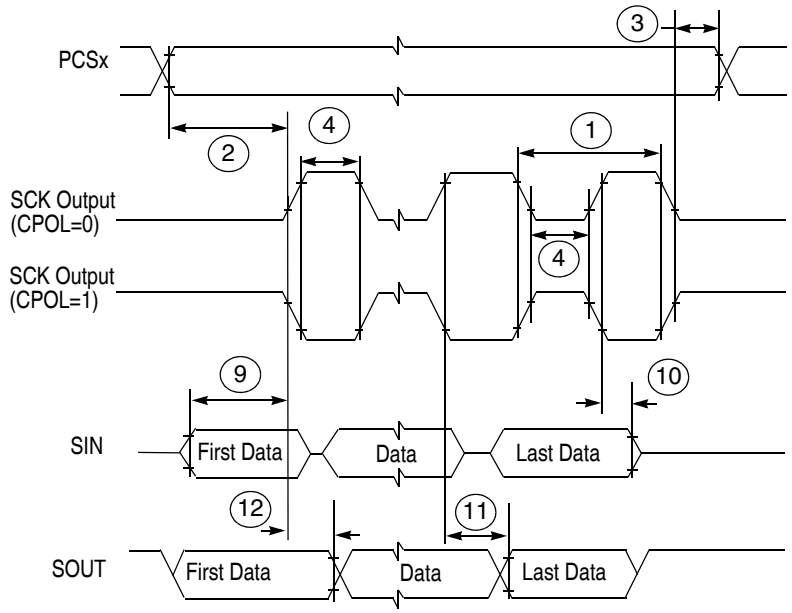


Figure 22. DSPI Modified Transfer Format Timing — Master, CPHA = 0

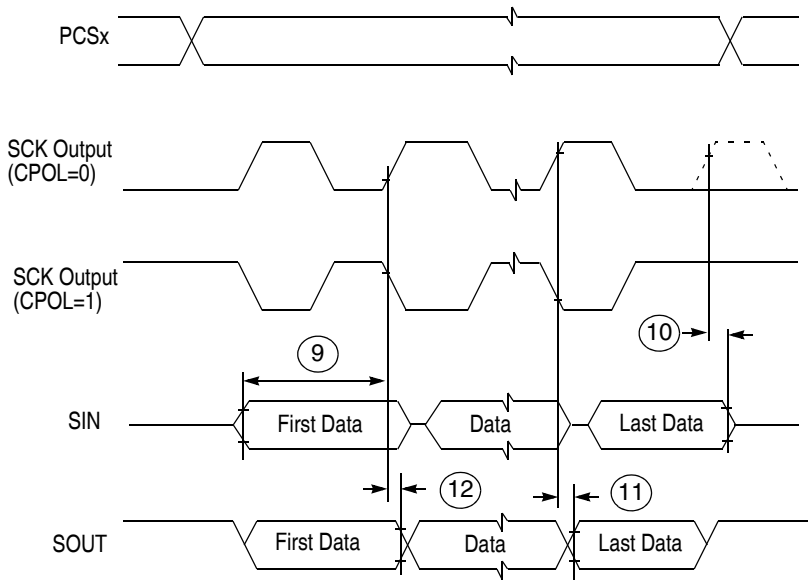


Figure 23. DSPI Modified Transfer Format Timing — Master, CPHA = 1

3 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/powerpc. The following table lists the package case number per device. Use these numbers in the web page's "keyword" search engine to find the latest package outline drawings.

Table 26. Package Information

Package	Package Case Number
144 LQFP	98ASS23177W
176 LQFP	98ASS23479W
208 MAPBGA	98ARS23882W

4 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/powerpc.

4.1 Revision History

Table 27 summarizes revisions to this document.

Table 27. Revision History of MPC5510 Data Sheet

Revision	Date	Substantive Changes
Rev. 0	9/2007	Initial Release. Preliminary content.
Rev. 1	6/2008	(Note: Change descriptions refer to locations in Rev. 0.) Changed MPC5516 to MPC5510 Family where appropriate. Modified Figure 1. MPC5510 Family Block Diagram. Deleted Table 1. MPC5510 Family Comparison, Maximum Feature Set Deleted Table 2. MPC5510 Peripheral Multiplexing Examples Corrected PK0 and PK1 pin assignments on 208 MAPBGA (Table 3 and Figure 4). Modified Table 4, footnote 4. Modified Table 8. DC Electrical Specifications and table footnotes. Modified Table 9. Operating Currents and table footnotes. Modified Table 12. 3.3V High Frequency External Oscillator, row 5. Modified Table 14. 5V High Frequency (16 MHz) Internal RC Oscillator, row 2. Modified Table 16. FMPLL Electrical Specifications, row 4. Modified Table 17. eQADC Conversion Specifications (Operating) and table footnotes. Modified Table 18. Flash Program and EraseSpecifications, row 5. Modified Table 19. Flash EEPROM Module Life (Full Temperature Range), row 1 Modified Table 28. Package Information.
Rev. 2	12/2008	(Note: Change descriptions refer to locations in Rev. 1.) Modified Table 1. MPC5510 Signal Properties: added note to TEST signal. Modified Table 6. DC Electrical Specifications: rows 1b, 5, 8, 9, 10, 11, 16, 19, 25, and footnotes. Modified Table 7. Operating Currents: Max column header, rows 1, 2, 3, 4, and footnotes. Modified Table 9. Low Voltage Monitors: rows 2, 3, 4, 6. Modified Table 10. 3.3V High Frequence External Oscillator: row 1 added footnote, removed duplicate footnote #3. Modified Table 11. 5V Low Frequency (32 kHz) External Oscillator: row 1. Modified Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator: row 2. Modified Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator: row 2. Modified Table 14. FMPLL Electrical Specifications: rows 1 and 4; added two new rows. Modified Table 15. eQADC Conversion Specifications (Operating): rows 5, 6, 7, 8, 10, 11, and footnotes. Modified Figure 5. Pad Output Delay: moved the dashed horizontal line up so that it crosses the signal midway between top and bottom.
Rev. 3	3/2009	(Note: Change descriptions refer to locations in Rev. 2.) Modified Table 4. Thermal Characteristics: all values in 208 MAPBGA column. Modified Table 6. DC Electrical Specifications: spec #1c, added footnote; spec #25, added footnote. Modified Table 7. Operating Currents; spec #5. Modified Table 9. Low Voltage Monitors; spec #1. Modified Table 14. FMPLL Electrical Specifications: updated footnote 3; added spec #10a. Modified Table 15. eQADC Conversion Specifications (Operating): added another footnote. Modified Table 16: Flash Program and Erase Specifications: updated spec #7. Modified Figure 5: Pad Output Delay: adjusted lower timing diagram. Modified Figure 8: JTAG Test Clock Input Timing; updated so that it matches the spec definitions.
Rev. 4	7/2014	Updated the VCO Min. value from 192 to 250 MHz in Table 14., “FMPLL Electrical Specifications.