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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0, e200z1
Core Size	32-Bit Dual-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5517ebvlq66

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Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V_{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V_{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX $\overline{TS}$	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V_{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V_{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PD6	54	PD6 TXD_A eMIOS14	GPIO SCI_A Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	98	122	F14
PD7	55	PD7 RXD_A eMIOS15	GPIO SCI_A Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	97	121	F15
PD8	56	PD8 TXD_B SCL_A	GPIO SCI_B Transmit I^2C Serial Clock Line	I/O O I/O	V_{DDE1}	SH	—	—	94	118	G13
PD9	57	PD9 RXD_B SDA_A	GPIO SCI_B Receive I^2C Serial Data Line	I/O I I/O	V_{DDE1}	SH	—	—	93	117	F16
PD10	58	PD10 PCS_B2 CNTX_F NMI0	GPIO DSPI_B Peripheral Chip Select CAN_F Transmit NMI Input for Z1 Core	I/O O O I	V_{DDE1}	SH	—	—	92	116	G14
PD11	59	PD11 PCS_B1 CNRX_F NMI1	GPIO DSPI_B Peripheral Chip Select CAN_F Receive NMI Input for Z0 Core	I/O O I I	V_{DDE1}	SH	—	—	91	115	G15
PD12	60	PD12 PCS_B0 eMIOS9	GPIO DSPI_B Peripheral Chip Select eMIOS Channel	I/O I/O O	V_{DDE1}	SH	—	—	90	114	H14
PD13	61	PD13 SCK_B eMIOS8	GPIO DSPI_B Clock eMIOS Channel	I/O I/O O	V_{DDE1}	SH	—	—	89	113	H15
PD14	62	PD14 SOUT_B eMIOS7	GPIO DSPI_B Data Output eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	88	110	J14
PD15	63	PD15 SIN_B eMIOS6	GPIO DSPI_B Data Input eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	87	107	K14
Port E (16)											
PE0	64	PE0 PCS_A2 eMIOS5 MLBCLK	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Clock	I/O O O I	V_{DDE1}	SH	—	—	86	106	K16
PE1	65	PE1 PCS_A1 eMIOS4 MLBSI / MLBSIG	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Signal In (5-pin) / MLB Bi-directional Signal (3-pin)	I/O O O I I/O	V_{DDE1}	MH	—	—	85	103	L14
PE2	66	PE2 PCS_A0 eMIOS3 MLBDI / MLBDAT	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Data In (5-pin) / MLB Bi-directional Data (3-pin)	I/O I/O O I I/O	V_{DDE1}	MH	—	—	84	101	L15

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{TS}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V_{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V_{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V_{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V_{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V_{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Clock	I/O I O I/O	V_{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Data	I/O I O I/O	V_{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 $\overline{CS3}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 $\overline{CS2}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input[7] SCI_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input[7] SCI_E Receive eQADC External Mux Address	I/O I I O	V_{DDE2}	A + SH	—	—	19	24	J3

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PH6	118	PH6 AN21 TXD_F	GPIO eQADC Analog Input[7] SCI_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	18	23	J2
PH7	119	PH7 AN20 RXD_F	GPIO eQADC Analog Input[7] SCI_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	17	22	J1
PH8	120	PH8 AN19 CNTX_E MA0	GPIO eQADC Analog Input[7] CAN_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	14	17	H1
PH9	121	PH9 AN18/ANT CNRX_E	GPIO eQADC Analog Input[7] CAN_E Receive	I/O I I	V_{DDE2}	A + SH	—	—	13	14	G2
PH10	122	PH10 AN17/ANS CNRX_F	GPIO eQADC Analog Input[7] CAN_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	12	12	F4
PH11	123	PH11 AN16/ANR CNTX_F	GPIO eQADC Analog Input[7] CAN_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	11	11	F3
PH12	124	PH12 PCS_D5	GPIO DSPI_D Peripheral Chip Select	I/O O	V_{DDE2}	SH	—	—	—	—	F2
PH13	125	PH13	GPIO	I/O	V_{DDE2}	SH	—	—	—	—	F1
PH14	126	PH14 $\overline{WE2}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	53	T5
PH15	127	PH15 $\overline{WE3}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	52	R5
Port J (16)											
PJ0	128	PJ0 AD0	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N11
PJ1	129	PJ1 AD1	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	P11
PJ2	130	PJ2 AD2	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N10
PJ3	131	PJ3 AD3	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	R10
PJ4	132	PJ4 AD4	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	75	P10
PJ5	133	PJ5 AD5	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	73	T9
PJ6	134	PJ6 AD6	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	69	P9
PJ7	135	PJ7 AD7	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	67	R8

1.5 Pinout – 208 PBGA

Figure 4. MPC5510 Pinout – 208 PBGA

device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 14}$$

where:

T_T = thermocouple temperature on top of the package (^oC) *Eqn. 15*

Ψ_{JT} = thermal characterization parameter ($^oC/W$) *Eqn. 16*

P_D = power dissipation in the package (W) *Eqn. 17*

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

2.3 ESD Characteristics

Table 5. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

[8] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal; all peripheral and cores enabled and running a typical application using both SRAM and flash. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature.

[9] RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripheral and cores enabled and running a typical application using both SRAM and flash. Only for 208 MAPBGA and only 120C junction or lower. Be sure to calculate the junction temperature, as the maximum current at maximum ambient temperature can exceed the maximum junction temperature

2.6 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 8 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 8.

Table 8. I/O Pad Average DC Current[1]

Num	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Slew Rate Control	Current (mA)
1	Slow (Pad Type SH)	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium (Pad Type MH)	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9

1 These values are estimated from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

2.8 Oscillators Electrical Characteristics

Table 10. 3.3V High Frequency External Oscillator

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	Frequency Range[1]	f_{ref}	4[2]	40	MHz
2	Duty Cycle of reference	t_{dc}	40	60	%
3	EXTAL Input High Voltage External crystal mode [3] External clock mode	V_{IHEXT}	 V_{XTAL} + 0.4 0.65 x V_{DDSYN}	 V_{DDSYN} + 0.3 V_{DDSYN} + 0.3	V
4	EXTAL Input Low Voltage External crystal mode [3] External clock mode	V_{ILEXT}	 V_{DDSYN} – 0.3 V_{DDSYN} – 0.3	 V_{XTAL} – 0.4 0.35 x V_{DDSYN}	V
5	XTAL Current [4]	I_{XTAL}	2	6	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	3	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	3	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2\times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[5]	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2\times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[5]	pF
11	Startup Time	$t_{startup}$	—	10	ms

1 Since this is an amplitude controlled oscillator the use of overtone oscillators is not recommended. Only use fundamental frequency oscillators.

2 When PLL frequency modulation is active, reference frequencies less than 8MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400mV$ criteria has to be met for oscillator's comparator to produce output clock.

4 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

5 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively

Table 11. 5V Low Frequency (32 kHz) External Oscillator

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	Frequency Range	f_{ref32}	32	38	kHz
2	Duty Cycle of reference	t_{dc32}	40	60	%
3	XTAL32 Current [1]	I_{XTAL32}	0.5	3	µA
4	Crystal manufacturer's recommended capacitive load	C_{L32}	See crystal specification	See crystal specification	pF
5	Startup Time	$t_{startup}$	—	2	s

1 I_{xtal32} is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

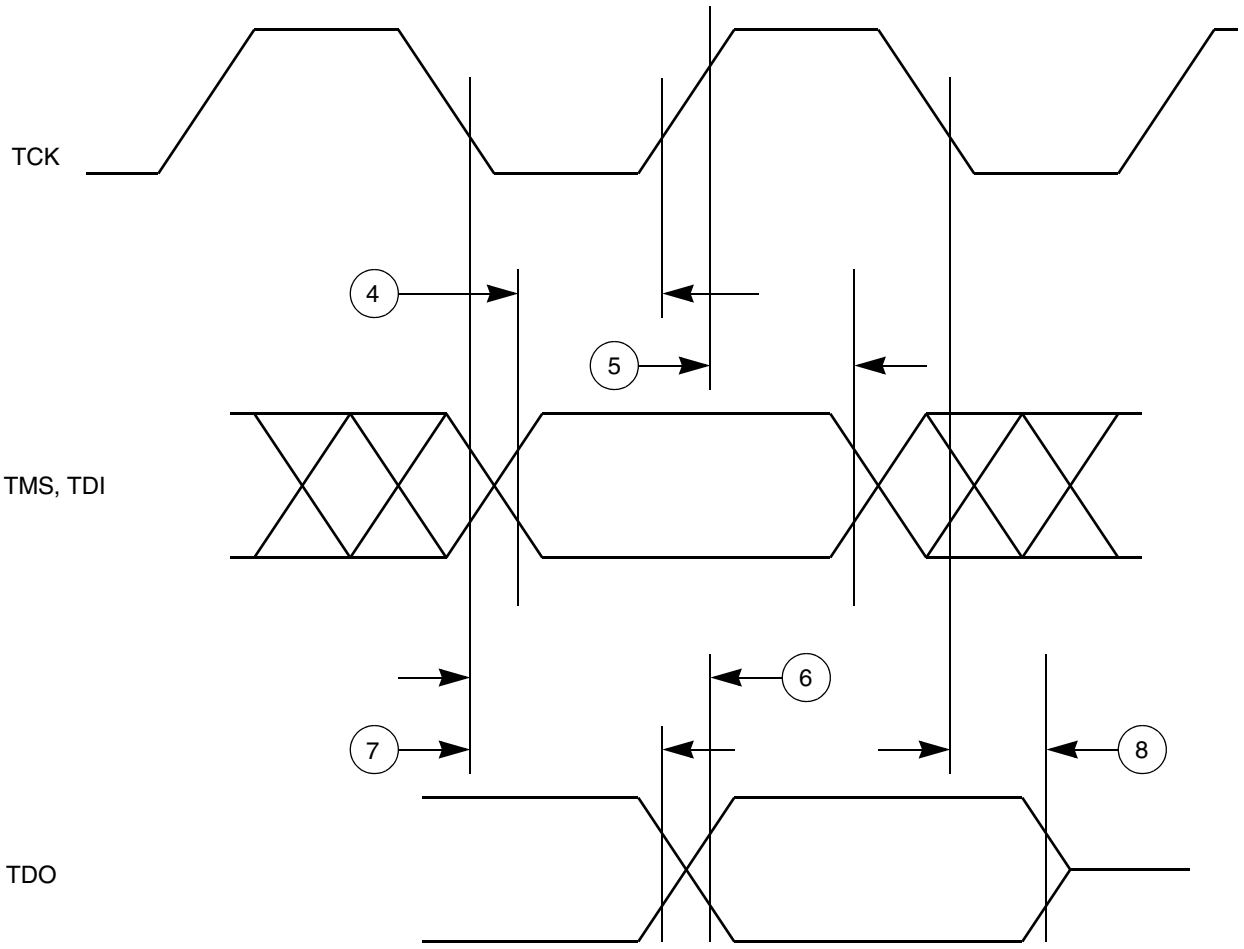

Figure 9. JTAG Test Access Port Timing

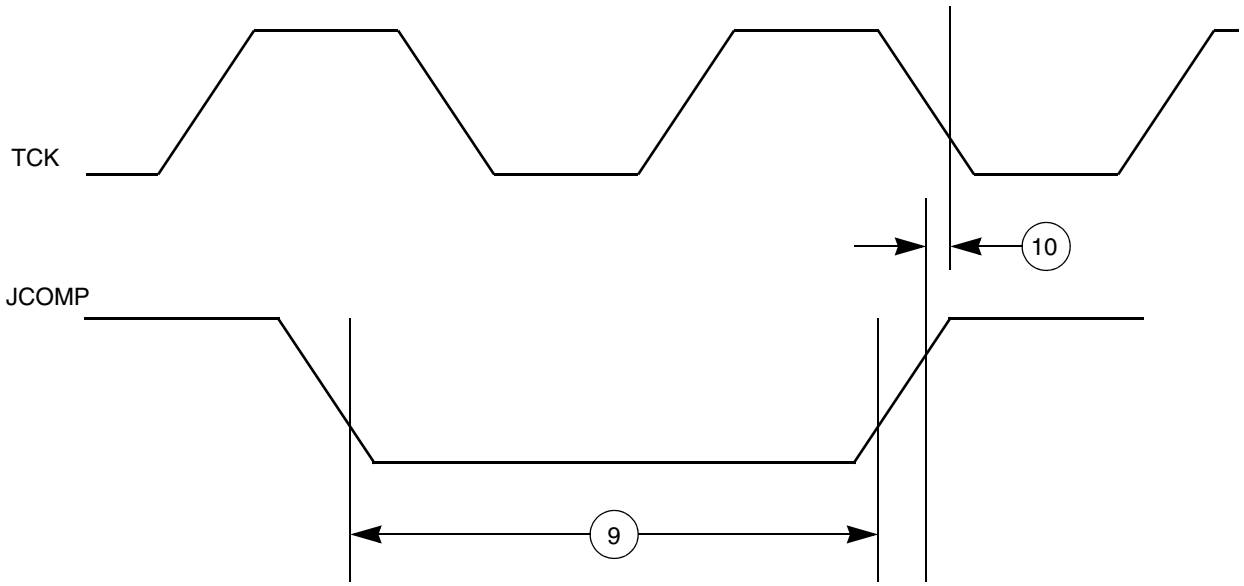

Figure 10. JTAG JCOMP Timing

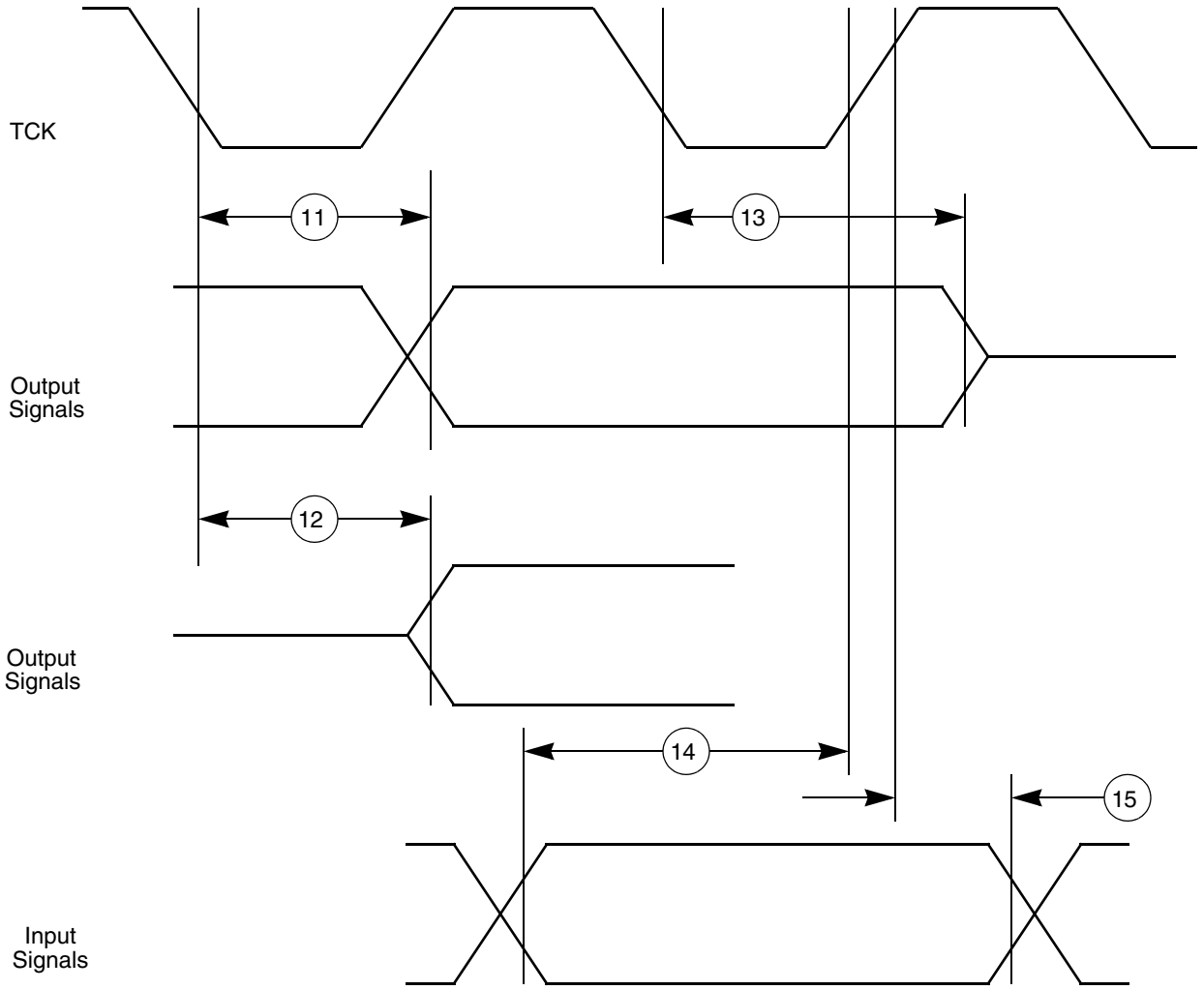

Figure 11. JTAG Boundary Scan Timing

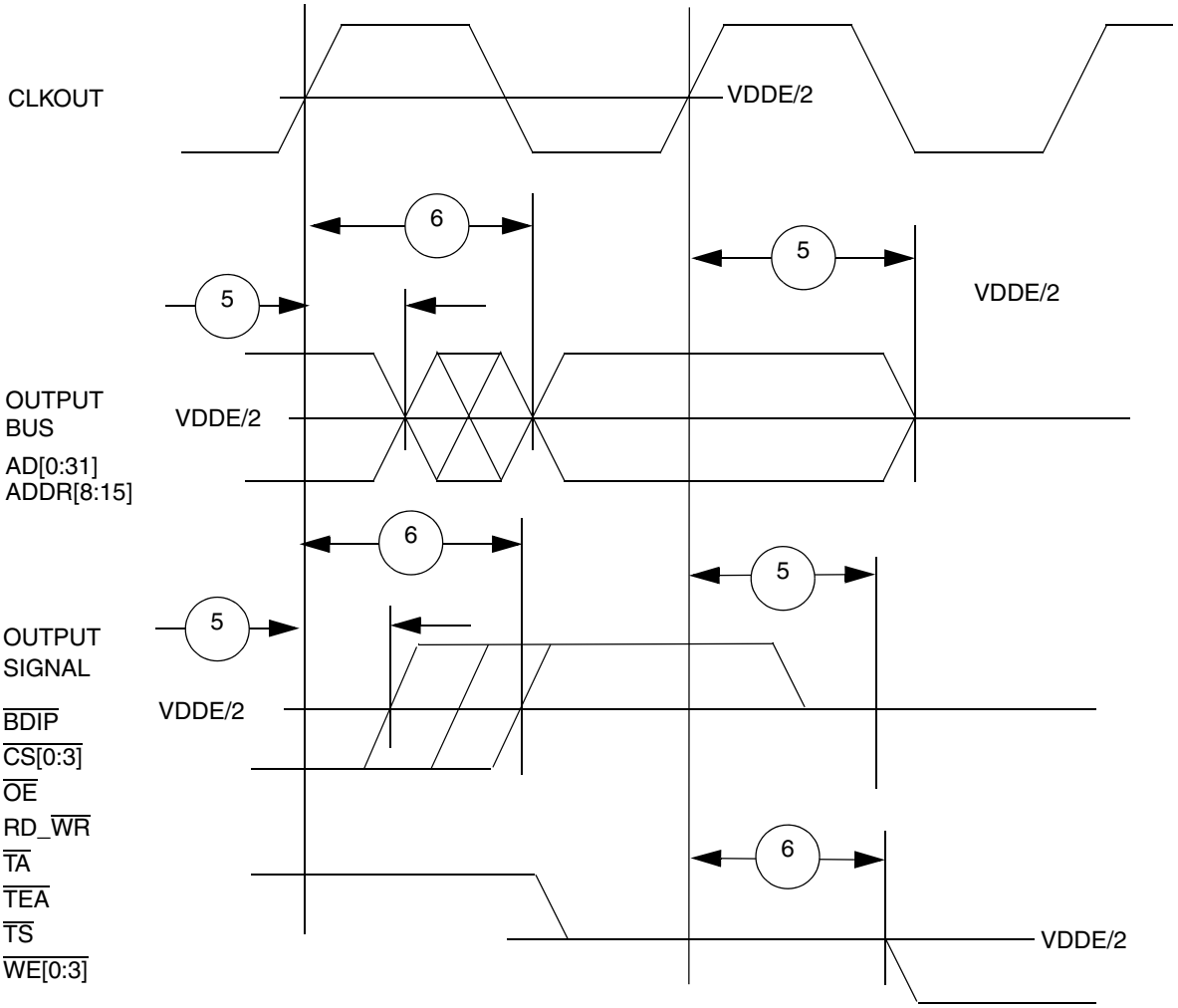

Figure 15. Synchronous Output Timing

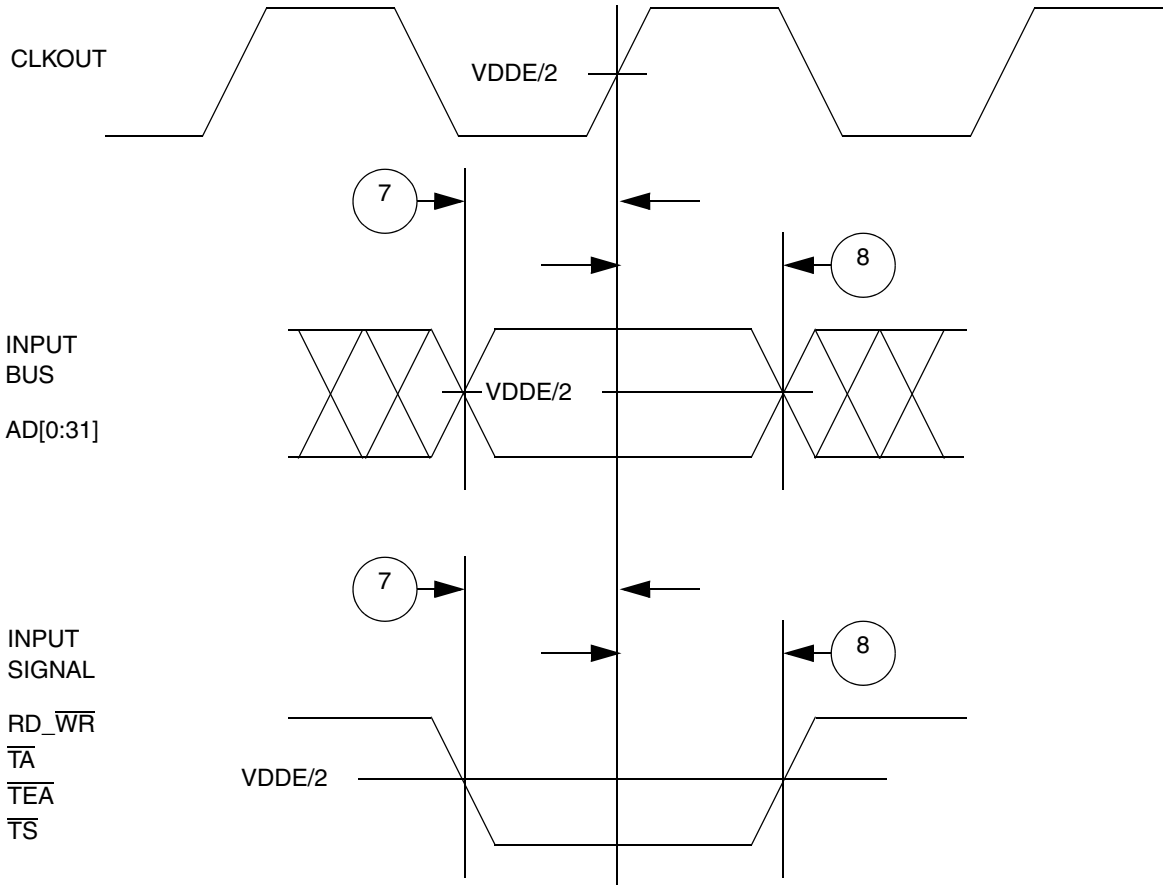

Figure 16. Synchronous Input Timing

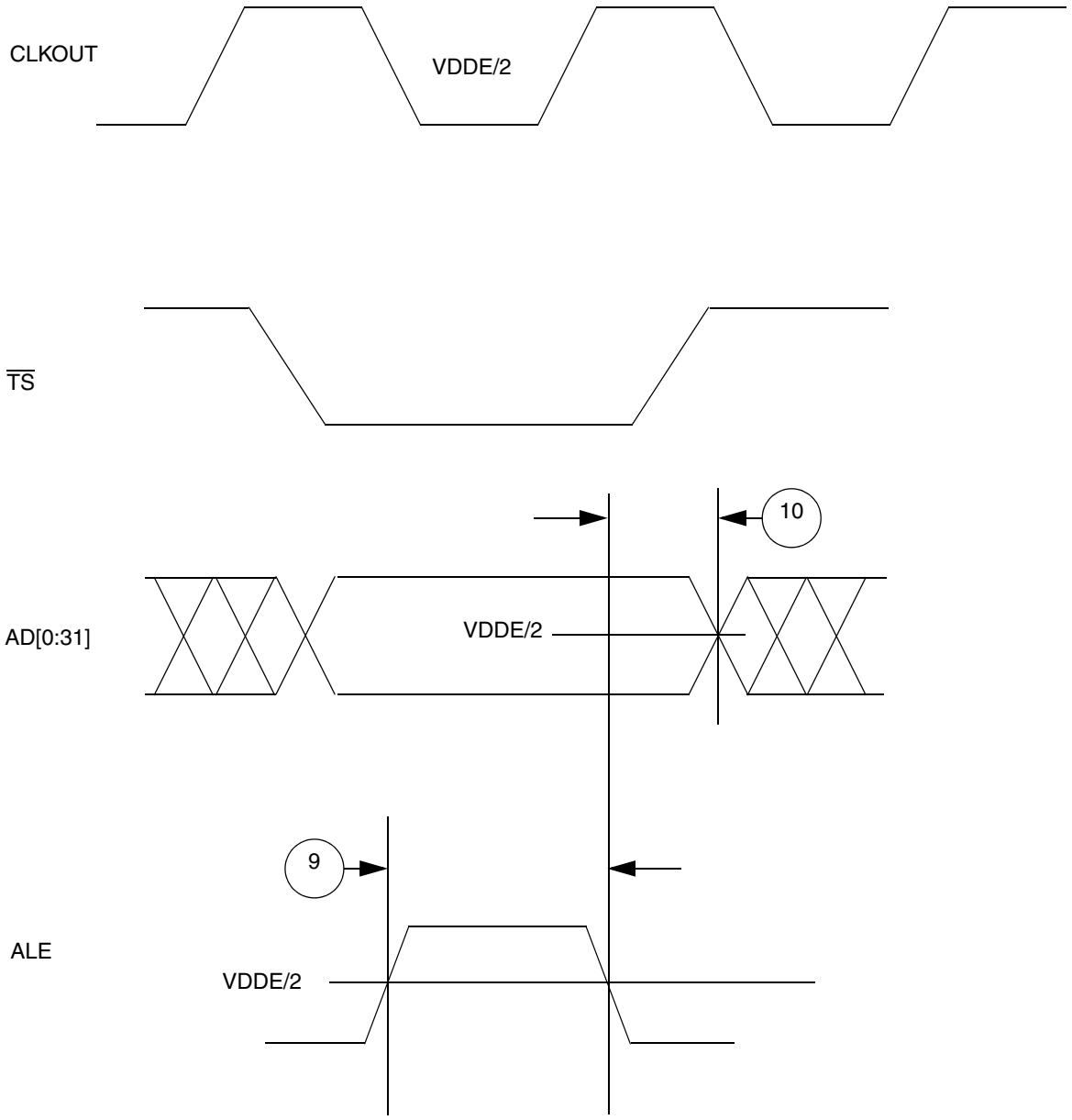

Figure 17. Address Latch Enable (ALE) Timing

2.13.6 Enhanced Modular I/O Subsystem (eMIOS)

Table 24. eMIOS Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1	—	t_{CYC}

3 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/powerpc. The following table lists the package case number per device. Use these numbers in the web page's "keyword" search engine to find the latest package outline drawings.

Table 26. Package Information

Package	Package Case Number
144 LQFP	98ASS23177W
176 LQFP	98ASS23479W
208 MAPBGA	98ARS23882W

4 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/powerpc.

4.1 Revision History

Table 27 summarizes revisions to this document.

Table 27. Revision History of MPC5510 Data Sheet

Revision	Date	Substantive Changes
Rev. 0	9/2007	Initial Release. Preliminary content.
Rev. 1	6/2008	(Note: Change descriptions refer to locations in Rev. 0.) Changed MPC5516 to MPC5510 Family where appropriate. Modified Figure 1. MPC5510 Family Block Diagram. Deleted Table 1. MPC5510 Family Comparison, Maximum Feature Set Deleted Table 2. MPC5510 Peripheral Multiplexing Examples Corrected PK0 and PK1 pin assignments on 208 MAPBGA (Table 3 and Figure 4). Modified Table 4, footnote 4. Modified Table 8. DC Electrical Specifications and table footnotes. Modified Table 9. Operating Currents and table footnotes. Modified Table 12. 3.3V High Frequency External Oscillator, row 5. Modified Table 14. 5V High Frequency (16 MHz) Internal RC Oscillator, row 2. Modified Table 16. FMPLL Electrical Specifications, row 4. Modified Table 17. eQADC Conversion Specifications (Operating) and table footnotes. Modified Table 18. Flash Program and EraseSpecifications, row 5. Modified Table 19. Flash EEPROM Module Life (Full Temperature Range), row 1 Modified Table 28. Package Information.
Rev. 2	12/2008	(Note: Change descriptions refer to locations in Rev. 1.) Modified Table 1. MPC5510 Signal Properties: added note to TEST signal. Modified Table 6. DC Electrical Specifications: rows 1b, 5, 8, 9, 10, 11, 16, 19, 25, and footnotes. Modified Table 7. Operating Currents: Max column header, rows 1, 2, 3, 4, and footnotes. Modified Table 9. Low Voltage Monitors: rows 2, 3, 4, 6. Modified Table 10. 3.3V High Frequence External Oscillator: row 1 added footnote, removed duplicate footnote #3. Modified Table 11. 5V Low Frequency (32 kHz) External Oscillator: row 1. Modified Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator: row 2. Modified Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator: row 2. Modified Table 14. FMPLL Electrical Specifications: rows 1 and 4; added two new rows. Modified Table 15. eQADC Conversion Specifications (Operating): rows 5, 6, 7, 8, 10, 11, and footnotes. Modified Figure 5. Pad Output Delay: moved the dashed horizontal line up so that it crosses the signal midway between top and bottom.
Rev. 3	3/2009	(Note: Change descriptions refer to locations in Rev. 2.) Modified Table 4. Thermal Characteristics: all values in 208 MAPBGA column. Modified Table 6. DC Electrical Specifications: spec #1c, added footnote; spec #25, added footnote. Modified Table 7. Operating Currents; spec #5. Modified Table 9. Low Voltage Monitors; spec #1. Modified Table 14. FMPLL Electrical Specifications: updated footnote 3; added spec #10a. Modified Table 15. eQADC Conversion Specifications (Operating): added another footnote. Modified Table 16: Flash Program and Erase Specifications: updated spec #7. Modified Figure 5: Pad Output Delay: adjusted lower timing diagram. Modified Figure 8: JTAG Test Clock Input Timing; updated so that it matches the spec definitions.
Rev. 4	7/2014	Updated the VCO Min. value from 192 to 250 MHz in Table 14., “FMPLL Electrical Specifications.

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Document Number: MPC5510
Rev. 4
7/2014