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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0, e200z1
Core Size	32-Bit Dual-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5517ebvlq66r

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V_{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V_{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX $\overline{TS}$	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V_{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V_{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PC10	42	PC10 eMIOS10 PCS_C5 SCK_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Clock	I/O I/O O I/O	V_{DDE1}	SH	—	—	110	134	A14
PC11	43	PC11 eMIOS11 PCS_C4 SOUT_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial Out	I/O I/O O O	V_{DDE1}	SH	—	—	109	133	B14
PC12	44	PC12 eMIOS12 PSC_C3 SIN_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial In	I/O I/O O I	V_{DDE1}	SH	—	—	108	132	B16
PC13	45	PC13 eMIOS13 PCS_A5 PCS_D0	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	107	131	C15
PC14	46	PC14 eMIOS14 PCS_A4 PCS_D1	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	106	130	C16
PC15	47	PC15 eMIOS15 PCS_A3 PCS_D2	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	105	129	D14
Port D (16)											
PD0	48	PD0 CNTX_A PCS_D3	GPIO CAN_A Transmit DSPI_D Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	104	128	D15
PD1	49	PD1 CNRX_A PCS_D4	GPIO CAN_A Receive DSPI_D Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	103	127	D16
PD2	50	PD2 CNRX_B eMIOS10 BOOTCFG PCS_D5	GPIO CAN_B Receive eMIOS Channel Boot Configuration DSPI_D Peripheral Chip Select	I/O I O I O	V_{DDE1}	SH	BOOTCFG (Pulldown)	GPI (Pulldown)	102	126	E14
PD3	51	PD3 CNTX_B eMIOS11	GPIO CAN_B Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	101	125	E15
PD4	52	PD4 CNTX_C eMIOS12	GPIO CAN_C Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	100	124	E16
PD5	53	PD5 CNRX_C eMIOS13	GPIO CAN_C Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	99	123	F13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V_{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V_{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V_{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6[8]	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V_{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7[8]	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V_{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 $\overline{TS}$ TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V_{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V_{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V_{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V_{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V_{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V_{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V_{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Clock	I/O I O I/O	V_{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input[7] eMIOS Channel I^2C_A Serial Data	I/O I O I/O	V_{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 $\overline{CS3}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 $\overline{CS2}$	GPIO eQADC Analog Input[7] eMIOS Channel EBI Chip Select	I/O I O O	V_{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input[7] SCI_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input[7] SCI_E Receive eQADC External Mux Address	I/O I I O	V_{DDE2}	A + SH	—	—	19	24	J3

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PH6	118	PH6 AN21 TXD_F	GPIO eQADC Analog Input[7] SCI_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	18	23	J2
PH7	119	PH7 AN20 RXD_F	GPIO eQADC Analog Input[7] SCI_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	17	22	J1
PH8	120	PH8 AN19 CNTX_E MA0	GPIO eQADC Analog Input[7] CAN_E Transmit eQADC External Mux Address	I/O I O O	V_{DDE2}	A + SH	—	—	14	17	H1
PH9	121	PH9 AN18/ANT CNRX_E	GPIO eQADC Analog Input[7] CAN_E Receive	I/O I I	V_{DDE2}	A + SH	—	—	13	14	G2
PH10	122	PH10 AN17/ANS CNRX_F	GPIO eQADC Analog Input[7] CAN_F Receive	I/O I I	V_{DDE2}	A + SH	—	—	12	12	F4
PH11	123	PH11 AN16/ANR CNTX_F	GPIO eQADC Analog Input[7] CAN_F Transmit	I/O I O	V_{DDE2}	A + SH	—	—	11	11	F3
PH12	124	PH12 PCS_D5	GPIO DSPI_D Peripheral Chip Select	I/O O	V_{DDE2}	SH	—	—	—	—	F2
PH13	125	PH13	GPIO	I/O	V_{DDE2}	SH	—	—	—	—	F1
PH14	126	PH14 $\overline{WE2}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	53	T5
PH15	127	PH15 $\overline{WE3}$	GPIO EBI Write Enable	I/O O	V_{DDE2}	MH	—	—	—	52	R5
Port J (16)											
PJ0	128	PJ0 AD0	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N11
PJ1	129	PJ1 AD1	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	P11
PJ2	130	PJ2 AD2	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	N10
PJ3	131	PJ3 AD3	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	—	R10
PJ4	132	PJ4 AD4	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	75	P10
PJ5	133	PJ5 AD5	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	73	T9
PJ6	134	PJ6 AD6	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	69	P9
PJ7	135	PJ7 AD7	GPIO EBI Muxed Address/Data	I/O I/O	V_{DDE3}	MH	—	—	—	67	R8

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 5}$$

where:

T_J = junction temperature (^oC) *Eqn. 6*

T_B = board temperature at the package perimeter ($^oC/W$) *Eqn. 7*

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8 *Eqn. 8*

P_D = power dissipation in the package (W) *Eqn. 9*

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 10}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$) *Eqn. 11*

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$) *Eqn. 12*

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$) *Eqn. 13*

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 14}$$

where:

T_T = thermocouple temperature on top of the package (^oC) *Eqn. 15*

Ψ_{JT} = thermal characterization parameter ($^oC/W$) *Eqn. 16*

P_D = power dissipation in the package (W) *Eqn. 17*

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
805 East Middlefield Rd
Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

Table 6. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
21	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 100	100	mV
22	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} - V_{SSA}$	– 100	100	mV
23	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
24	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	– 100	100	mV
25	Slew rate on VDDA, VDDR, and VDDE power supply pins[9]	Vramp	1	100	V/ms
26	Capactive Supply Load VDD VDD33 VDDSYN	Vload	 800 200 200	 — —	nF

1 Please refer to Section 2.2.1, “General Notes for Specifications at Maximum Junction Temperature” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

2 M parts can’t go above 66 MHz.

3 V_{PP} can drop to 0 volts during read-only operations and before entry to Sleep mode, to reduce power consumption.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 If V_{DDE1} is below V_{DDA} than the analog input limits (spec #9 (Analog (AE/A) Input Voltage) in Table 6) will be based on the V_{DDE1} voltage level.

6 Absolute value of current, measured at V_{IL} and V_{IH}.

7 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH.

8 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: A and AE.

9 This applies to the ramp up rate from 0.3 volts to 3.0 volts.

2.5 Operating Current Specifications

Table 7. Operating Currents

Num	Characteristic	Symbol	Typ[1] 25C Ambient	Typ[1] 70C Ambient	Max[1] -40–145C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{PP} + I_{DDA} + I_{DDR}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3}$					
1	$V_{DDE(1,2,3)}$ Current $V_{DDE(1,2,3)}$ @ 3.0V - 5.5V Static[2], or when in SLEEP or STOP Dynamic[3]	I_{DDE}	 1 Note [3]	 3 Note [3]	 30 Note [3]	 µA mA
2	V_{PP} Current V_{PP} @ 0V (All modes) V_{PP} @ 5.25V SLEEP mode STOP mode RUN mode	I_{PP}	 1 15 15 1	 1 20 20 1	 1 30 30 25	 µA µA µA mA
3	V_{DDA} Current V_{DDA} @ 4.5V - 5.25V RUN mode[4] SLEEP/STOP[5] mode with 32KIRC SLEEP/STOP[5] mode with 32KOSC SLEEP/STOP[5] mode with 16MIRC	I_{DDA}	 5 12 12 111	 5 16 16 165	 10 26 28 225	 mA µA µA µA
4	V_{DDR} Current V_{DDR} @ 4.5V - 5.25V SLEEP mode with XOSC[6] (additonal) with RTC/API (additonal) each 8K RAM block (additional) STOP mode with XOSC[6] (additonal) RUN mode (Using 16 MHz IRC) RUN mode (Maximum @ 48 MHz)[7] RUN mode (Maximum @ 66 MHz)[8] RUN mode (Maximum @ 80MHz)[9]	I_{DDR}	 20 500 1 0.8 170 500 30 50 105 120	 25 600 1 7 600 600 35 75 110 130	 360 900 3 45 1500 900 40 90 120 135	 µA µA µA µA µA µA mA mA mA mA

1 Typ - Nominal voltage levels and functional activity. Max - Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 8 for more information.

4 RUN mode is a typical application with the ADC, 16MIRC, 32KIRC running.

5 SLEEP/STOP mode means that only the listed peripherals are on. All others are diabled.

6 XOSC: optionally enabled in SLEEP and STOP modes (oscillator remains running from crystal but XOSC clock output disabled).

7 RUN mode condition includes PLL selected as source of system clock, XOSC enabled with 40MHz crystal, all peripherals enabled, both cores running, and running a typical application using both SRAM and flash.

2.7 Low Voltage Characteristics

Table 9. Low Voltage Monitors

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level [1]	V_{POR}	—	0.70	—	V
2	Low Voltage Monitor 1.5V [1] Assert Level De-assert Level	 V_{LV15A} V_{LV15D}	 — —	 1.40 1.45	 — —	V
3	Low Voltage Monitor 3.3V [2] Assert Level De-assert Level	 V_{LV33A} V_{LV33D}	 — —	 3.05 3.10	 — —	V
4	Low Voltage Monitor Synthesizer [3] Assert Level De-assert Level	 V_{LVSYNA} V_{LVSYND}	 — —	 3.05 3.10	 — —	V
5	Low Voltage Monitor 5.0V Low Threshold [4] Assert Level De-assert Level	 V_{LV5LA} V_{LV5LD}	 3.30 3.35	 3.35 3.40	 3.40 3.45	V
6	Low Voltage Monitor 5.0V [4] Assert Level De-assert Level	 V_{LV5A} V_{LV5D}	 4.50 4.55	 4.55 4.60	 4.70 4.75	V
7	Low Voltage Monitor 5.0V High Threshold [4] Assert Level De-assert Level	 V_{LV5HA} V_{LV5HD}	 4.70 4.75	 4.75 4.80	 4.80 4.85	V

1 Monitors V_{DD}
2 Monitors V_{DD33}
3 Monitors V_{DDSYN}
4 Monitors V_{DDA}

Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut}	12.8	16	22.3	MHz
2	Frequency after loading factory trim[2]	F_t	15.1	16	16.9	MHz
3	Application trim resolution[3]	T_s	—	—	± 0.5	%
4	Application frequency trim step[3]	F_s	—	300	—	kHz
5	Start up time	S_t	—	—	500	ns

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut32}	20.8	32.0	43.2	kHz
2	Frequency after loading factory trim[2]	F_{t32}	26	32.0	38	kHz
3	Application trim resolution[3]	T_{s32}	—	—	± 2	%
4	Application frequency trim step[3]	F_{s32}	—	1	—	kHz
5	Start up time	S_{t32}	—	—	100	µs

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

2.9 FMPLL Electrical Characteristics

Table 14. FMPLL Electrical Specifications [1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	System frequency[2] -40 °C ≤ T_J ≤ 120 °C -40 °C ≤ T_J ≤ 145 °C	f_{sys}	 375 375	 80000 [3] 66000	kHz
2	PLL Reference Frequency (output of predivider)	f_{pllref}	4	10	MHz
3	VCO Frequency[4]	f_{vco}	250	500	MHz
4	PLL Frequency [5] -40 °C ≤ T_J ≤ 120 °C -40 °C ≤ T_J ≤ 145 °C	f_{pll}	 3 3	 80 [3] 66	MHz
5	Loss of Reference Frequency [6]	f_{LOR}	100	1000	kHz
6	Self Clocked Mode Frequency [7]	f_{SCM}	13	35	MHz
7	PLL Lock Time [8]	t_{lpll}	—	750	µs
8	Frequency un-LOCK Range	f_{UL}	– 4.0	4.0	% f_{sys}
9	Frequency LOCK Range	f_{LCK}	– 2.0	2.0	% f_{sys}
10	CLKOUT Cycle-to-cycle Jitter,[9, 10]	C_{jitter}	– 5	5	% f_{clkout}
10a	CLKOUT Jitter at 10 µs period [9,10, 11]	C_{jitter}	– 0.05	0.05	% f_{clkout}
11	Frequency Modulation Depth 1% Setting [12,13] (f_{sys}Max must not be exceeded)	C_{mod}	0.5	2	%f_{sys}
12	Frequency Modulation Depth 2% Setting [12,13] (f_{sys}Max must not be exceeded)	C_{mod}	1	3	%f_{sys}

1 V_{DDSYN} = 3.0V to 3.6 V, V_{SSSYN} = 0 V, TA = TL to TH

2 The maximum value is without frequency modulation turned on. If frequency modulation is turned on, the maximum value (average frequency) must be de-rated by the percentage of modulation enabled.

3 80 MHz is only available in the 208 pin package.

4 Optimum performance is achieved with the highest VCO frequency feasible based on the highest ERFD that results in the desired PLL frequency.

5 The VCO frequency range is higher than the maximum allowable PLL frequency. The synthesizer control register 2's enchanced reduced frequency divider (FMPLL_SYNCR2[ERFD]) in enhanced operation mode must be programmed to divide the VCO frequency within the PLL frequency range.

6 Loss of reference frequency is the reference frequency detected by the PLL which then transitions into self clocked mode.

7 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}.

8 This specification applies to the period required for the PLL to relock after changing the enhanced multiplication factor divider (EMFD) bits in the synthesizer control register 1 (SYNCR1) in enhanced operation mode.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider set to divide-by-2.

10 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

11 The PLL % jitter reduces with more cycles. 10 µs was picked for a reference point for LIN (100 Kbits), slower speeds will have even less % jitter.

12 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

13 These depth ranges are obtained by filtering the raw cycle-to-cycle clock frequency data to eliminate the presence of the the normal clock jitter riding on top of the FM waveform. The allowable modulation rates are 400 kHz to 1 MHz.

2.11 Flash Memory Electrical Characteristics

Table 16. Flash Program and Erase Specifications[1]

Num	Characteristic	Symbol	Min	Typ	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time [4]	$T_{dwprogram}$	—	10	—	500	µs
2	Page (128 bits) Program Time [4]	$T_{pprogram}$	—	15	44	500	µs
3	16 Kbyte Block Pre-program and Erase Time	$T_{16kpperase}$	—	325	525	5000	ms
4	64 Kbyte Block Pre-program and Erase Time	$T_{64kpperase}$	—	525	675	5000	ms
5	128 Kbyte Block Pre-program and Erase Time	$T_{128kpperase}$	—	675	1800	7500	ms
6	Minimum operating frequency for program and erase operations	—	25	—	—	—	MHz
7	Wait States Relative to System Frequency PFCRPn[RWSC] = 0b000; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b001; PFCRPn[WWSC] = 0b01 PFCRPn[RWSC] = 0b010; PFCRPn[WWSC] = 0b01	T_{rwsc}	 — — —	 — — —	 — — —	 25 50 80	MHz
8	Recovery Time Stop mode exit or STOP bit negated Sleep mode exit (with CRP_RECPTR[FASTREC]=1) [5]	$T_{recover}$	 — —	 — —	 — —	 20 120	 µs µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, nomial supply values and operation at 25 °C.

3 The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 This does not include software overhead.

5 If CRP_RECPTR[FASTREC]=0, then hardware will wait 2340 system clocks before exiting from Sleep mode to account for the flash recovery time. The default system clock source after Sleep is the 16MIRC. A nominal frequency of 16MHz equates to a hardware wait of 146µs.

Table 17. Flash EEPROM Module Life (Full Temperature Range)

Num	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of Program/Erase cycles per block over the operating temperature range (T_J) 16 Kbyte and 64 Kbyte blocks 128 Kbyte blocks	P/E	 100,000 1000	 — 100,000	cycles
2	Data retention Blocks with 0 – 1,000 P/E cycles Blocks with 1,001 – 100,000 P/E cycles	Retention	 20 5	—	years

1 Typical endurance is evaluated at 25C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619 “Typical Endurance for Nonvolatile Memory.”

2.13 AC Timing

2.13.1 Reset and Boot Configuration Pins

Table 19. Reset and Boot Configuration Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

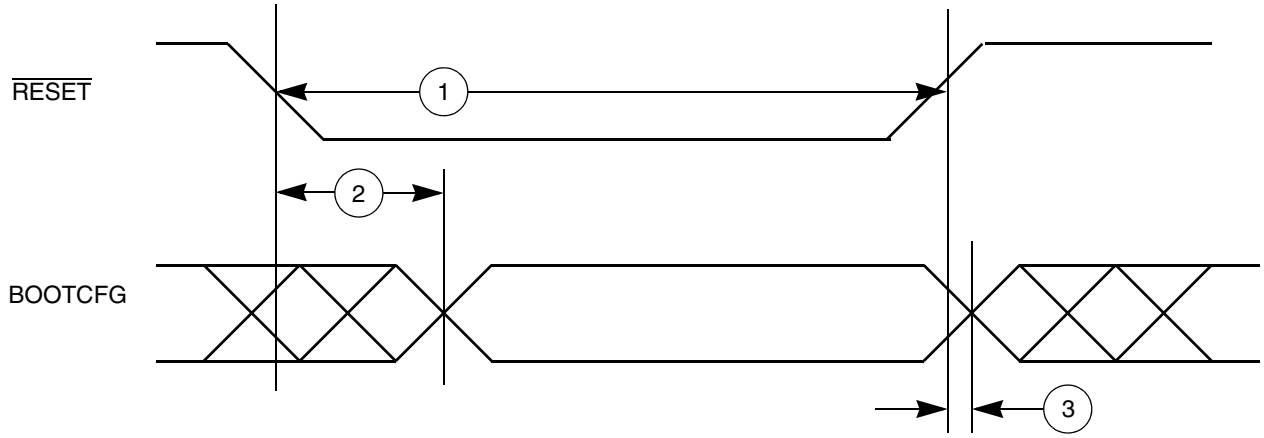

Figure 6. Reset and Boot Configuration Timing

2.13.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 20. IRQ/NMI Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

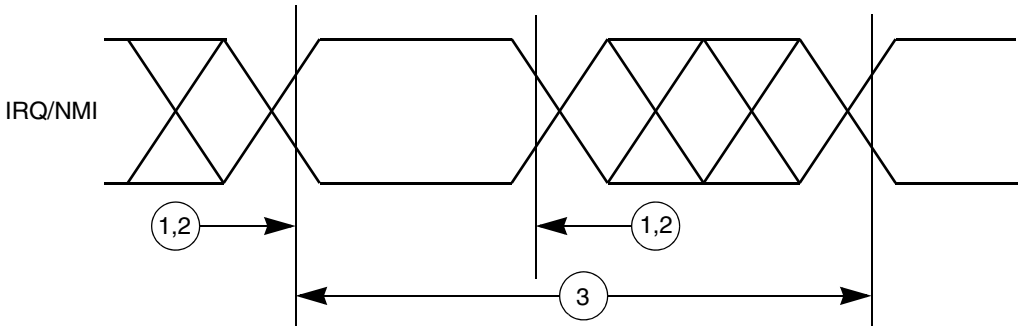

Figure 7. IRQ and NMI Timing

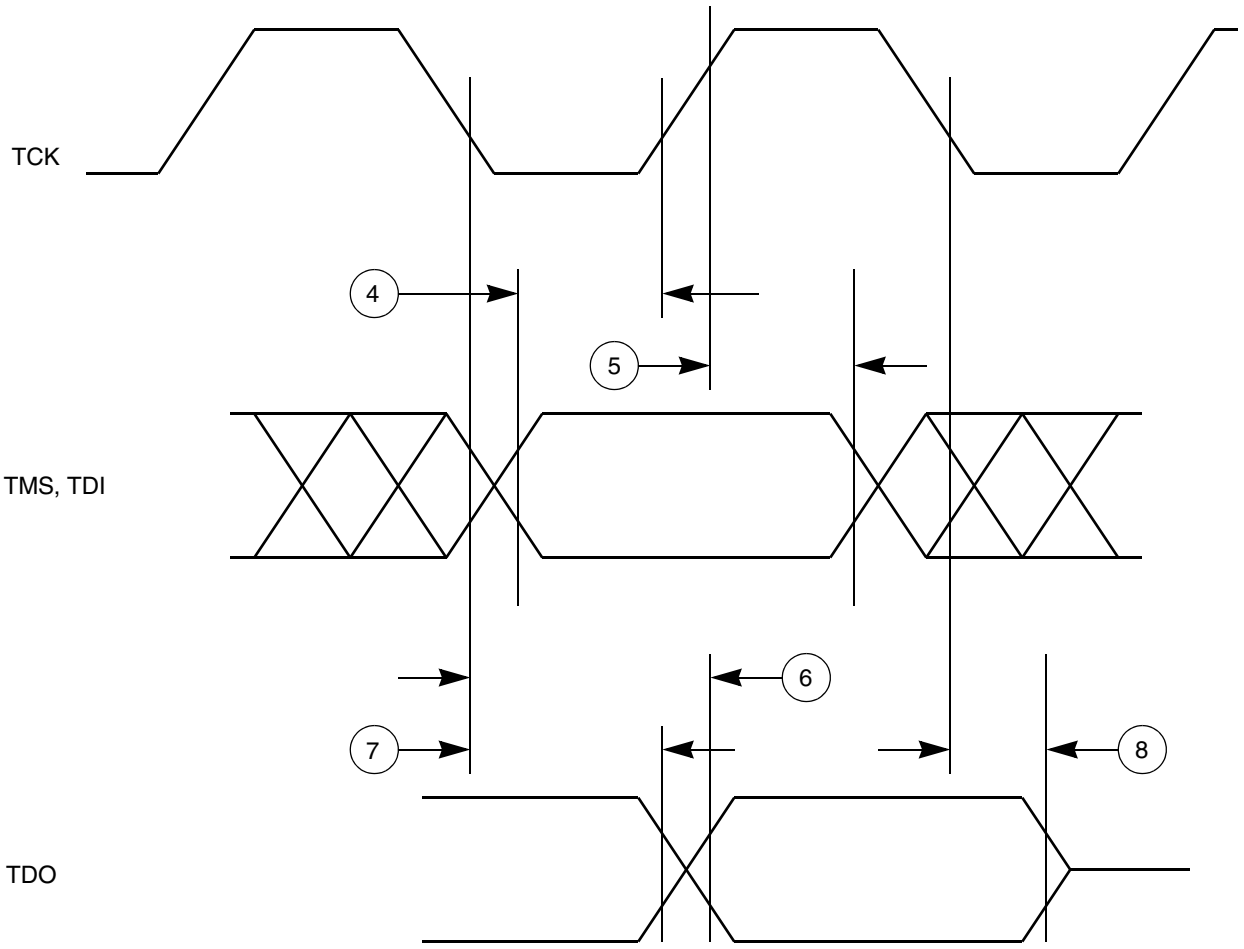

Figure 9. JTAG Test Access Port Timing

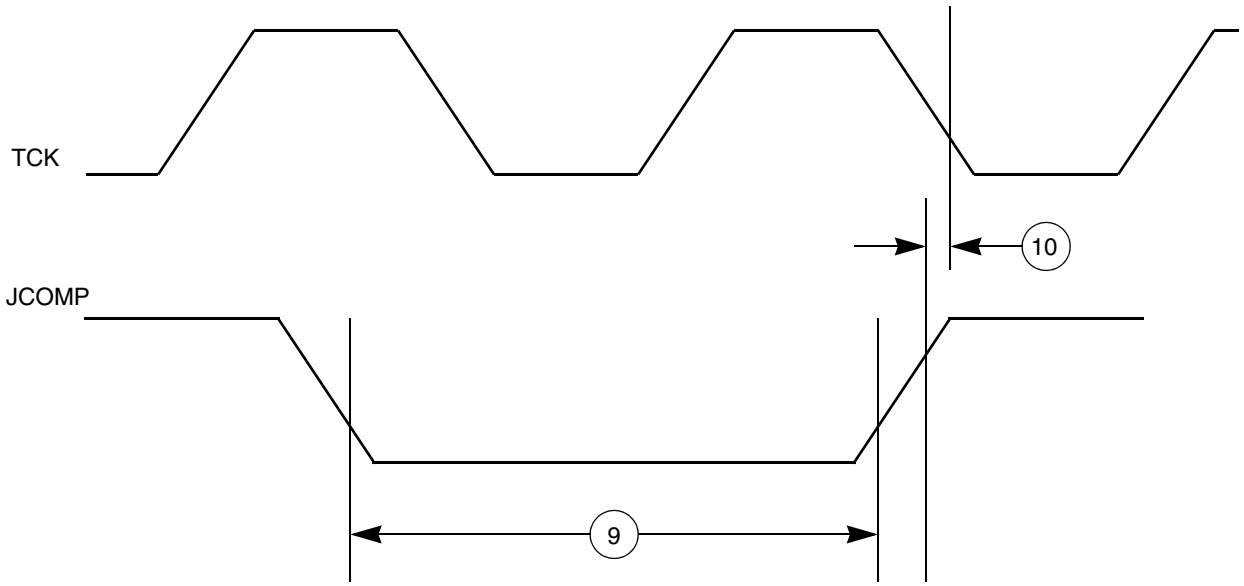

Figure 10. JTAG JCOMP Timing

2.13.4 Nexus Debug Interface

Table 22. Nexus Debug Port Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	40	—	ns
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–2	4.0	ns
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–2	4.0	ns
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–2	4.0	ns
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1		t_{MCYC}
8	TCK Cycle Time[3]	t_{TCYC}	40	—	ns
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	t_{NTDIH}, t_{NTMSH}	4	—	ns
12	TCK Low to TDO Data Valid	t_{JOV}	0	8	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 30pF with SRC = 0b11.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

3 The system clock frequency needs to be three times faster that the TCK frequency.

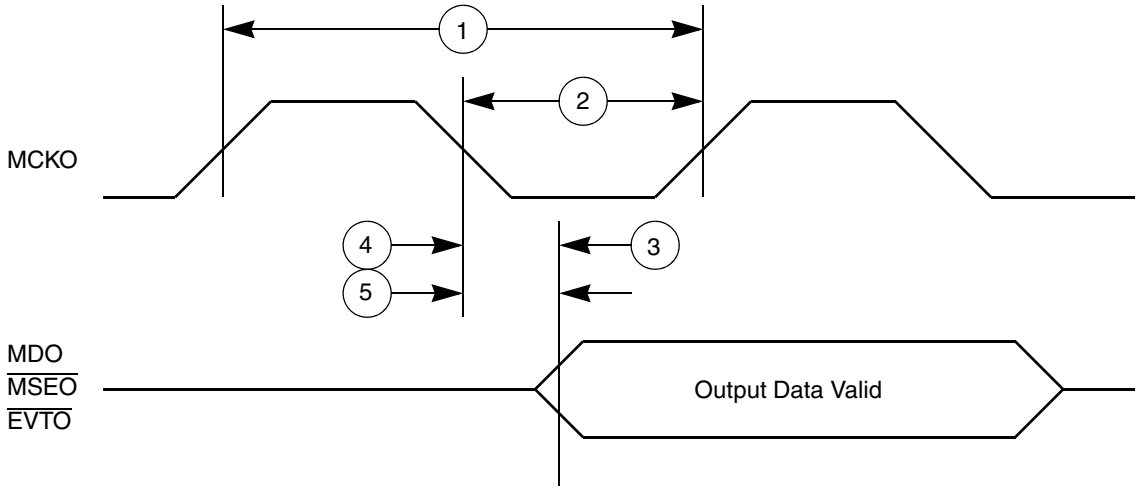

Figure 12. Nexus Output Timing

2.13.5 External Bus Interface (EBI)

Table 23. External Bus Operation Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
1	CLKOUT Period[2]	T_C	40.0	—	ns
2	CLKOUT duty cycle	t_{CDC}	45%	55%	T_C
3	CLKOUT rise time	t_{CRT}	—	—[3]	ns
4	CLKOUT fall time	t_{CFT}	—	—[3]	ns
5	CLKOUT Positive Edge to Output Signal Invalid or High Z (Hold Time)	t_{COH}	2.0	—	ns
6	CLKOUT Positive Edge to Output Signal Valid (Output Delay)	t_{COV}	—	10.0	ns
7	Input Signal Valid to CLKOUT Posedge (Setup Time)	t_{CIS}	20.0	—	ns
8	CLKOUT Posedge to Input Signal Invalid (Hold Time)	t_{CIH}	0	—	ns
9	ALE Pulse Width High Time	t_{ALEPWH}	20	—	ns
10	ALE Fall to AD Invalid	t_{ALEAD}	2	—	ns

1 EBI timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 50pF with SIU_PCR*n*[SRC] = 0b11.

2 Initialize SIU_ECCR[EBDF] to meet maximum external bus frequency.

3 Refer to Medium High Voltage (MH) pad AC specification in Table 18.

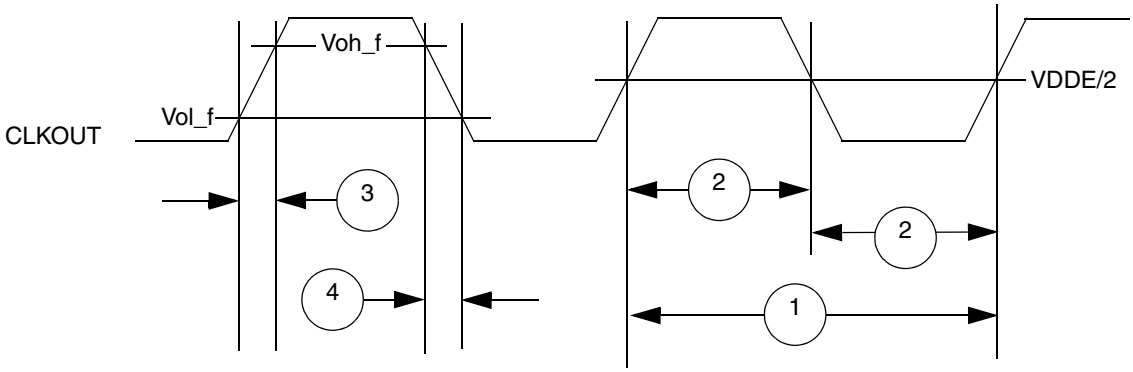

Figure 14. CLKOUT Timing

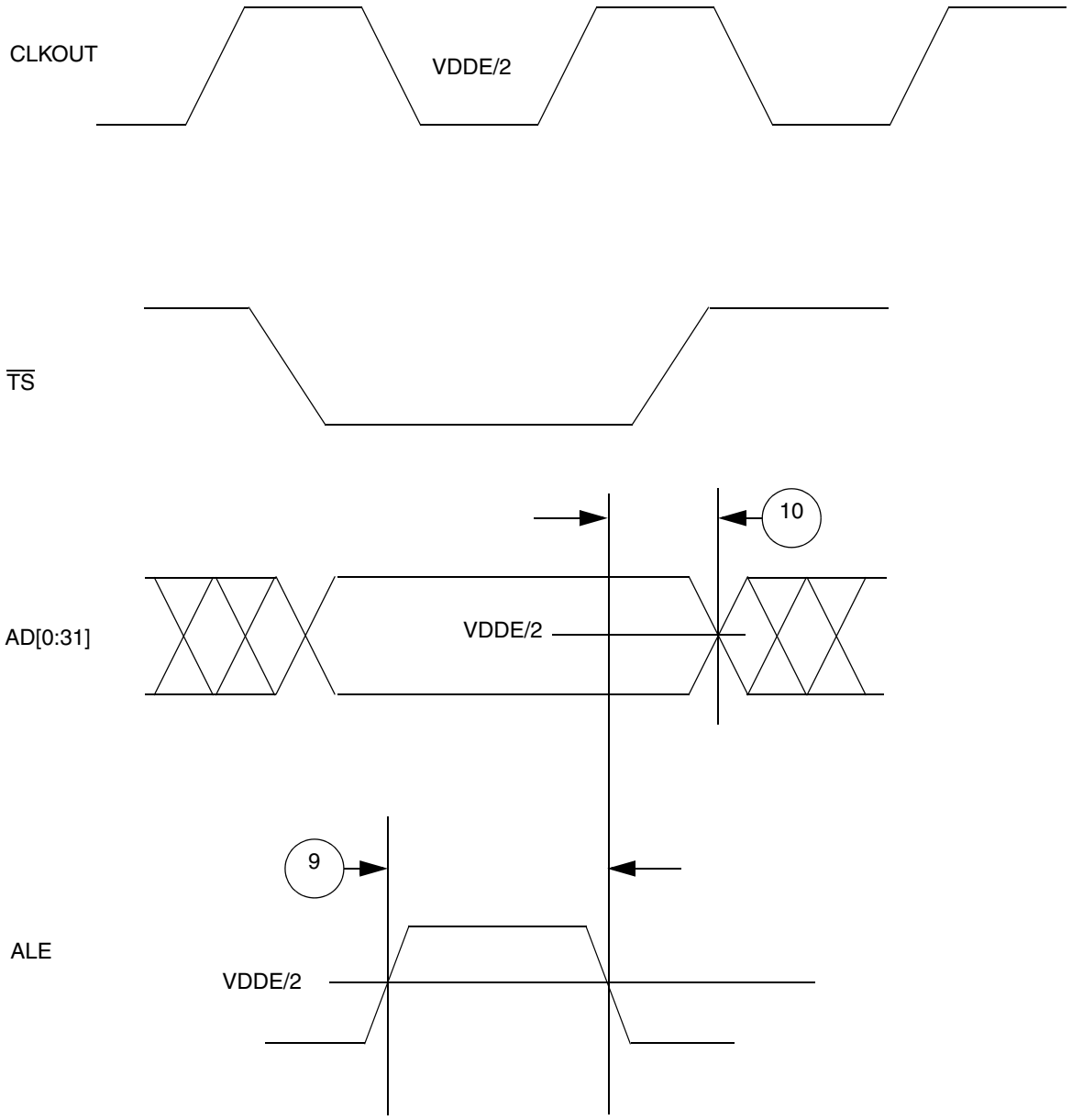

Figure 17. Address Latch Enable (ALE) Timing

2.13.6 Enhanced Modular I/O Subsystem (eMIOS)

Table 24. eMIOS Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1	—	t_{CYC}

2.13.7 Deserial Serial Peripheral Interface (DSPI)

Table 25. DSPI Timing[1]

Num	Characteristic	Symbol	66 MHz		Unit
			Min	Max	
1	SCK Cycle TIme[2,3]	t_{SCK}	60	—	ns
2	PCS to SCK Delay[4]	t_{CSC}	20	—	ns
3	After SCK Delay[5]	t_{ASC}	20	—	ns
4	SCK Duty Cycle	t_{SDC}	$t_{SCK}/2$ –2ns	$t_{SCK}/2$ + 2ns	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT driven)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	4	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	5	—	ns
9	Data Setup Time for Inputs	t_{SUI}			
	Master (MTFE = 0)		35	—	ns
	Slave		5	—	ns
	Master (MTFE = 1, CPHA = 0)[6]		5	—	ns
	Master (MTFE = 1, CPHA = 1)		35	—	ns
10	Data Hold Time for Inputs	t_{HI}			
	Master (MTFE = 0)		–4	—	ns
	Slave		10	—	ns
	Master (MTFE = 1, CPHA = 0)[6]		26	—	ns
	Master (MTFE = 1, CPHA = 1)		–4	—	ns
11	Data Valid (after SCK edge)	t_{SUO}			
	Master (MTFE = 0)		—	15	ns
	Slave		—	35	ns
	Master (MTFE = 1, CPHA=0)		—	30	ns
	Master (MTFE = 1, CPHA=1)		—	15	ns
12	Data Hold Time for Outputs	t_{HO}			
	Master (MTFE = 0)		–15	—	ns
	Slave		5.5	—	ns
	Master (MTFE = 1, CPHA = 0)		0	—	ns
	Master (MTFE = 1, CPHA = 1)		–15	—	ns

1 DSPI timing specified at VDDE = 3.0V to 5.5V, T_A = TL to TH, and CL = 50pF with SRC = 0b11.

2 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

3 The actual minimum SCK Cycle Time is limited by pad performance.

4 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]

5 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]

6 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

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