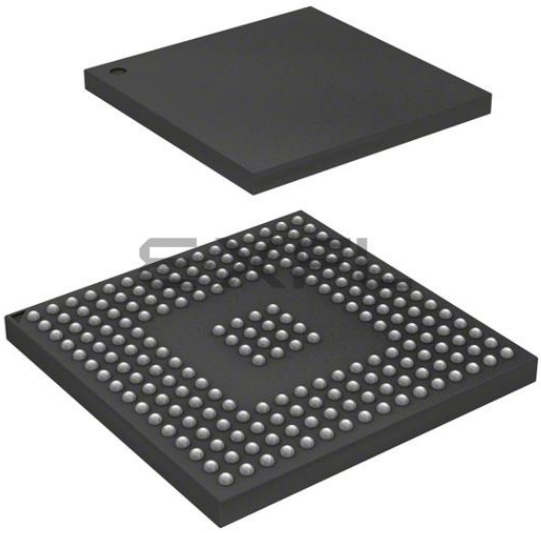

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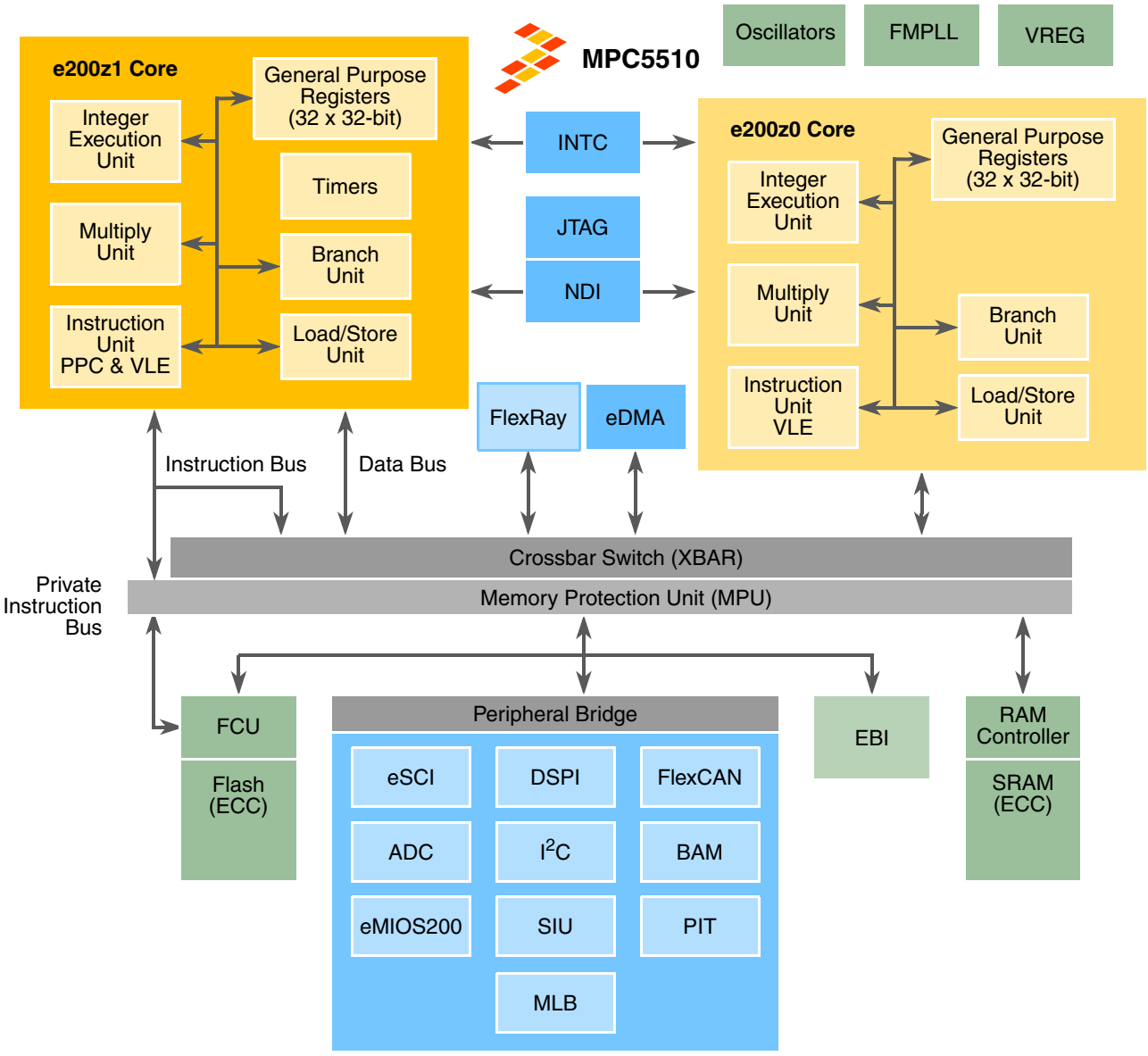
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0, e200z1
Core Size	32-Bit Dual-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	144
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5517gavmg80



LEGEND

ADC	– Analog to Digital Converter modules	**FlexRay**	– Dual Channel FlexRay controller
BAM	– Boot Assist Module	**FMPLL**	– Frequency Modulated Phase Locked Loop module
EBI	– External Bus Interface module	**I^2C**	– Inter IC Controller modules
ECC	– Error Correction Code	**INTC**	– Interrupt Controller module
DSPI	– Serial Peripherals Interface controller module	**JTAG**	– Joint Test Action Group interface
eDMA	– enhanced Direct Memory Controller module	**MLB**	– Media Local Bus emulation logic
eMIOS200	– Timed Input Output module	**NDI**	– Nexus Debug Interface module
eSCI	– Serial Communications Interface modules	**PIT**	– Periodic Interrupt Timer module
FCU	– Flash Controller Unit	**SIU**	– System Integration module
FlexCAN	– Controller Area Network controller modules	**VREG**	– Voltage Regulator

Figure 1. MPC5510 Family Block Diagram

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V_{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V_{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX $\overline{TS}$	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V_{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V_{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V_{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V_{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PC10	42	PC10 eMIOS10 PCS_C5 SCK_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Clock	I/O I/O O I/O	V_{DDE1}	SH	—	—	110	134	A14
PC11	43	PC11 eMIOS11 PCS_C4 SOUT_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial Out	I/O I/O O O	V_{DDE1}	SH	—	—	109	133	B14
PC12	44	PC12 eMIOS12 PSC_C3 SIN_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial In	I/O I/O O I	V_{DDE1}	SH	—	—	108	132	B16
PC13	45	PC13 eMIOS13 PCS_A5 PCS_D0	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	107	131	C15
PC14	46	PC14 eMIOS14 PCS_A4 PCS_D1	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	106	130	C16
PC15	47	PC15 eMIOS15 PCS_A3 PCS_D2	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE1}	SH	—	—	105	129	D14
Port D (16)											
PD0	48	PD0 CNTX_A PCS_D3	GPIO CAN_A Transmit DSPI_D Peripheral Chip Select	I/O O O	V_{DDE1}	SH	—	—	104	128	D15
PD1	49	PD1 CNRX_A PCS_D4	GPIO CAN_A Receive DSPI_D Peripheral Chip Select	I/O I O	V_{DDE1}	SH	—	—	103	127	D16
PD2	50	PD2 CNRX_B eMIOS10 BOOTCFG PCS_D5	GPIO CAN_B Receive eMIOS Channel Boot Configuration DSPI_D Peripheral Chip Select	I/O I O I O	V_{DDE1}	SH	BOOTCFG (Pulldown)	GPI (Pulldown)	102	126	E14
PD3	51	PD3 CNTX_B eMIOS11	GPIO CAN_B Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	101	125	E15
PD4	52	PD4 CNTX_C eMIOS12	GPIO CAN_C Transmit eMIOS Channel	I/O O O	V_{DDE1}	SH	—	—	100	124	E16
PD5	53	PD5 CNRX_C eMIOS13	GPIO CAN_C Receive eMIOS Channel	I/O I O	V_{DDE1}	SH	—	—	99	123	F13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PE3	67	PE3 SCK_A eMIOS2 MLBSO / MLBSIG_BUFEN	GPIO DSPI_A Clock eMIOS Channel MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin)	I/O I/O O O O	V_{DDE1}	MH	—	—	83	100	M13
PE4	68	PE4 SOUT_A eMIOS1 MLBDO / MLBDAT_BUFEN	GPIO DSPI_A Data Out eMIOS Channel MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin)	I/O O O O O	V_{DDE1}	MH	—	—	82	98	N14
PE5	69	PE5 SIN_A eMIOS0 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS	GPIO DSPI_A Data In eMIOS Channel MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data	I/O I O O O O	V_{DDE1}	MH	—	—	81	97	M15
PE6	70	PE6 CLKOUT	GPIO System Clock Output	I/O O	V_{DDE3}	MH	—	—	67	83	P13
PE7	71	PE7	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H13
PE8	72	PE8	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	H16
PE9	72	PE9	GPIO	I/O	V_{DDE1}	SH	—	—	—	—	J13
PE10	74	PE10	GPIO	I/O	V_{DDE1}	SH	—	—	—	112	J16
PE11	75	PE11	GPIO	I/O	V_{DDE1}	SH	—	—	—	111	J15
PE12	76	PE12	GPIO	I/O	V_{DDE1}	SH	—	—	—	109	K13
PE13	77	PE13	GPIO	I/O	V_{DDE1}	SH	—	—	—	108	L13
PE14	78	PE14	GPIO	I/O	V_{DDE1}	SH	—	—	—	102	L16
PE15	79	PE15	GPIO	I/O	V_{DDE1}	SH	—	—	—	99	M14
Port F (16)											
PF0	80	PF0 RD_$\overline{WR}$ EVTI[8]	GPIO EBI Read/Write Nexus Event In	I/O I/O I	V_{DDE3}	MH	—	—	66	82	N12
PF1	81	PF1 $\overline{TA}$ MLBCLK EVTO[8]	GPIO EBI Transfer Acknowledge MLB Clock Nexus Event Out	I/O I/O I O	V_{DDE3}	MH	—	—	65	81	P12
PF2	82	PF2 AD8 ADDR8 MLBSI / MLBSIG $\overline{MSEO}$[8]	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal In (5-pin) / MLB Bi-Directional Signal (3-pin) Nexus Message Start/End Out	I/O I/O O I I/O O	V_{DDE3}	MH	—	—	64	80	R12

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num[1]	Supported Functions[2]	Description	I/O Type	Voltage[3]	Pad[4] Type	Status During Reset[5]	Status After Reset[5]	Package Pin Locations		
									144	176	208
PJ8	136	PJ8 PCS_D4	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	27	K2
PJ9	137	PJ9 PCS_D3	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	26	K1
PJ10	138	PJ10 PCS_D2	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	25	J4
PJ11	139	PJ11 PCS_D1	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	19	H3
PJ12	140	PJ12 PCS_D0	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V_{DDE2}	SH	—	—	—	18	H2
PJ13	141	PJ13 SCK_D	GPIO DSPI_D Clock	I/O I/O	V_{DDE2}	SH	—	—	—	16	G4
PJ14	142	PJ14 SOUT_D	GPIO DSPI_D Serial Out	I/O O	V_{DDE2}	SH	—	—	—	15	G3
PJ15	143	PJ15 SIN_D	GPIO DSPI_D Serial In	I/O I	V_{DDE2}	SH	—	—	—	13	G1
Port K (2)											
PK0	144	PK0 EXTAL32	GPIO 32 kHz Crystal Oscillator Input	I I	V_{DDA}	AE + IH	—	—	—	168	B6
PK1	145	PK1 XTAL32	GPIO 32 kHz Crystal Oscillator Output	I O	V_{DDA}	AE + IH	—	—	—	166	A6
Miscellaneous Pins (9)											
EXTAL	—	EXTAL EXTCLK	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	AE	EXTAL		75	91	N16
XTAL	—	XTAL	Main Crystal Oscillator Output	O	V_{DDSYN}	AE	XTAL		74	90	P16
TMS	—	TMS	JTAG Test Mode Select Input	I	V_{DDE3}	SH	TMS (Pull Up)		72	88	T15
TCK	—	TCK	JTAG Test Clock Input	I	V_{DDE3}	IH	TCK (Pull Down)		71	87	R14
TDO	—	TDO	JTAG Test Data Output	O	V_{DDE3}	MH	TDO (Pull Up[9])		70	86	T14
TDI	—	TDI	JTAG Test Data Input	I	V_{DDE3}	IH	TDI (Pull Up)		69	85	R13
JCOMP	—	JCOMP	JTAG Compliancy	I	V_{DDE3}	IH	JCOMP (Pull Down)		68	84	T13
TEST[10]	—	TEST	Test Mode Select	I	V_{DDE3}	IH	TEST		62	78	R11
$\overline{\text{RESET}}$	—	$\overline{\text{RESET}}$	External Reset	I/O	V_{DDE2}	SH	$\overline{\text{RESET}}$ (Pull Up)		10	10	E4

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

2 This column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, function 1, function 2, and function 3. The unused functions by a given pin begin with function 3, then function 2, then function 1.

3 These are nominal voltages. Each segment provides the power and ground for the given set of I/O pins.

4 Pad types: SH - Bi-directional slow speed pad with input hysteresis; MH - Bi-directional medium speed pad with input hysteresis; IH - Input only pad with input hysteresis; AE/A - Analog pad.

5 A dash for the function in this column denotes the input and output buffer are turned off.

3 V_{RL} is shorted to V_{SSA} in the 144LQFP and 176 LQFP packages.

4 V_{PP} requires 5V for program/erase operations, but may be 0-5V otherwise. V_{PP} should not go high or low when the device is in Sleep mode.

5 Voltage generated from internal voltage regulator and no external connection or load allowed except the required bypass capacitors.

6 V_{FLASH} is shorted to V_{DD33} in the package.

1.4 Pinout – 176 LQFP

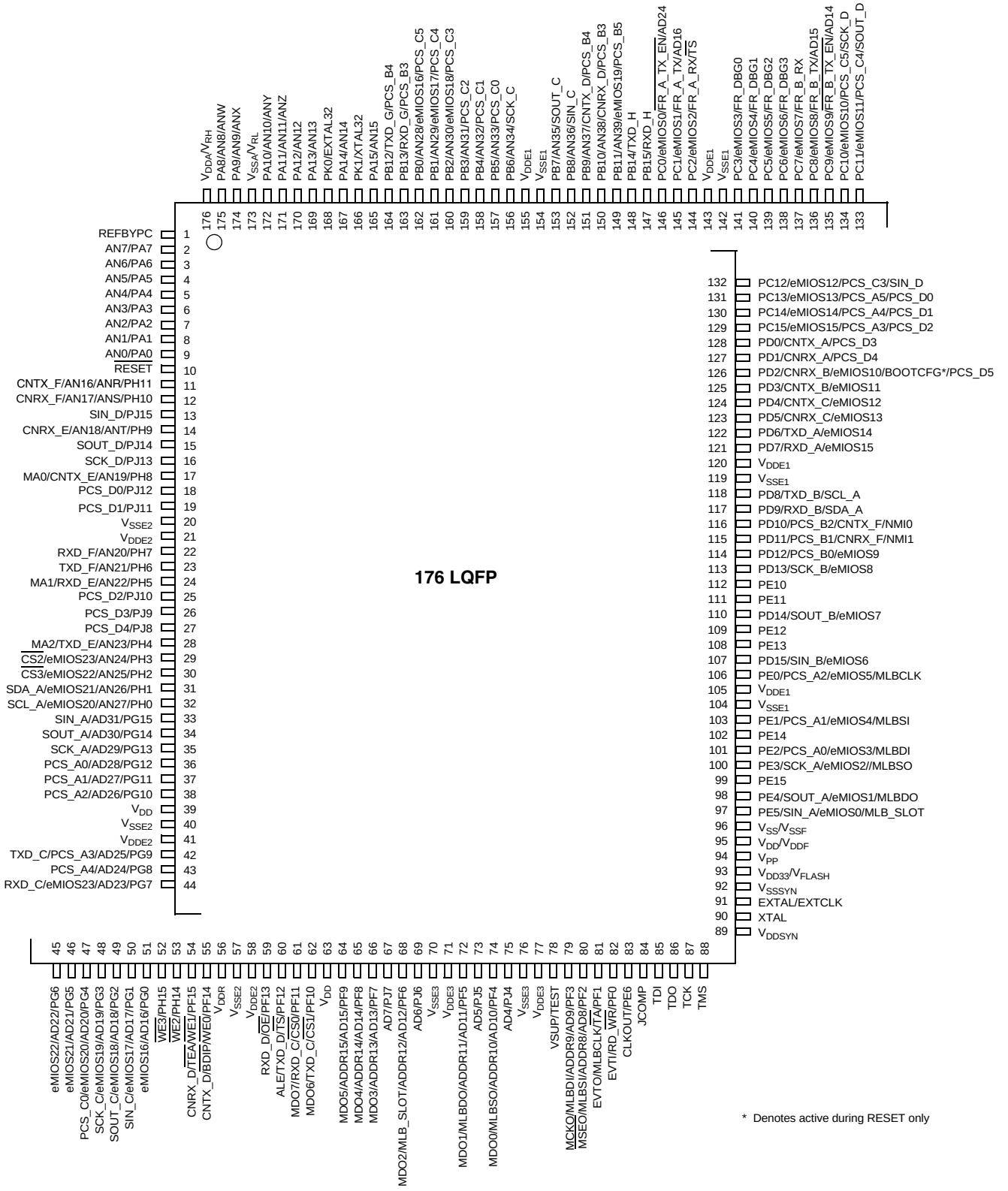


Figure 3. MPC5510 Pinout – 176 LQFP

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Num	Characteristic	Symbol	Min	Max[2]	Unit
1	5.0V Voltage Regulator Reference Voltage	V_{DDR}	– 0.3	6.5	V
2	5.0V Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	– 0.3	6.5	V
3	5.0V Flash Program/Erase Voltage	V_{PP}	– 0.3	6.5	V
4	3.3V – 5.0V External I/O Supply Voltage [3]	V_{DDE1}[4] V_{DDE2}[4] V_{DDE3}[4]	– 0.3 – 0.3 – 0.3	6.5 6.5 6.5	V
5	DC Input Voltage [5]	V_{IN}	–1.0[6]	6.5[7]	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 0.3	5.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 5.5	5.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 0.3	0.3	V
9	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	$- V_{DDA}$	0.3	V
10	Maximum DC Digital Input Current [8] (per pin, applies to all digital MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
11	Maximum DC Analog Input Current [9] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
12	Storage Temperature Range	T_{STG}	– 55.0	150.0	°C
13	Maximum Solder Temperature [10]	T_{SDR}	—	260.0	°C
14	Moisture Sensitivity Level [11]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn–in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 AC signal over and undershoot of the input voltages of up to +/– 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

6 Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

7 Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25mA.

9 Total injection current for all analog input pins must not exceed 15mA.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 4. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	176 LQFP	144 LQFP
1	Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	44	38	43
2	Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	27	31	34
3	Junction to Ambient [1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	35	30	34
4	Junction to Ambient [1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	24	25	28
5	Junction to Board [4]	$R_{\theta JB}$	°C/W	16	20	22
6	Junction to Case [5]	$R_{\theta JC}$	°C/W	8	6	7
7	Junction to Package Top [6] Natural Convection	Ψ_{JT}	°C/W	2	2	2

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package } (^oC) \quad \textit{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance } (^oC/W) \quad \textit{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \textit{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \textit{Eqn. 5}$$

where:

T_J = junction temperature (^oC) *Eqn. 6*

T_B = board temperature at the package perimeter ($^oC/W$) *Eqn. 7*

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8 *Eqn. 8*

P_D = power dissipation in the package (W) *Eqn. 9*

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 10}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$) *Eqn. 11*

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$) *Eqn. 12*

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$) *Eqn. 13*

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

2.4 DC Electrical Specifications

Table 6. DC Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1a	**C parts** Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 105 85	 °C °C
1b	**V parts** Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 120 105	 °C °C
1c	**M parts**[2] Operating junction temperature range Operating ambient temperature range[1]	 T_J T_A	 – 40 – 40	 145 125	 °C °C
2	5.0V Voltage Regulator Reference Voltage	V_{DDR}	4.5	5.25	V
3	5.0V Analog Supply Voltage	V_{DDA}	4.5	5.25	V
4	5.0V Flash Program/Erase Voltage [3]	V_{PP}	4.5	5.25	V
5	3.3V – 5.0V External I/O Supply Voltage	V_{DDE1}[4,5] V_{DDE2}[4] V_{DDE3}[4]	3.0 3.0 3.0	5.5 5.5 5.5	V
6	Pad (SH/MH/IH) Input High Voltage	V_{IH}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
7	Pad (SH/MH/IH) Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
8	Pad (SH/MH/IH) Input Hysteresis	V_{HYS}	$0.1 \times V_{DDE}$	$0.2 \times V_{DDE}$	V
9	Analog (AE/A) Input Voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$ see note[5]	V
10	Slow/Medium I/O Output High Voltage I_{OH} = –1.0 mA I_{OH} = –0.2 mA	V_{OH}	 $0.80 \times V_{DDE}$ $0.95 \times V_{DDE}$	—	V
11	Slow/Medium I/O Output Low Voltage I_{OL} = 1.0 mA I_{OH} = 0.2 mA	V_{OL}	—	 $0.20 \times V_{DDE}$ $0.05 \times V_{DDE}$	V
12	Input Capacitance (Digital Pins: Pad type MH,SH, IH with no A or AE)	C_{IN}	—	7	pF
13	Input Capacitance (Analog Pins: Pad type A, AE, and AE+IH)	C_{IN_A}	—	10	pF
14	Input Capacitance (Shared digital and analog pins: A with SH or MH)	C_{IN_M}	—	12	pF
15	Slow/Medium I/O Weak Pull Up/Down Absolute Current [6]	I_{ACT}	10	170	µA
16	I/O Input Leakage Current [7]	I_{INACT_D}	– 1.5	1.5	µA
17	DC Injection Current (per pin)	I_{IC}	– 2.0	2.0	mA
18	Analog Input Current, Channel Off [8] (Analog pins AE and AE+IH)	I_{INACT_A}	– 200	200	nA
19	Analog Input Current (Shared digital and analog pins: A with SH or MH)	I_{INACT_AD}	–1.5	1.5	µA
20	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 100	100	mV

Table 6. DC Electrical Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
21	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	– 100	100	mV
22	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} - V_{SSA}$	– 100	100	mV
23	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
24	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	– 100	100	mV
25	Slew rate on VDDA, VDDR, and VDDE power supply pins[9]	Vramp	1	100	V/ms
26	Capactive Supply Load VDD VDD33 VDDSYN	Vload	 800 200 200	 — —	nF

1 Please refer to Section 2.2.1, “General Notes for Specifications at Maximum Junction Temperature” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

2 M parts can’t go above 66 MHz.

3 V_{PP} can drop to 0 volts during read-only operations and before entry to Sleep mode, to reduce power consumption.

4 V_{DDE1}, V_{DDE2}, and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

5 If V_{DDE1} is below V_{DDA} than the analog input limits (spec #9 (Analog (AE/A) Input Voltage) in Table 6) will be based on the V_{DDE1} voltage level.

6 Absolute value of current, measured at V_{IL} and V_{IH}.

7 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH.

8 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: A and AE.

9 This applies to the ramp up rate from 0.3 volts to 3.0 volts.

2.7 Low Voltage Characteristics

Table 9. Low Voltage Monitors

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level [1]	V_{POR}	—	0.70	—	V
2	Low Voltage Monitor 1.5V [1] Assert Level De-assert Level	 V_{LV15A} V_{LV15D}	 — —	 1.40 1.45	 — —	V
3	Low Voltage Monitor 3.3V [2] Assert Level De-assert Level	 V_{LV33A} V_{LV33D}	 — —	 3.05 3.10	 — —	V
4	Low Voltage Monitor Synthesizer [3] Assert Level De-assert Level	 V_{LVSYNA} V_{LVSYND}	 — —	 3.05 3.10	 — —	V
5	Low Voltage Monitor 5.0V Low Threshold [4] Assert Level De-assert Level	 V_{LV5LA} V_{LV5LD}	 3.30 3.35	 3.35 3.40	 3.40 3.45	V
6	Low Voltage Monitor 5.0V [4] Assert Level De-assert Level	 V_{LV5A} V_{LV5D}	 4.50 4.55	 4.55 4.60	 4.70 4.75	V
7	Low Voltage Monitor 5.0V High Threshold [4] Assert Level De-assert Level	 V_{LV5HA} V_{LV5HD}	 4.70 4.75	 4.75 4.80	 4.80 4.85	V

1 Monitors V_{DD}
2 Monitors V_{DD33}
3 Monitors V_{DDSYN}
4 Monitors V_{DDA}

Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut}	12.8	16	22.3	MHz
2	Frequency after loading factory trim[2]	F_t	15.1	16	16.9	MHz
3	Application trim resolution[3]	T_s	—	—	± 0.5	%
4	Application frequency trim step[3]	F_s	—	300	—	kHz
5	Start up time	S_t	—	—	500	ns

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut32}	20.8	32.0	43.2	kHz
2	Frequency after loading factory trim[2]	F_{t32}	26	32.0	38	kHz
3	Application trim resolution[3]	T_{s32}	—	—	± 2	%
4	Application frequency trim step[3]	F_{s32}	—	1	—	kHz
5	Start up time	S_{t32}	—	—	100	µs

1 Across process, voltage, and temperature
2 Across voltage and temperature
3 Fixed voltage and temperature

2.13 AC Timing

2.13.1 Reset and Boot Configuration Pins

Table 19. Reset and Boot Configuration Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

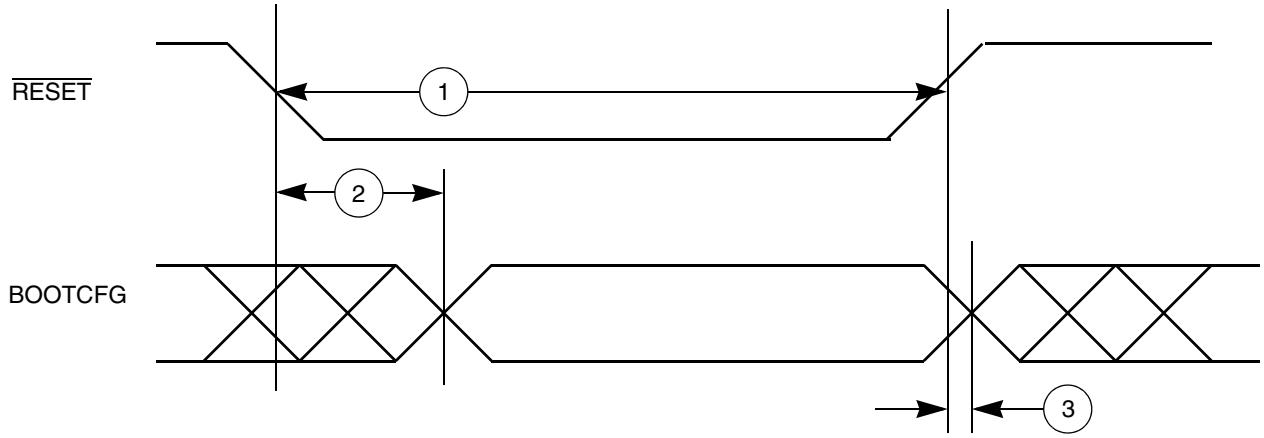


Figure 6. Reset and Boot Configuration Timing

2.13.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 20. IRQ/NMI Timing

Num	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

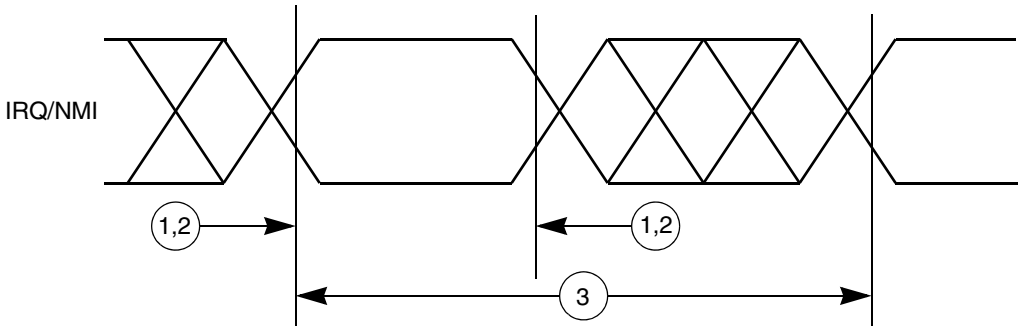


Figure 7. IRQ and NMI Timing

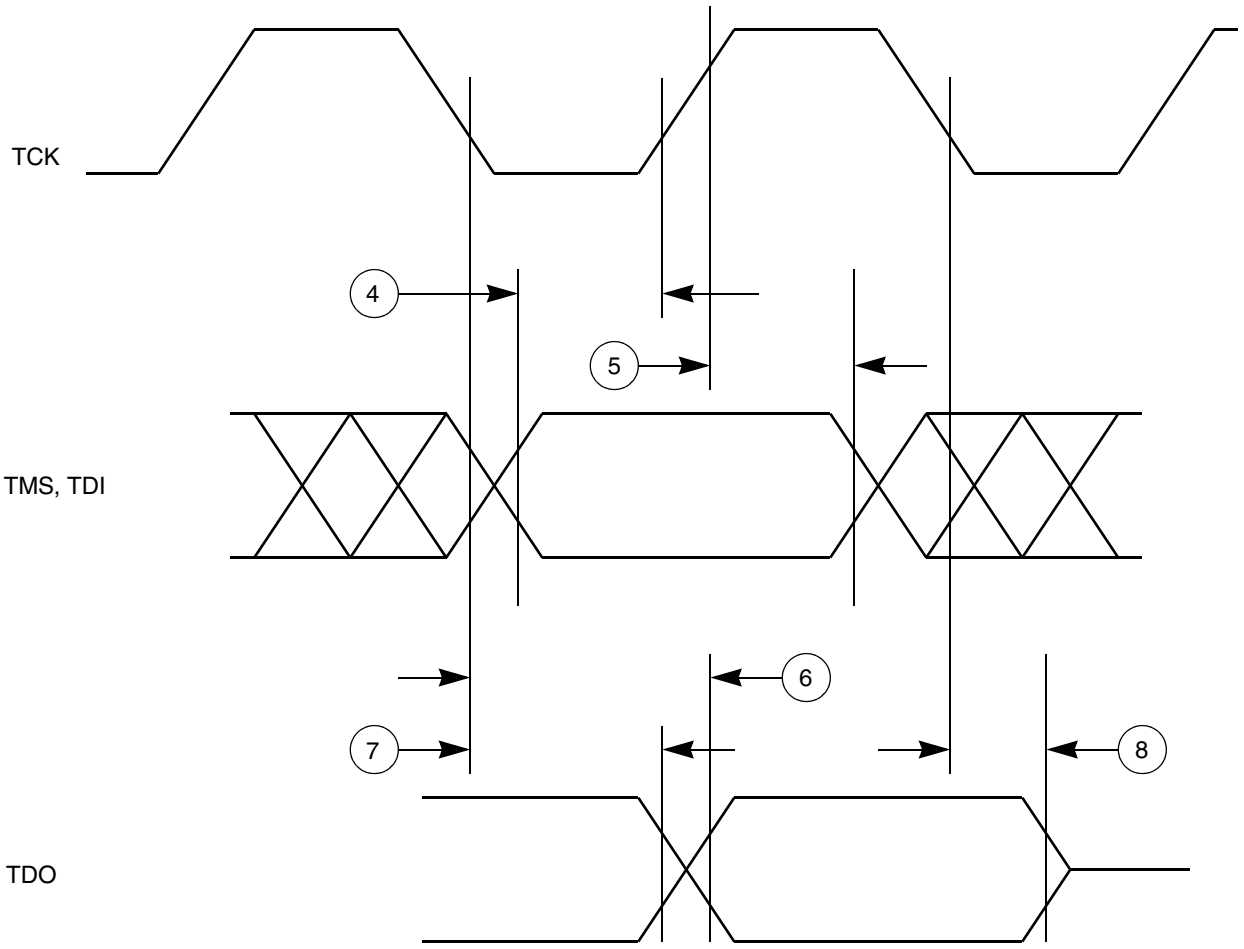


Figure 9. JTAG Test Access Port Timing

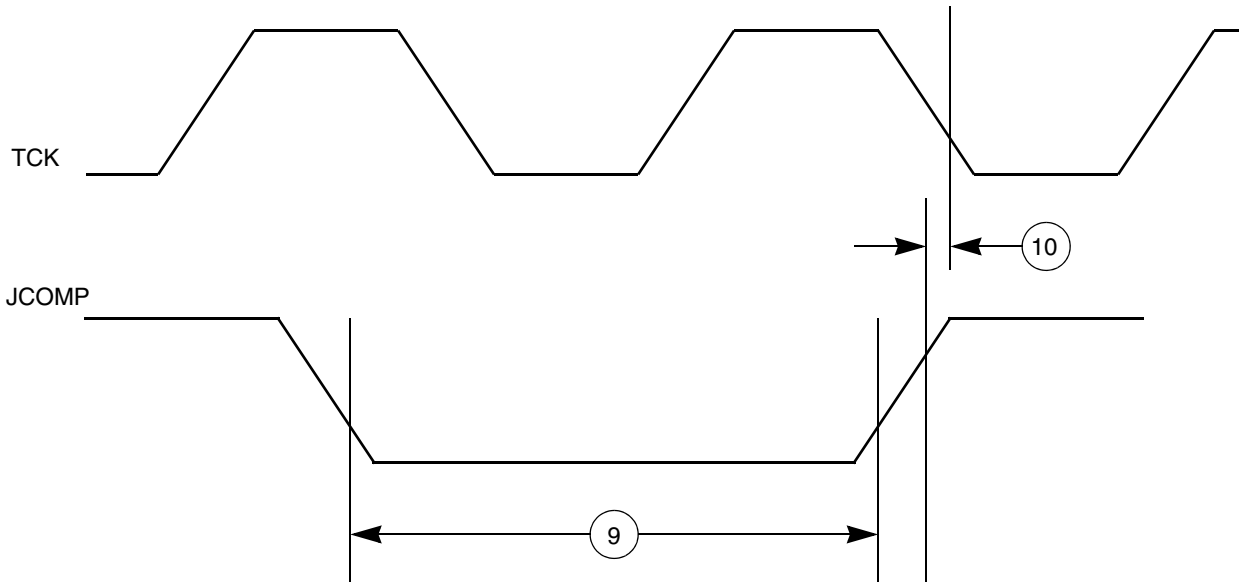


Figure 10. JTAG JCOMP Timing

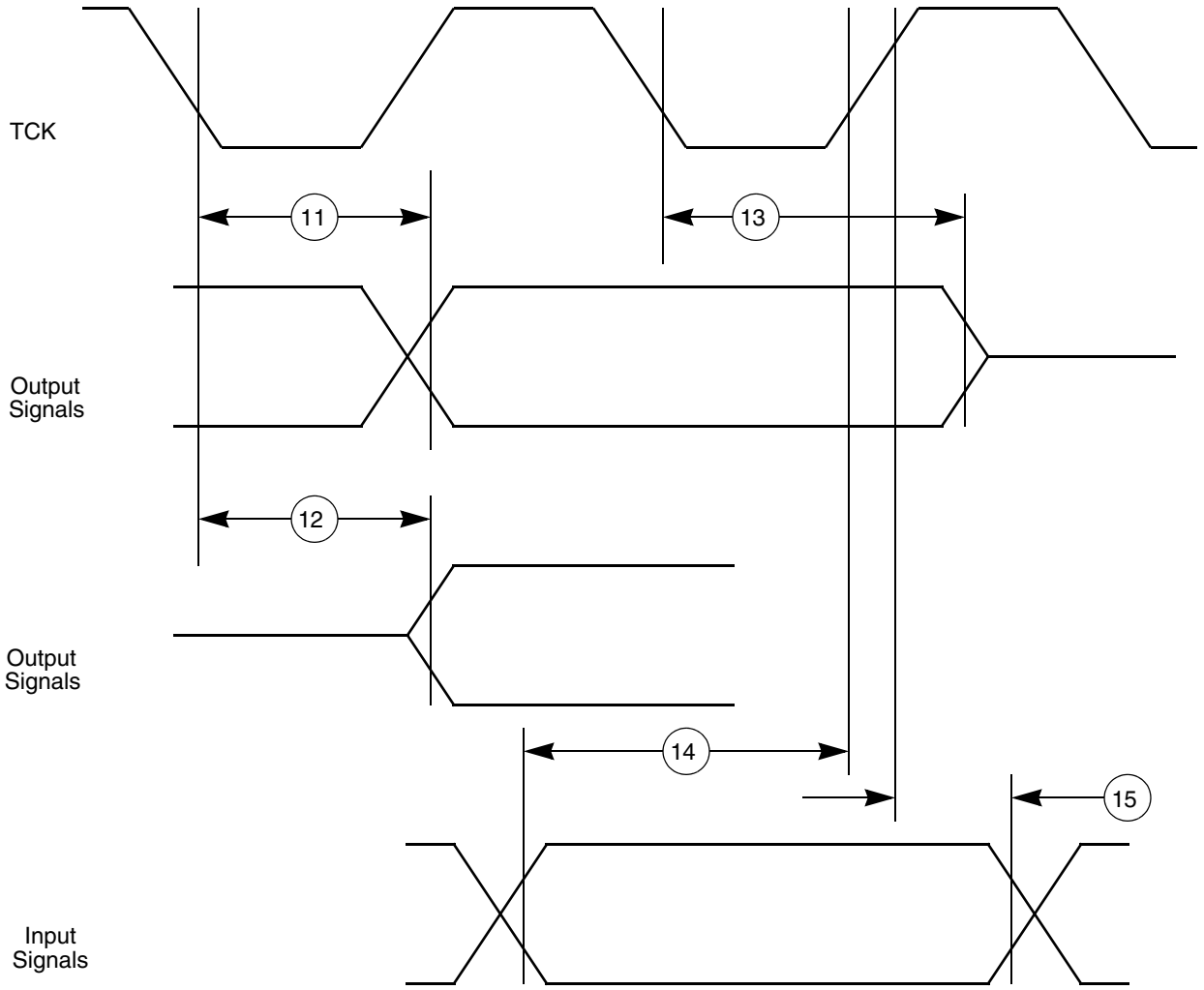


Figure 11. JTAG Boundary Scan Timing

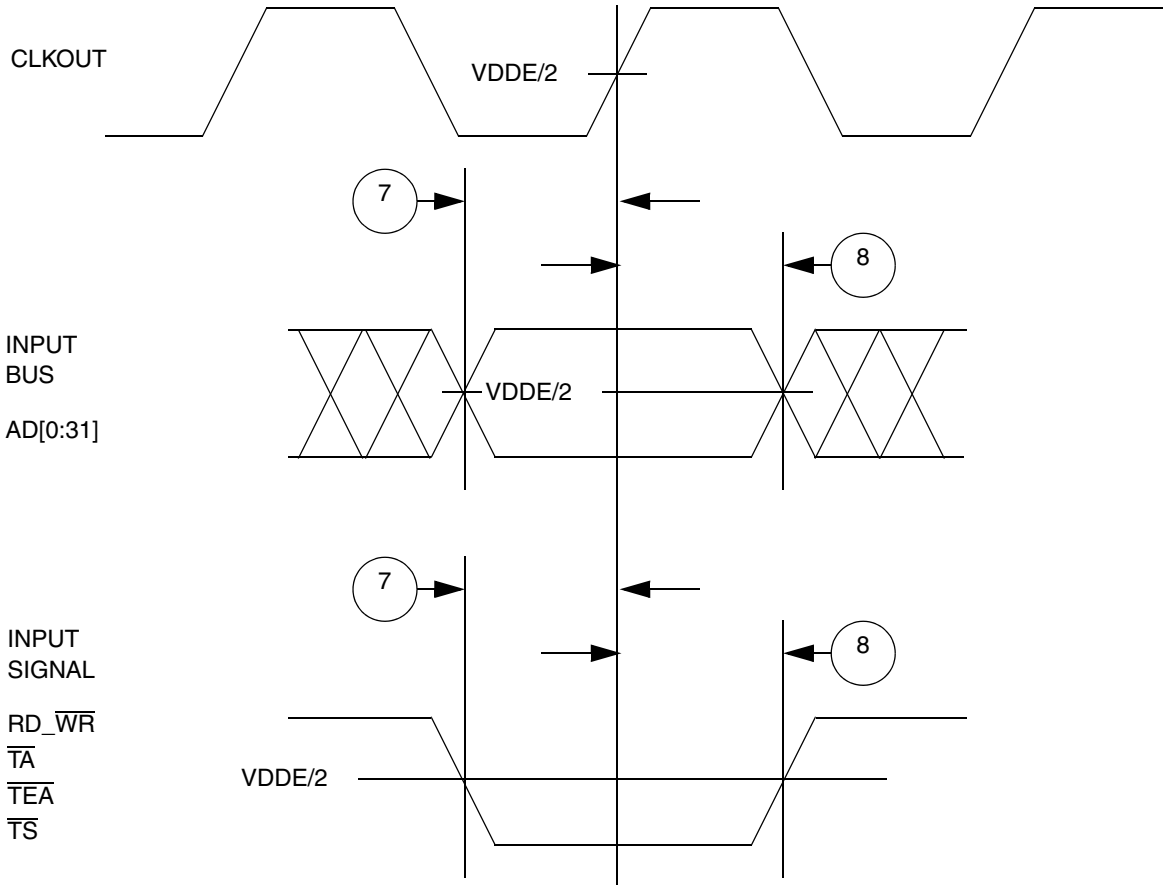


Figure 16. Synchronous Input Timing

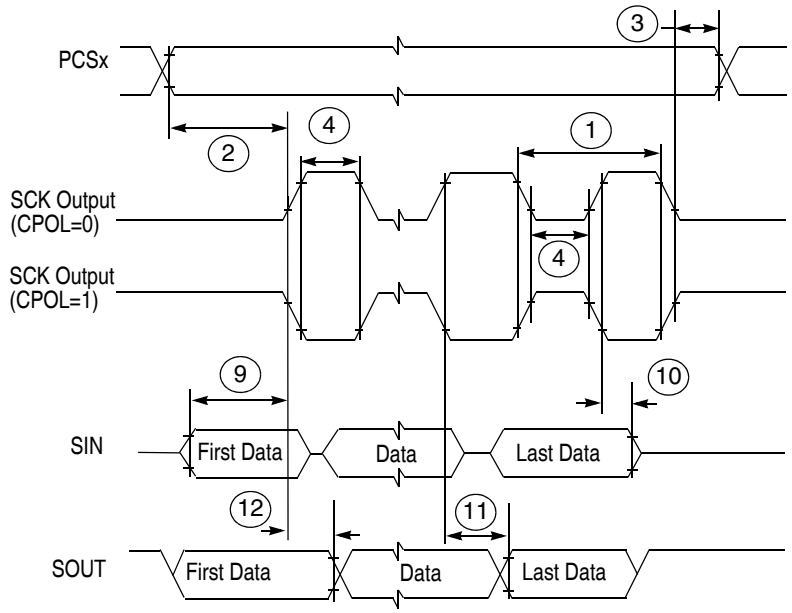


Figure 22. DSPI Modified Transfer Format Timing — Master, CPHA = 0

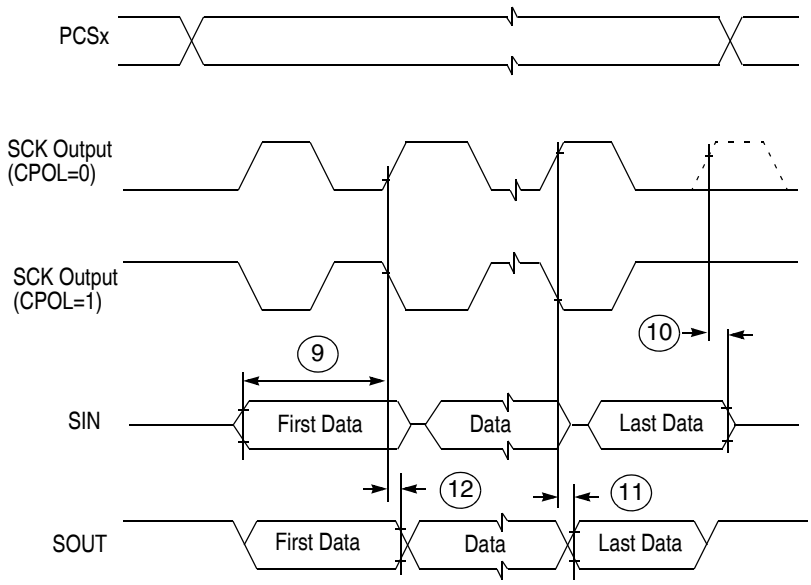


Figure 23. DSPI Modified Transfer Format Timing — Master, CPHA = 1

4.1 Revision History

Table 27 summarizes revisions to this document.

Table 27. Revision History of MPC5510 Data Sheet

Revision	Date	Substantive Changes
Rev. 0	9/2007	Initial Release. Preliminary content.
Rev. 1	6/2008	(Note: Change descriptions refer to locations in Rev. 0.) Changed MPC5516 to MPC5510 Family where appropriate. Modified Figure 1. MPC5510 Family Block Diagram. Deleted Table 1. MPC5510 Family Comparison, Maximum Feature Set Deleted Table 2. MPC5510 Peripheral Multiplexing Examples Corrected PK0 and PK1 pin assignments on 208 MAPBGA (Table 3 and Figure 4). Modified Table 4, footnote 4. Modified Table 8. DC Electrical Specifications and table footnotes. Modified Table 9. Operating Currents and table footnotes. Modified Table 12. 3.3V High Frequency External Oscillator, row 5. Modified Table 14. 5V High Frequency (16 MHz) Internal RC Oscillator, row 2. Modified Table 16. FMPLL Electrical Specifications, row 4. Modified Table 17. eQADC Conversion Specifications (Operating) and table footnotes. Modified Table 18. Flash Program and EraseSpecifications, row 5. Modified Table 19. Flash EEPROM Module Life (Full Temperature Range), row 1 Modified Table 28. Package Information.
Rev. 2	12/2008	(Note: Change descriptions refer to locations in Rev. 1.) Modified Table 1. MPC5510 Signal Properties: added note to TEST signal. Modified Table 6. DC Electrical Specifications: rows 1b, 5, 8, 9, 10, 11, 16, 19, 25, and footnotes. Modified Table 7. Operating Currents: Max column header, rows 1, 2, 3, 4, and footnotes. Modified Table 9. Low Voltage Monitors: rows 2, 3, 4, 6. Modified Table 10. 3.3V High Frequence External Oscillator: row 1 added footnote, removed duplicate footnote #3. Modified Table 11. 5V Low Frequency (32 kHz) External Oscillator: row 1. Modified Table 12. 5V High Frequency (16 MHz) Internal RC Oscillator: row 2. Modified Table 13. 5V Low Frequency (32 kHz) Internal RC Oscillator: row 2. Modified Table 14. FMPLL Electrical Specifications: rows 1 and 4; added two new rows. Modified Table 15. eQADC Conversion Specifications (Operating): rows 5, 6, 7, 8, 10, 11, and footnotes. Modified Figure 5. Pad Output Delay: moved the dashed horizontal line up so that it crosses the signal midway between top and bottom.
Rev. 3	3/2009	(Note: Change descriptions refer to locations in Rev. 2.) Modified Table 4. Thermal Characteristics: all values in 208 MAPBGA column. Modified Table 6. DC Electrical Specifications: spec #1c, added footnote; spec #25, added footnote. Modified Table 7. Operating Currents; spec #5. Modified Table 9. Low Voltage Monitors; spec #1. Modified Table 14. FMPLL Electrical Specifications: updated footnote 3; added spec #10a. Modified Table 15. eQADC Conversion Specifications (Operating): added another footnote. Modified Table 16: Flash Program and Erase Specifications: updated spec #7. Modified Figure 5: Pad Output Delay: adjusted lower timing diagram. Modified Figure 8: JTAG Test Clock Input Timing; updated so that it matches the spec definitions.
Rev. 4	7/2014	Updated the VCO Min. value from 192 to 250 MHz in Table 14., “FMPLL Electrical Specifications.