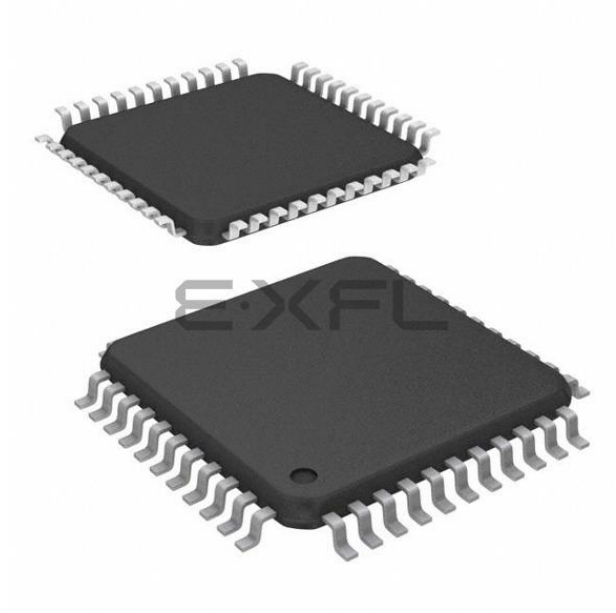


Welcome to E-XFL.COM

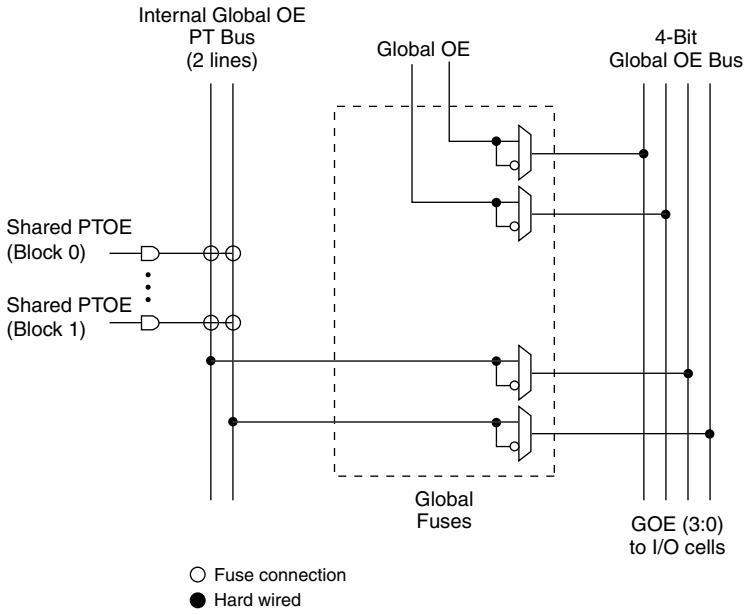
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	30
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032c-75tn44c

Figure 10. Global OE Generation for ispMACH 4032



Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6[1, 2]	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T_j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

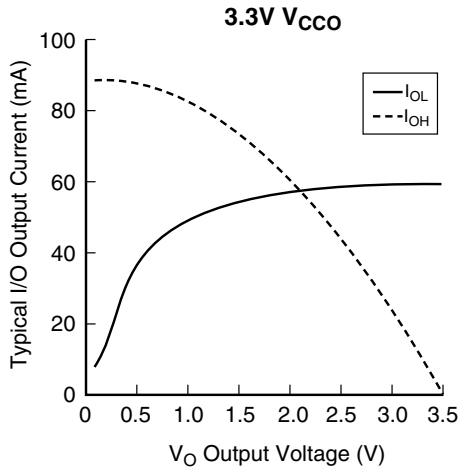
Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

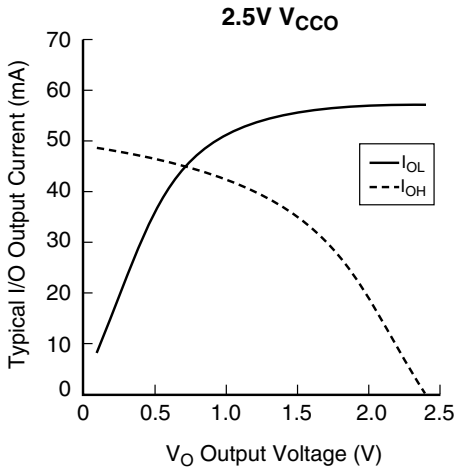
Note: Valid over commercial temperature range.

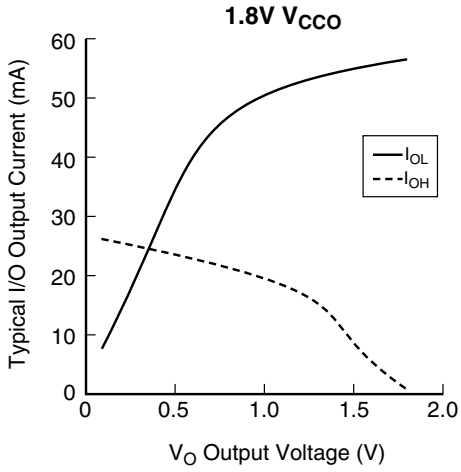
Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.


3.3V V_{CCO}
Typical I/O Output Current (mA)
100
80
60
40
20
0
0 0.5 1.0 1.5 2.0 2.5 3.0 3.5
V_O Output Voltage (V)
I_{OL}
I_{OH}

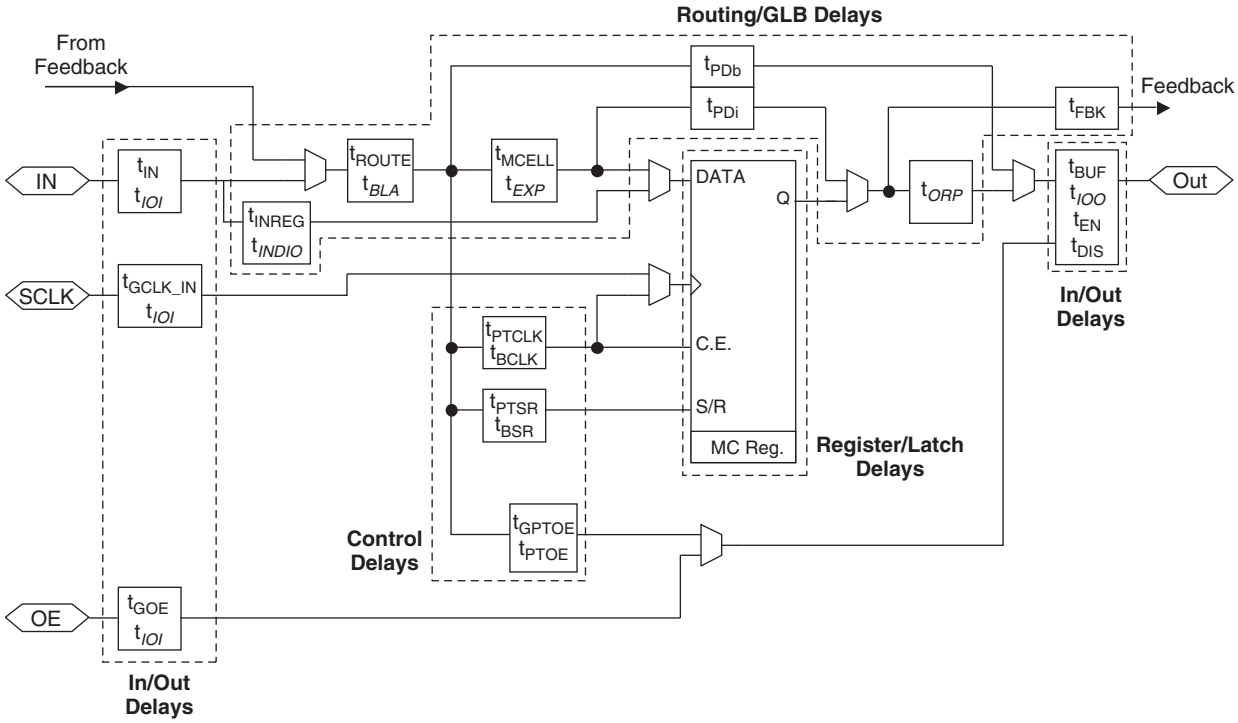

2.5V V_{CCO}
Typical I/O Output Current (mA)
70
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0 2.5
V_O Output Voltage (V)
I_{OL}
I_{OH}


1.8V V_{CCO}
Typical I/O Output Current (mA)
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0
V_O Output Voltage (V)
I_{OL}
I_{OH}

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t_S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_H	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000V/B/C Timing Adders[1] (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.00	—	1.00	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

ispMACH 4000V/B/C/Z Power Supply and NC Connections[1] (Cont.)

Signal	132-ball csBGA[7]	144-pin TQFP[4]	176-pin TQFP[4]	256-ball ftBGA/fpBGA[2, 3, 7, 9]
VCC	P1, A14, B7, N8	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
VCCO0 VCCO (Bank 0)	G3, P5, C1[8], M2[8], C5	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1 VCCO (Bank 1)	M10, M14[8], H12, A10, C13[8]	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	B1, P2, N14, A13	1, 37, 73, 109	2, 46[5], 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank 0)	E2, K2, N4, B4	10, 18[6], 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	N11, K13, E13, B11	55, 65, 82, 90[6], 99, 118	67, 79, 101, 119, 143	
NC	**4064Z:** C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1 **4128Z:** P8, A7	**4128V**: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 **4256V**: 18, 90	1, 43, 44, 45, 89, 131, 132, 133	**4256V/B/C, 128 I/O:** A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15 **4256V/B/C, 160 I/O:** A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15 **4384V/B/C:** B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4 **4512V/B/C:** None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. V_{CCO} balls connect to two power planes within the package, one for V_{CCO0} and one for V_{CCO1}.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
33	1	B10	B^10	D4	D^2	D10	D^5
34	1	B11	B^11	D6	D^3	D8	D^4
35	-	TDO	-	TDO	-	TDO	-
36	-	VCC	-	VCC	-	VCC	-
37	-	GND	-	GND	-	GND	-
38	1	B12	B^12	D8	D^4	D6	D^3
39	1	B13	B^13	D10	D^5	D4	D^2
40	1	B14	B^14	D12	D^6	D2	D^1
41	1	B15/GOE1	B^15	D14/GOE1	D^7	D0/GOE1	D^0
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
44	0	A0/GOE0	A^0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1	A1	A^1
46	0	A2	A^2	A4	A^2	A2	A^2
47	0	A3	A^3	A6	A^3	A4	A^3
48	0	A4	A^4	A8	A^4	A6	A^4

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	TDI	-	TDI	-
C3	0	A5	A^5	A8	A^5
C1	0	A6	A^6	A10	A^6
D1	0	A7	A^7	A11	A^7
D3	0	GND (Bank 0)	-	GND (Bank 0)	-
E3	0	NC[1]	-	I[1]	-
E1	0	NC[1]	-	I[1]	-
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
F1	0	A8	A^8	B15	B^7
G3	0	A9	A^9	B12	B^6
G1	0	A10	A^10	B10	B^5
H1	0	A11	A^11	B8	B^4
J1	0	NC	-	I	-
K1	-	TCK	-	TCK	-
K2	-	VCC	-	VCC	-
H3	-	GND	-	GND	-
K3	-	NC[1]	-	I[1]	-
K4	0	A12	A^12	B6	B^3
H4	0	A13	A^13	B4	B^2
H5	0	A14	A^14	B2	B^1

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3	P12	P^3
85	1	D2	D^2	H4	H^2	P10	P^2
86	1	D1	D^1	H2	H^1	P6	P^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	P^0
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^0
92	0	A1	A^1	A2	A^1	A6	A^1
93	0	A2	A^2	A4	A^2	A10	A^2
94	0	A3	A^3	A6	A^3	A12	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4	B2	B^0
98	0	A5	A^5	A10	A^5	B6	B^1
99	0	A6	A^6	A12	A^6	B10	B^2
100	0	A7	A^7	A14	A^7	B12	B^3

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

		ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
Ball Number	Bank Number	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
P8	1	NC[1]	-	NC[1]	-	I[1]	-
M8	1	NC	-	E0	E^0	I2	I^1
P9	1	C0	C^0	E1	E^1	I4	I^2
N9	1	C1	C^1	E2	E^2	I6	I^3
M9	1	C2	C^2	E4	E^3	I8	I^4
N10	1	C3	C^3	E5	E^4	I10	I^5
P10	1	NC	-	E6	E^5	I12	I^6
M10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
N11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P11	1	NC	-	E8	E^6	J2	J^1
M11	1	C4	C^4	E9	E^7	J4	J^2
P12	1	C5	C^5	E10	E^8	J6	J^3
N12	1	C6	C^6	E12	E^9	J8	J^4
P13	1	C7	C^7	E13	E^10	J10	J^5
P14	1	NC	-	E14	E^11	J12	J^6
N14	-	GND	-	GND	-	GND	-
N13	-	TMS	-	TMS	-	TMS	-
M14	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
M12	1	NC	-	F0	F^0	K12	K^6
M13	1	C8	C^8	F1	F^1	K10	K^5
L14	1	C9	C^9	F2	F^2	K8	K^4
L12	1	C10	C^10	F4	F^3	K6	K^3
L13	1	C11	C^11	F5	F^4	K4	K^2
K14	1	NC	-	F6	F^5	K2	K^1
K13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
K12	1	NC	-	F8	F^6	L12	L^6
J13	1	C12	C^12	F9	F^7	L10	L^5
J14	1	C13	C^13	F10	F^8	L8	L^4
J12	1	C14	C^14	F12	F^9	L6	L^3
H14	1	C15	C^15	F13	F^10	L4	L^2
H13	1	I	-	F14	F^11	L2	L^1
H12	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
G13	1	NC	-	G14	G^11	M2	M^1
G14	1	NC	-	G13	G^10	M4	M^2
G12	1	D15	D^15	G12	G^9	M6	M^3
F14	1	D14	D^14	G10	G^8	M8	M^4
F13	1	D13	D^13	G9	G^7	M10	M^5
F12	1	D12	D^12	G8	G^6	M12	M^6
E13	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
E14	1	NC	-	G6	G^5	N2	N^1
E12	1	D11	D^11	G5	G^4	N4	N^2

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC[2]	-	I[2]	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D^2	E4	E^2	G4	G^2
20	0	D2	D^1	E2	E^1	G2	G^1
21	0	D0	D^0	E0	E^0	G0	G^0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E^0	H0	H^0	J0	J^0
24	0	E2	E^1	H2	H^1	J2	J^1
25	0	E4	E^2	H4	H^2	J4	J^2
26	0	E6	E^3	H6	H^3	J6	J^3
27	0	E8	E^4	H8	H^4	J8	J^4
28	0	E10	E^5	H10	H^5	J10	J^5
29	0	E12	E^6	H12	H^6	J12	J^6
30	0	E14	E^7	H14	H^7	J14	J^7
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F^0	J0	J^0	N0	N^0
33	0	F2	F^1	J2	J^1	N2	N^1
34	0	F4	F^2	J4	J^2	N4	N^2
35	0	F6	F^3	J6	J^3	N6	N^3
36	0	F8	F^4	J8	J^4	N8	N^4
37	0	F10	F^5	J10	J^5	N10	N^5
38	0	F12	F^6	J12	J^6	N12	N^6
39	0	F14	F^7	J14	J^7	N14	N^7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G^7	K14	K^7	O14	O^7
48	0	G12	G^6	K12	K^6	O12	O^6
49	0	G10	G^5	K10	K^5	O10	O^5
50	0	G8	G^4	K8	K^4	O8	O^4
51	0	G6	G^3	K6	K^3	O6	O^3
52	0	G4	G^2	K4	K^2	O4	O^2
53	0	G2	G^1	K2	K^1	O2	O^1
54	0	G0	G^0	K0	K^0	O0	O^0
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H^7	L14	L^7	P14	P^7
58	0	H12	H^6	L12	L^6	P12	P^6
59	0	H10	H^5	L10	L^5	P10	P^5

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E^7	E10	E^7	H14	H^7	J14	J^7
K3	0	NC	-	E12	E^8	G0	G^0	I0	I^0
K4	0	NC	-	E14	E^9	G2	G^1	I4	I^1
L1	0	NC	-	NC	-	I14	I^7	K0	K^0
L2	0	NC	-	NC	-	I12	I^6	K2	K^1
M1	0	NC	-	NC	-	NC	-	K4	K^2
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K^3
N1	0	NC	-	NC	-	I10	I^5	K8	K^4
M3	0	NC	-	NC	-	I8	I^4	K10	K^5
M4	0	NC	-	F0	F^0	G4	G^2	I8	I^2
N2	0	NC	-	F1	F^1	G6	G^3	I12	I^3
K5	0	F0	F^0	F2	F^2	J0	J^0	N0	N^0
P1	0	F2	F^1	F4	F^3	J2	J^1	N2	N^1
K6	0	F4	F^2	F6	F^4	J4	J^2	N4	N^2
N3	0	F6	F^3	F8	F^5	J6	J^3	N6	N^3
L5	0	F8	F^4	F9	F^6	J8	J^4	N8	N^4
P2	0	F10	F^5	F10	F^7	J10	J^5	N10	N^5
L6	0	F12	F^6	F12	F^8	J12	J^6	N12	N^6
R1	0	F14	F^7	F14	F^9	J14	J^7	N14	N^7
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G^9	I6	I^3	K12	K^6
M5	0	NC	-	G12	G^8	I4	I^2	K14	K^7
N4	0	G14	G^7	G10	G^7	K14	K^7	O14	O^7
T3	0	G12	G^6	G9	G^6	K12	K^6	O12	O^6
R3	0	G10	G^5	G8	G^5	K10	K^5	O10	O^5
M6	0	G8	G^4	G6	G^4	K8	K^4	O8	O^4
P4	0	G6	G^3	G4	G^3	K6	K^3	O6	O^3
L7	0	G4	G^2	G2	G^2	K4	K^2	O4	O^2
N5	0	G2	G^1	G1	G^1	K2	K^1	O2	O^1
M7	0	G0	G^0	G0	G^0	K0	K^0	O0	O^0
P5	0	NC	-	NC	-	G8	G^4	M0	M^0
R4	0	NC	-	NC	-	G10	G^5	M4	M^1
T4	0	NC	-	NC	-	NC	-	L0	L^0
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L^1
T5	0	NC	-	NC	-	I2	I^1	L8	L^2
R6	0	NC	-	NC	-	I0	I^0	L12	L^3
T6	0	NC	-	H14	H^9	G12	G^6	M8	M^2
N7	0	NC	-	H12	H^8	G14	G^7	M12	M^3
P7	0	H14	H^7	H10	H^7	L14	L^7	P14	P^7
R7	0	H12	H^6	H9	H^6	L12	L^6	P12	P^6
L8	0	H10	H^5	H8	H^5	L10	L^5	P10	P^5
T7	0	H8	H^4	H6	H^4	L8	L^4	P8	P^4
M8	0	H6	H^3	H4	H^3	L6	L^3	P6	P^3
N8	0	H4	H^2	H2	H^2	L4	L^2	P4	P^2
R8	0	H2	H^1	H1	H^1	L2	L^1	P2	P^1
P8	0	H0	H^0	H0	H^0	L0	L^0	P0	P^0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I^0	I0	I^0	M0	M^0	AX0	AX^0
R9	1	I2	I^1	I1	I^1	M2	M^1	AX2	AX^1
T9	1	I4	I^2	I2	I^2	M4	M^2	AX4	AX^2
T10	1	I6	I^3	I4	I^3	M6	M^3	AX6	AX^3
R10	1	I8	I^4	I6	I^4	M8	M^4	AX8	AX^4
M9	1	I10	I^5	I8	I^5	M10	M^5	AX10	AX^5
P10	1	I12	I^6	I9	I^6	M12	M^6	AX12	AX^6
L9	1	I14	I^7	I10	I^7	M14	M^7	AX14	AX^7
N10	1	NC	-	I12	I^8	BX14	BX^7	DX0	DX^0
T11	1	NC	-	I14	I^9	BX12	BX^6	DX4	DX^1
R11	1	NC	-	NC	-	P0	P^0	EX0	EX^0
T12	1	NC	-	NC	-	P2	P^1	EX4	EX^1
N12	1	NC	-	NC	-	NC	-	EX8	EX^2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX^3
T13	1	NC	-	J0	J^0	BX10	BX^5	DX8	DX^2
P12	1	NC	-	J1	J^1	BX8	BX^4	DX12	DX^3
M10	1	J0	J^0	J2	J^2	N0	N^0	BX0	BX^0
R13	1	J2	J^1	J4	J^3	N2	N^1	BX2	BX^1
L10	1	J4	J^2	J6	J^4	N4	N^2	BX4	BX^2
T14	1	J6	J^3	J8	J^5	N6	N^3	BX6	BX^3
M11	1	J8	J^4	J9	J^6	N8	N^4	BX8	BX^4

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J^5	J10	J^7	N10	N^5	BX10	BX^5
P13	1	J12	J^6	J12	J^8	N12	N^6	BX12	BX^6
N13	1	J14	J^7	J14	J^9	N14	N^7	BX14	BX^7
M12	1	NC	-	NC	-	P4	P^2	FX0	FX^0
T15	1	NC	-	NC	-	P6	P^3	FX2	FX^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX^2
R16	1	NC	-	NC	-	P8	P^4	FX6	FX^3
N14	1	NC	-	NC	-	P10	P^5	FX8	FX^4
P15	1	K14	K^7	K14	K^9	O14	O^7	CX14	CX^7
L11	1	K12	K^6	K12	K^8	O12	O^6	CX12	CX^6
P16	1	K10	K^5	K10	K^7	O10	O^5	CX10	CX^5
K11	1	K8	K^4	K9	K^6	O8	O^4	CX8	CX^4
M14	1	K6	K^3	K8	K^5	O6	O^3	CX6	CX^3
K12	1	K4	K^2	K6	K^4	O4	O^2	CX4	CX^2
N15	1	K2	K^1	K4	K^3	O2	O^1	CX2	CX^1
N16	1	K0	K^0	K2	K^2	O0	O^0	CX0	CX^0
M15	1	NC	-	K1	K^1	BX6	BX^3	HX0	HX^0
M13	1	NC	-	K0	K^0	BX4	BX^2	HX4	HX^1
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX^5
L15	1	NC	-	NC	-	P12	P^6	FX12	FX^6
L16	1	NC	-	NC	-	P14	P^7	FX14	FX^7
J11	1	NC	-	L14	L^9	BX2	BX^1	HX8	HX^2
K15	1	NC	-	L12	L^8	BX0	BX^0	HX12	HX^3
J12	1	L14	L^7	L10	L^7	AX14	AX^7	GX14	GX^7
K13	1	L12	L^6	L9	L^6	AX12	AX^6	GX12	GX^6
K14	1	L10	L^5	L8	L^5	AX10	AX^5	GX10	GX^5
K16	1	L8	L^4	L6	L^4	AX8	AX^4	GX8	GX^4
J16	1	L6	L^3	L4	L^3	AX6	AX^3	GX6	GX^3
J15	1	L4	L^2	L2	L^2	AX4	AX^2	GX4	GX^2
H16	1	L2	L^1	L1	L^1	AX2	AX^1	GX2	GX^1
J13	1	L0	L^0	L0	L^0	AX0	AX^0	GX0	GX^0
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M^0	M0	M^0	DX0	DX^0	JX0	JX^0

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C[1]	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C[1]	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C[1]	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI[1]	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI[1]	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI[1]	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI[1]	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI[1]	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI[1]	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
	LC4256V-10T100I	256	3.3	10	TQFP	100	64	I
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I[1]	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I[1]	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I[1]	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I[1]	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I[1]	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I[1]	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FTN256AI	256	3.3	5	Lead-free ftBGA	256	128	I
	LC4256V-75FTN256AI	256	3.3	7.5	Lead-free ftBGA	256	128	I
	LC4256V-10FTN256AI	256	3.3	10	Lead-free ftBGA	256	128	I
	LC4256V-5FTN256BI	256	3.3	5	Lead-free ftBGA	256	160	I
	LC4256V-75FTN256BI	256	3.3	7.5	Lead-free ftBGA	256	160	I
	LC4256V-10FTN256BI	256	3.3	10	Lead-free ftBGA	256	160	I
	LC4256V-5FN256AI[1]	256	3.3	5	Lead-free fpBGA	256	128	I
	LC4256V-75FN256AI[1]	256	3.3	7.5	Lead-free fpBGA	256	128	I
	LC4256V-10FN256AI[1]	256	3.3	10	Lead-free fpBGA	256	128	I
	LC4256V-5FN256BI[1]	256	3.3	5	Lead-free fpBGA	256	160	I
	LC4256V-75FN256BI[1]	256	3.3	7.5	Lead-free fpBGA	256	160	I
	LC4256V-10FN256BI[1]	256	3.3	10	Lead-free fpBGA	256	160	I
	LC4256V-5TN176I	256	3.3	5	Lead-free TQFP	176	128	I
	LC4256V-75TN176I	256	3.3	7.5	Lead-free TQFP	176	128	I
	LC4256V-10TN176I	256	3.3	10	Lead-free TQFP	176	128	I
	LC4256V-5TN144I	256	3.3	5	Lead-free TQFP	144	96	I
	LC4256V-75TN144I	256	3.3	7.5	Lead-free TQFP	144	96	I
	LC4256V-10TN144I	256	3.3	10	Lead-free TQFP	144	96	I
	LC4256V-5TN100I	256	3.3	5	Lead-free TQFP	100	64	I
	LC4256V-75TN100I	256	3.3	7.5	Lead-free TQFP	100	64	I
	LC4256V-10TN100I	256	3.3	10	Lead-free TQFP	100	64	I
LC4384V	LC4384V-5FTN256I	384	3.3	5	Lead-free ftBGA	256	192	I
	LC4384V-75FTN256I	384	3.3	7.5	Lead-free ftBGA	256	192	I
	LC4384V-10FTN256I	384	3.3	10	Lead-free ftBGA	256	192	I
	LC4384V-5FN256I[1]	384	3.3	5	Lead-free fpBGA	256	192	I
	LC4384V-75FN256I[1]	384	3.3	7.5	Lead-free fpBGA	256	192	I
	LC4384V-10FN256I[1]	384	3.3	10	Lead-free fpBGA	256	192	I
	LC4384V-5TN176I	384	3.3	5	Lead-free TQFP	176	128	I
	LC4384V-75TN176I	384	3.3	7.5	Lead-free TQFP	176	128	I
	LC4384V-10TN176I	384	3.3	10	Lead-free TQFP	176	128	I
LC4512V	LC4512V-5FTN256I	512	3.3	5	Lead-free ftBGA	256	208	I
	LC4512V-75FTN256I	512	3.3	7.5	Lead-free ftBGA	256	208	I
	LC4512V-10FTN256I	512	3.3	10	Lead-free ftBGA	256	208	I
	LC4512V-5FN256I[1]	512	3.3	5	Lead-free fpBGA	256	208	I
	LC4512V-75FN256I[1]	512	3.3	7.5	Lead-free fpBGA	256	208	I
	LC4512V-10FN256I[1]	512	3.3	10	Lead-free fpBGA	256	208	I
	LC4512V-5TN176I	512	3.3	5	Lead-free TQFP	176	128	I
	LC4512V-75TN176I	512	3.3	7.5	Lead-free TQFP	176	128	I
	LC4512V-10TN176I	512	3.3	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150µA to -200µA.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.