



Welcome to [E·XFL.COM](https://www.e-xfl.com)

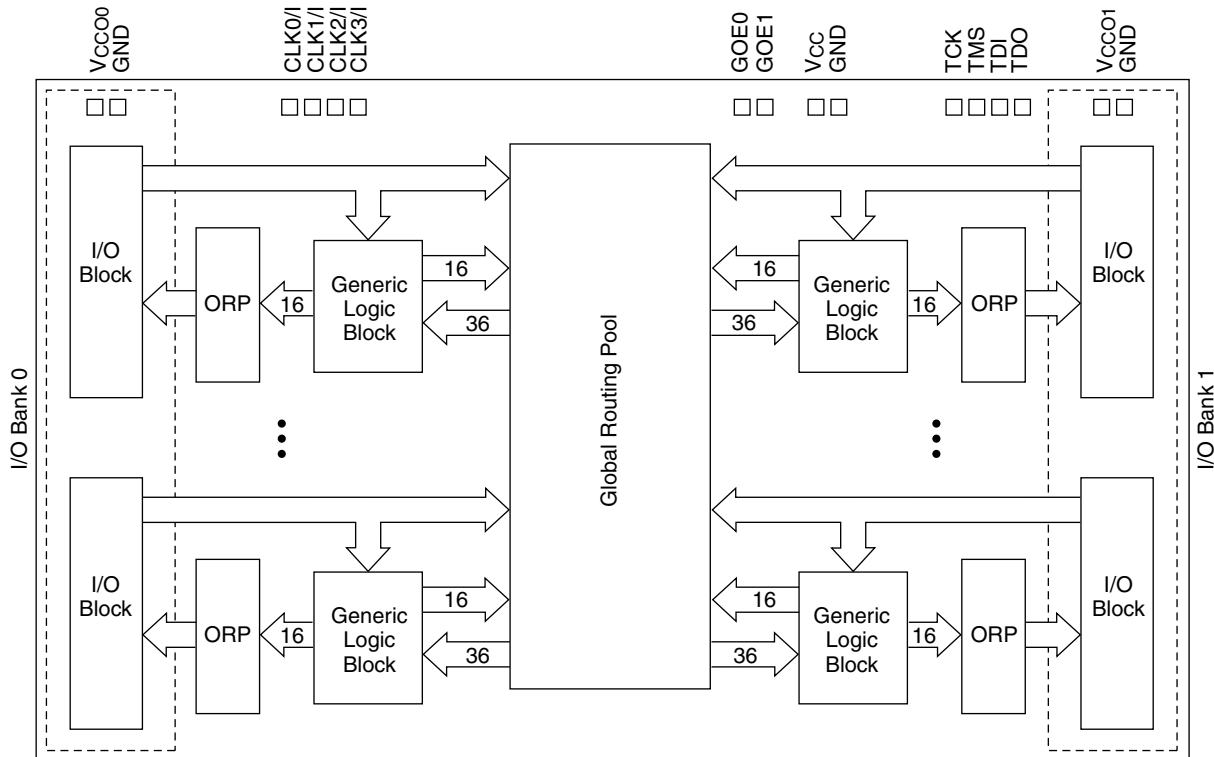
Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032c-75tn48c

Figure 1. Functional Block Diagram

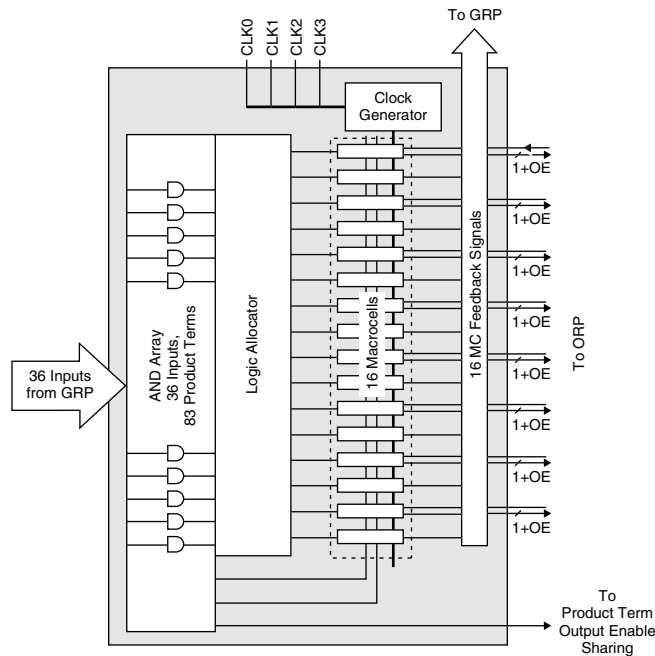
The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CC0} of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

Absolute Maximum Ratings^{1, 2, 3}

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied ^{4, 5}	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V _{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6 ^{1, 2}	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T _j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics^{1,2,3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, $T_j = 105^\circ C$	—	± 30	± 150	μA
		$0 \leq V_{IN} \leq 3.0V$, $T_j = 130^\circ C$	—	± 30	± 200	μA

1. Insensitive to sequence of V_{CC} or V_{CCO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
2. $0 < V_{CC} < V_{CC} (MAX)$, $0 < V_{CCO} < V_{CCO} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} . Device defaults to pull-up until fuse circuitry is active.

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	341	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	361	—	μA
		V _{CC} = 1.9V, T _A = 85°C	—	372	—	μA
		V _{CC} = 1.9V, T _A = 125°C	—	468	—	μA
ICC ^{4, 5}	Standby Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	13	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	32	55	μA
		V _{CC} = 1.9V, T _A = 85°C	—	43	90	μA
		V _{CC} = 1.9V, T _A = 125°C	—	135	—	μA

1. T_A = 25°C, frequency = 1.0 MHz.

2. Device configured with 16-bit counters.

3. I_{CC} varies with specific device configuration and operating frequency.

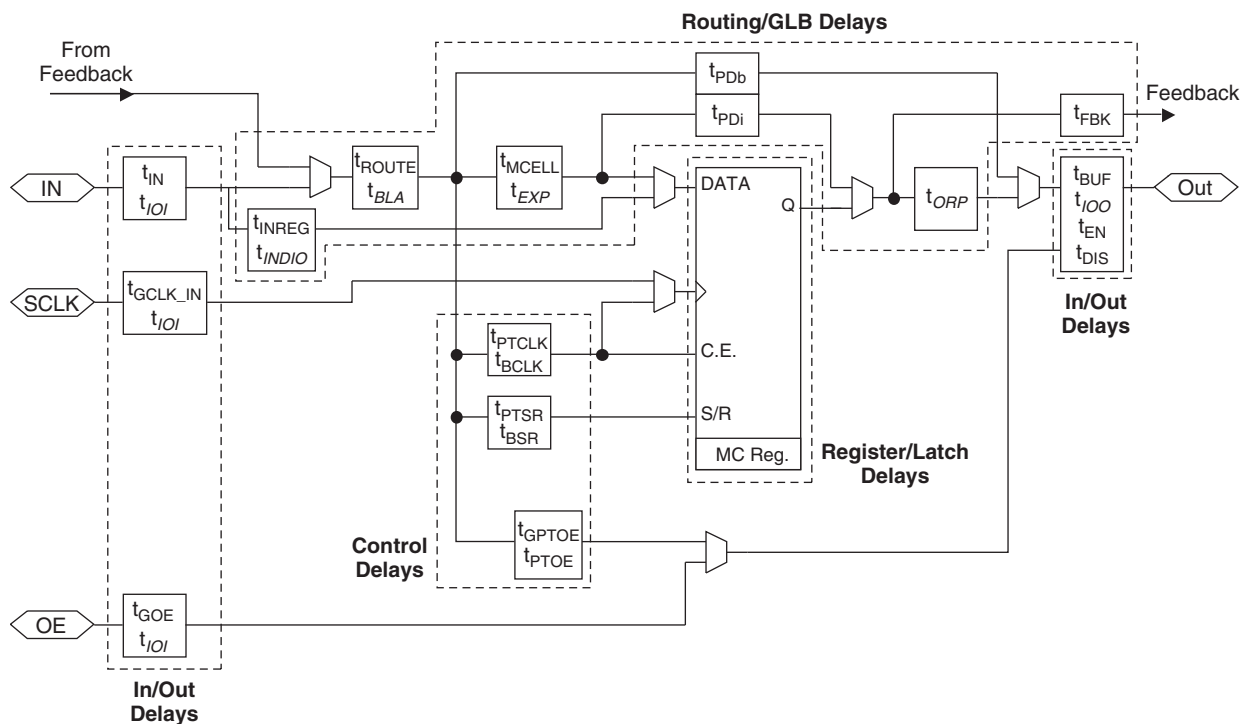
4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.

5. Includes V_{CCO} current without output loading.

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#).

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.95	—	1.50	—	2.00	ns
t _{GOE}	Global OE Pin Delay	—	4.04	—	6.04	—	7.04	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.83	—	2.28	—	3.28	ns
t _{BUF}	Delay through Output Buffer	—	1.00	—	1.50	—	1.50	ns
t _{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	ns
t _{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	1.51	—	2.26	—	3.26	ns
t _{MCELL}	Macrocell Delay	—	1.05	—	1.45	—	1.95	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.56	—	0.96	—	1.46	ns
t _{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	1.54	—	2.24	—	3.24	ns
t _{PDi}	Macrocell Propagation Delay	—	0.94	—	1.24	—	1.74	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.52	—	1.77	—	1.77	—	ns
t _{ST_PT}	T-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t _H	D-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t _{HT}	T-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	1.52	—	1.57	—	1.57	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	0.68	—	1.18	—	1.18	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.68	—	1.18	—	1.18	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.67	—	1.17	ns
t _{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	ns
t _{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	ns
t _{SL}	Latch Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t _{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t _{SRI}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	ns
t _{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	0.62	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	2.51	—	3.41	—	3.41	ns

ispMACH 4000Z Timing Adders ¹

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block load-ing adder	—	0.04	—	0.05	—	0.05	ns
t _{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t _{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:
44-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A ²	A4	A ²
43	0	A3	A ³	A6	A ³
44	0	A4	A ⁴	A8	A ⁴

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-	TDI	-
2	0	A5	A ⁵	A10	A ⁵	A8	A ⁵
3	0	A6	A ⁶	A12	A ⁶	A10	A ⁶
4	0	A7	A ⁷	A14	A ⁷	A11	A ⁷
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A ⁸	B0	B ⁰	B15	B ⁷
8	0	A9	A ⁹	B2	B ¹	B12	B ⁶
9	0	A10	A ¹⁰	B4	B ²	B10	B ⁵
10	0	A11	A ¹¹	B6	B ³	B8	B ⁴
11	-	TCK	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-	VCC	-
13	-	GND	-	GND	-	GND	-
14	0	A12	A ¹²	B8	B ⁴	B6	B ³
15	0	A13	A ¹³	B10	B ⁵	B4	B ²
16	0	A14	A ¹⁴	B12	B ⁶	B2	B ¹
17	0	A15	A ¹⁵	B14	B ⁷	B0	B ⁰
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
20	1	B0	B ⁰	C0	C ⁰	C0	C ⁰
21	1	B1	B ¹	C2	C ¹	C1	C ¹
22	1	B2	B ²	C4	C ²	C2	C ²
23	1	B3	B ³	C6	C ³	C4	C ³
24	1	B4	B ⁴	C8	C ⁴	C6	C ⁴
25	-	TMS	-	TMS	-	TMS	-
26	1	B5	B ⁵	C10	C ⁵	C8	C ⁵
27	1	B6	B ⁶	C12	C ⁶	C10	C ⁶
28	1	B7	B ⁷	C14	C ⁷	C11	C ⁷
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B ⁸	D0	D ⁰	D15	D ⁷
32	1	B9	B ⁹	D2	D ¹	D12	D ⁶

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E3	0	NC	-	B8	B ⁶	D12	D ⁶
F2	0	A12	A ¹²	B9	B ⁷	D10	D ⁵
F1	0	A13	A ¹³	B10	B ⁸	D8	D ⁴
F3	0	A14	A ¹⁴	B12	B ⁹	D6	D ³
G1	0	A15	A ¹⁵	B13	B ¹⁰	D4	D ²
G2	0	I	-	B14	B ¹¹	D2	D ¹
G3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
H2	0	NC	-	C14	C ¹¹	E2	E ¹
H1	0	B15	B ¹⁵	C13	C ¹⁰	E4	E ²
H3	0	B14	B ¹⁴	C12	C ⁹	E6	E ³
J1	0	B13	B ¹³	C10	C ⁸	E8	E ⁴
J2	0	B12	B ¹²	C9	C ⁷	E10	E ⁵
J3	0	NC	-	C8	C ⁶	E12	E ⁶
K2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
K1	0	NC	-	C6	C ⁵	F2	F ¹
K3	0	B11	B ¹¹	C5	C ⁴	F4	F ²
L2	0	B10	B ¹⁰	C4	C ³	F6	F ³
L1	0	B9	B ⁹	C2	C ²	F8	F ⁴
L3	0	B8	B ⁸	C1	C ¹	F10	F ⁵
M1	0	I	-	C0	C ⁰	F12	F ⁶
M2	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N1	-	TCK	-	TCK	-	TCK	-
P1	-	VCC	-	VCC	-	VCC	-
P2	-	GND	-	GND	-	GND	-
N2	0	I	-	D14	D ¹¹	G12	G ⁶
P3	0	B7	B ⁷	D13	D ¹⁰	G10	G ⁵
M3	0	B6	B ⁶	D12	D ⁹	G8	G ⁴
N3	0	B5	B ⁵	D10	D ⁸	G6	G ³
P4	0	B4	B ⁴	D9	D ⁷	G4	G ²
M4	0	NC	-	D8	D ⁶	G2	G ¹
N4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
P5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N5	0	NC	-	D6	D ⁵	H12	H ⁶
M5	0	B3	B ³	D5	D ⁴	H10	H ⁵
N6	0	B2	B ²	D4	D ³	H8	H ⁴
P6	0	B1	B ¹	D2	D ²	H6	H ³
M6	0	B0	B ⁰	D1	D ¹	H4	H ²
P7	0	NC	-	D0	D ⁰	H2	H ¹
N7	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
M7	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
N8	-	VCC	-	VCC	-	VCC	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
129	-	VCC	-	VCC	-
130	0	A0/GOE0	A^0	A2/GOE0	A^1
131	0	A1	A^1	A4	A^2
132	0	A2	A^2	A6	A^3
133	0	A4	A^3	A8	A^4
134	0	A5	A^4	A10	A^5
135	0	A6	A^5	A12	A^6
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
137	0	GND (Bank 0)	-	GND (Bank 0)	-
138	0	A8	A^6	B2	B^1
139	0	A9	A^7	B4	B^2
140	0	A10	A^8	B6	B^3
141	0	A12	A^9	B8	B^4
142	0	A13	A^10	B10	B^5
143	0	A14	A^11	B12	B^6
144	0	NC ²	-	I ²	-

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.

2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	NC	-	NC	-	NC	-
2	-	GND	-	GND	-	GND	-
3	-	TDI	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1	C2	C^1
12	0	C0	C^0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	E14	E^7	G14	G^7
15	0	D12	D^6	E12	E^6	G12	G^6
16	0	D10	D^5	E10	E^5	G10	G^5
17	0	D8	D^4	E8	E^4	G8	G^4
18	0	D6	D^3	E6	E^3	G6	G^3

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D [^] 2	E4	E [^] 2	G4	G [^] 2
20	0	D2	D [^] 1	E2	E [^] 1	G2	G [^] 1
21	0	D0	D [^] 0	E0	E [^] 0	G0	G [^] 0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E [^] 0	H0	H [^] 0	J0	J [^] 0
24	0	E2	E [^] 1	H2	H [^] 1	J2	J [^] 1
25	0	E4	E [^] 2	H4	H [^] 2	J4	J [^] 2
26	0	E6	E [^] 3	H6	H [^] 3	J6	J [^] 3
27	0	E8	E [^] 4	H8	H [^] 4	J8	J [^] 4
28	0	E10	E [^] 5	H10	H [^] 5	J10	J [^] 5
29	0	E12	E [^] 6	H12	H [^] 6	J12	J [^] 6
30	0	E14	E [^] 7	H14	H [^] 7	J14	J [^] 7
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F [^] 0	J0	J [^] 0	N0	N [^] 0
33	0	F2	F [^] 1	J2	J [^] 1	N2	N [^] 1
34	0	F4	F [^] 2	J4	J [^] 2	N4	N [^] 2
35	0	F6	F [^] 3	J6	J [^] 3	N6	N [^] 3
36	0	F8	F [^] 4	J8	J [^] 4	N8	N [^] 4
37	0	F10	F [^] 5	J10	J [^] 5	N10	N [^] 5
38	0	F12	F [^] 6	J12	J [^] 6	N12	N [^] 6
39	0	F14	F [^] 7	J14	J [^] 7	N14	N [^] 7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G [^] 7	K14	K [^] 7	O14	O [^] 7
48	0	G12	G [^] 6	K12	K [^] 6	O12	O [^] 6
49	0	G10	G [^] 5	K10	K [^] 5	O10	O [^] 5
50	0	G8	G [^] 4	K8	K [^] 4	O8	O [^] 4
51	0	G6	G [^] 3	K6	K [^] 3	O6	O [^] 3
52	0	G4	G [^] 2	K4	K [^] 2	O4	O [^] 2
53	0	G2	G [^] 1	K2	K [^] 1	O2	O [^] 1
54	0	G0	G [^] 0	K0	K [^] 0	O0	O [^] 0
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H [^] 7	L14	L [^] 7	P14	P [^] 7
58	0	H12	H [^] 6	L12	L [^] 6	P12	P [^] 6
59	0	H10	H [^] 5	L10	L [^] 5	P10	P [^] 5

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C ⁷	C14	C ⁹	C14	C ⁷	C14	C ⁷
F5	0	C12	C ⁶	C12	C ⁸	C12	C ⁶	C12	C ⁶
D3	0	C10	C ⁵	C10	C ⁷	C10	C ⁵	C10	C ⁵
C1	0	C8	C ⁴	C9	C ⁶	C8	C ⁴	C8	C ⁴
C2	0	C6	C ³	C8	C ⁵	C6	C ³	C6	C ³
E3	0	C4	C ²	C6	C ⁴	C4	C ²	C4	C ²
D2	0	C2	C ¹	C4	C ³	C2	C ¹	C2	C ¹
F6	0	C0	C ⁰	C2	C ²	C0	C ⁰	C0	C ⁰
D1	0	NC	-	C1	C ¹	F6	F ³	H0	H ⁰
E2	0	NC	-	C0	C ⁰	F4	F ²	H4	H ¹
E4	0	NC	-	NC	-	D6	D ³	F4	F ²
G5	0	NC	-	NC	-	D4	D ²	F6	F ³
E1	0	NC	-	NC	-	NC	-	F8	F ⁴
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F ⁵
F1	0	NC	-	NC	-	D2	D ¹	F12	F ⁶
G1	0	NC	-	NC	-	D0	D ⁰	F14	F ⁷
G6	0	NC	-	D14	D ⁹	F2	F ¹	H8	H ²
G4	0	NC	-	D12	D ⁸	F0	F ⁰	H12	H ³
H6	0	D14	D ⁷	D10	D ⁷	E14	E ⁷	G14	G ⁷
G3	0	D12	D ⁶	D9	D ⁶	E12	E ⁶	G12	G ⁶
H5	0	D10	D ⁵	D8	D ⁵	E10	E ⁵	G10	G ⁵
G2	0	D8	D ⁴	D6	D ⁴	E8	E ⁴	G8	G ⁴
H1	0	D6	D ³	D4	D ³	E6	E ³	G6	G ³
H2	0	D4	D ²	D2	D ²	E4	E ²	G4	G ²
H3	0	D2	D ¹	D1	D ¹	E2	E ¹	G2	G ¹
H4	0	D0	D ⁰	D0	D ⁰	E0	E ⁰	G0	G ⁰
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E ⁰	E0	E ⁰	H0	H ⁰	J0	J ⁰
J3	0	E2	E ¹	E1	E ¹	H2	H ¹	J2	J ¹
J2	0	E4	E ²	E2	E ²	H4	H ²	J4	J ²
J1	0	E6	E ³	E4	E ³	H6	H ³	J6	J ³
K1	0	E8	E ⁴	E6	E ⁴	H8	H ⁴	J8	J ⁴
J5	0	E10	E ⁵	E8	E ⁵	H10	H ⁵	J10	J ⁵
K2	0	E12	E ⁶	E9	E ⁶	H12	H ⁶	J12	J ⁶

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J ⁵	J10	J ⁷	N10	N ⁵	BX10	BX ⁵
P13	1	J12	J ⁶	J12	J ⁸	N12	N ⁶	BX12	BX ⁶
N13	1	J14	J ⁷	J14	J ⁹	N14	N ⁷	BX14	BX ⁷
M12	1	NC	-	NC	-	P4	P ²	FX0	FX ⁰
T15	1	NC	-	NC	-	P6	P ³	FX2	FX ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX ²
R16	1	NC	-	NC	-	P8	P ⁴	FX6	FX ³
N14	1	NC	-	NC	-	P10	P ⁵	FX8	FX ⁴
P15	1	K14	K ⁷	K14	K ⁹	O14	O ⁷	CX14	CX ⁷
L11	1	K12	K ⁶	K12	K ⁸	O12	O ⁶	CX12	CX ⁶
P16	1	K10	K ⁵	K10	K ⁷	O10	O ⁵	CX10	CX ⁵
K11	1	K8	K ⁴	K9	K ⁶	O8	O ⁴	CX8	CX ⁴
M14	1	K6	K ³	K8	K ⁵	O6	O ³	CX6	CX ³
K12	1	K4	K ²	K6	K ⁴	O4	O ²	CX4	CX ²
N15	1	K2	K ¹	K4	K ³	O2	O ¹	CX2	CX ¹
N16	1	K0	K ⁰	K2	K ²	O0	O ⁰	CX0	CX ⁰
M15	1	NC	-	K1	K ¹	BX6	BX ³	HX0	HX ⁰
M13	1	NC	-	K0	K ⁰	BX4	BX ²	HX4	HX ¹
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX ⁵
L15	1	NC	-	NC	-	P12	P ⁶	FX12	FX ⁶
L16	1	NC	-	NC	-	P14	P ⁷	FX14	FX ⁷
J11	1	NC	-	L14	L ⁹	BX2	BX ¹	HX8	HX ²
K15	1	NC	-	L12	L ⁸	BX0	BX ⁰	HX12	HX ³
J12	1	L14	L ⁷	L10	L ⁷	AX14	AX ⁷	GX14	GX ⁷
K13	1	L12	L ⁶	L9	L ⁶	AX12	AX ⁶	GX12	GX ⁶
K14	1	L10	L ⁵	L8	L ⁵	AX10	AX ⁵	GX10	GX ⁵
K16	1	L8	L ⁴	L6	L ⁴	AX8	AX ⁴	GX8	GX ⁴
J16	1	L6	L ³	L4	L ³	AX6	AX ³	GX6	GX ³
J15	1	L4	L ²	L2	L ²	AX4	AX ²	GX4	GX ²
H16	1	L2	L ¹	L1	L ¹	AX2	AX ¹	GX2	GX ¹
J13	1	L0	L ⁰	L0	L ⁰	AX0	AX ⁰	GX0	GX ⁰
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M ⁰	M0	M ⁰	DX0	DX ⁰	JX0	JX ⁰

Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispMACH 4000Z devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

Conventional Packaging

ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35M56C	32	1.8	3.5	csBGA	56	32	C
	LC4032ZC-5M56C	32	1.8	5	csBGA	56	32	C
	LC4032ZC-75M56C	32	1.8	7.5	csBGA	56	32	C
	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32	C
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32	C
LC4064ZC	LC4064ZC-37M132C	64	1.8	3.7	csBGA	132	64	C
	LC4064ZC-5M132C	64	1.8	5	csBGA	132	64	C
	LC4064ZC-75M132C	64	1.8	7.5	csBGA	132	64	C
	LC4064ZC-37T100C	64	1.8	3.7	TQFP	100	64	C
	LC4064ZC-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064ZC-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064ZC-37M56C	64	1.8	3.7	csBGA	56	32	C
	LC4064ZC-5M56C	64	1.8	5	csBGA	56	32	C
	LC4064ZC-75M56C	64	1.8	7.5	csBGA	56	32	C
	LC4064ZC-37T48C	64	1.8	3.7	TQFP	48	32	C
	LC4064ZC-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064ZC-75T48C	64	1.8	7.5	TQFP	48	32	C
LC4128ZC	LC4128ZC-42M132C	128	1.8	4.2	csBGA	132	96	C
	LC4128ZC-75M132C	128	1.8	7.5	csBGA	132	96	C
	LC4128ZC-42T100C	128	1.8	4.2	TQFP	100	64	C
	LC4128ZC-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256ZC	LC4256ZC-45T176C	256	1.8	4.5	TQFP	176	128	C
	LC4256ZC-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256ZC-45M132C	256	1.8	4.5	csBGA	132	96	C
	LC4256ZC-75M132C	256	1.8	7.5	csBGA	132	96	C
	LC4256ZC-45T100C	256	1.8	4.5	TQFP	100	64	C
	LC4256ZC-75T100C	256	1.8	7.5	TQFP	100	64	C

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5M56I	32	1.8	5	csBGA	56	32	I
	LC4032ZC-75M56I	32	1.8	7.5	csBGA	56	32	I
	LC4032ZC-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032ZC-75T48I	32	1.8	7.5	TQFP	48	32	I

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5M132I	64	1.8	5	csBGA	132	64	I
	LC4064ZC-75M132I	64	1.8	7.5	csBGA	132	64	I
	LC4064ZC-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064ZC-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064ZC-5M56I	64	1.8	5	csBGA	56	34	I
	LC4064ZC-75M56I	64	1.8	7.5	csBGA	56	34	I
	LC4064ZC-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064ZC-75T48I	64	1.8	7.5	TQFP	48	32	I
LC4128ZC	LC4128ZC-75M132I	128	1.8	7.5	csBGA	132	96	I
	LC4128ZC-75T100I	128	1.8	7.5	TQFP	100	64	I
LC4256ZC	LC4256ZC-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256ZC-75M132I	256	1.8	7.5	csBGA	132	96	I
	LC4256ZC-75T100I	256	1.8	7.5	TQFP	100	64	I

ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75T48E	32	1.8	7.5	TQFP	48	32	E
LC4064ZC	LC4064ZC-75T100E	64	1.8	7.5	TQFP	100	64	E
	LC4064ZC-75T48E	64	1.8	7.5	TQFP	48	32	E
LC4128ZC	LC4128ZC-75T100E	128	1.8	7.5	TQFP	100	64	E
LC4256ZC	LC4256ZC-75T176E	256	1.8	7.5	TQFP	176	128	E
	LC4256ZC-75T100E	256	1.8	7.5	TQFP	100	64	E

ispMACH 4000C (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25T48C	32	1.8	2.5	TQFP	48	32	C
	LC4032C-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032C-75T48C	32	1.8	7.5	TQFP	48	32	C
	LC4032C-25T44C	32	1.8	2.5	TQFP	44	30	C
	LC4032C-5T44C	32	1.8	5	TQFP	44	30	C
	LC4032C-75T44C	32	1.8	7.5	TQFP	44	30	C
LC4064C	LC4064C-25T100C	64	1.8	2.5	TQFP	100	64	C
	LC4064C-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064C-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064C-25T48C	64	1.8	2.5	TQFP	48	32	C
	LC4064C-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064C-75T48C	64	1.8	7.5	TQFP	48	32	C
	LC4064C-25T44C	64	1.8	2.5	TQFP	44	30	C
	LC4064C-5T44C	64	1.8	5	TQFP	44	30	C
	LC4064C-75T44C	64	1.8	7.5	TQFP	44	30	C

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC ¹	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC ¹	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC ¹	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC ¹	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC ¹	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC ¹	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C ¹	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C ¹	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C ¹	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

Lead-Free Packaging**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices**

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 μ A to -200 μ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.