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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	30
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032v-10t44i

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

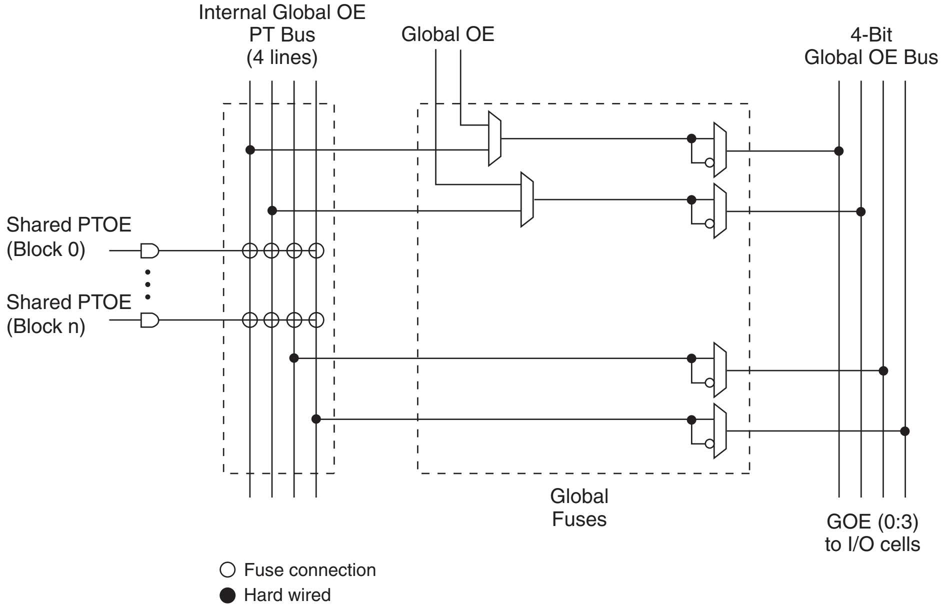
Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 device that has a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except ispMACH 4032



Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C/Z (1.8V)	**ispMACH 4000B (2.5V)**	**ispMACH 4000V (3.3V)**
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6[1, 2]	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T_j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided ($V_{IN} - V_{CCO}$) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	341	—	µA
		Vcc = 1.9V, T_A = 70°C	—	361	—	µA
		Vcc = 1.9V, T_A = 85°C	—	372	—	µA
		Vcc = 1.9V, T_A = 125°C	—	468	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	13	—	µA
		Vcc = 1.9V, T_A = 70°C	—	32	55	µA
		Vcc = 1.9V, T_A = 85°C	—	43	90	µA
		Vcc = 1.9V, T_A = 125°C	—	135	—	µA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000V/B/C External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t_R	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t_{CW}	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t_{WIR}	Input register clock width, high or low	2.2	—	2.8	—	4.0		ns
f_{MAX}[4]	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/(t_S + t_{CO})]$	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.95	—	1.50	—	2.00	ns
t_{GOE}	Global OE Pin Delay	—	4.04	—	6.04	—	7.04	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.83	—	2.28	—	3.28	ns
t_{BUF}	Delay through Output Buffer	—	1.00	—	1.50	—	1.50	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	1.51	—	2.26	—	3.26	ns
t_{MCELL}	Macrocell Delay	—	1.05	—	1.45	—	1.95	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.56	—	0.96	—	1.46	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	1.54	—	2.24	—	3.24	ns
t_{PDi}	Macrocell Propagation Delay	—	0.94	—	1.24	—	1.74	ns
Register/Latch Delays								
t_S	D-Register Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.52	—	1.77	—	1.77	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t_H	D-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t_{HT}	T-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.52	—	1.57	—	1.57	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.68	—	1.18	—	1.18	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.68	—	1.18	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.67	—	1.17	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	0.62	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.51	—	3.41	—	3.41	ns

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.95	—	1.25	—	1.80	ns
t_{GOE}	Global OE Pin Delay	—	3.00	—	3.50	—	4.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.05	—	2.15	ns
t_{BUF}	Delay through Output Buffer	—	1.10	—	1.00	—	1.30	ns
t_{EN}	Output Enable Time	—	2.50	—	2.50	—	2.70	ns
t_{DIS}	Output Disable Time	—	2.50	—	2.50	—	2.70	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	2.25	—	2.05	—	2.50	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.65	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.35	—	0.05	—	0.05	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.20	—	0.70	—	1.90	ns
t_{PDi}	Macrocell Propagation Delay	—	0.45	—	0.65	—	1.00	ns
Register/Latch Delays								
t_{S}	D-Register Setup Time (Global Clock)	1.00	—	1.10	—	1.35	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	2.10	—	1.90	—	2.45	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.20	—	1.30	—	1.55	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	2.30	—	2.10	—	2.75	—	ns
t_{H}	D-Register Hold Time	1.90	—	1.90	—	3.15	—	ns
t_{HT}	T-Resister Hold Time	1.90	—	1.90	—	3.15	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.30	—	1.10	—	0.75	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.30	—	1.50	—	1.95	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.00	—	1.00	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.75	—	1.15	—	1.05	ns
t_{CES}	Clock Enable Setup Time	2.00	—	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.00	—	1.00	—	1.65	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	2.10	—	1.90	—	2.15	—	ns
t_{HL}	Latch Hold Time	2.00	—	2.00	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.97	—	0.97	—	0.28	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.80	—	1.80	—	1.67	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.83	—	1.83	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	4.30	—	4.20	—	3.50	ns

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PTOE}	Macrocell PT OE Delay	—	2.50	—	2.70	—	2.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2

ispMACH 4000Z Timing Adders (Cont.)[1]

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.30	—	1.30	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t_{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

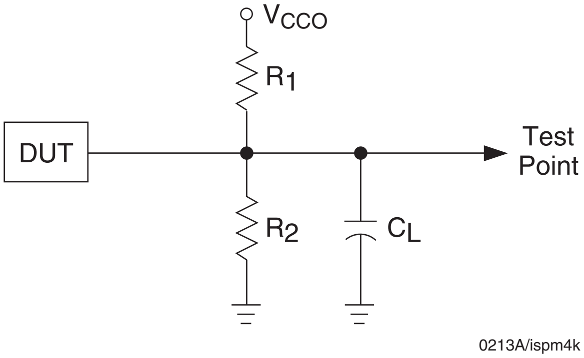


Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $V_{CCO}/2$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $V_{CCO}/2$	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

[1] C_L includes test fixtures and probe capacitance.

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3	P12	P^3
85	1	D2	D^2	H4	H^2	P10	P^2
86	1	D1	D^1	H2	H^1	P6	P^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	P^0
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^0
92	0	A1	A^1	A2	A^1	A6	A^1
93	0	A2	A^2	A4	A^2	A10	A^2
94	0	A3	A^3	A6	A^3	A12	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4	B2	B^0
98	0	A5	A^5	A10	A^5	B6	B^1
99	0	A6	A^6	A12	A^6	B10	B^2
100	0	A7	A^7	A14	A^7	B12	B^3

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
105	1	VCCO (Bank 1)	-
106	1	H6	H^5
107	1	H5	H^4
108	1	H4	H^3
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^3
120	0	A5	A^4
121	0	A6	A^5
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A^6
125	0	A9	A^7
126	0	A10	A^8
127	0	A12	A^9
128	0	A14	A^11

ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	GND	-	GND	-	GND	-
B2	-	TDI	-	TDI	-	TDI	-
C1	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
C3	0	NC	-	B0	B^0	C12	C^6
C2	0	A8	A^8	B1	B^1	C10	C^5
D1	0	A9	A^9	B2	B^2	C8	C^4
D3	0	A10	A^10	B4	B^3	C6	C^3
D2	0	A11	A^11	B5	B^4	C4	C^2
E1	0	NC		B6	B^5	C2	C^1
E2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-

ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E3	0	NC	-	B8	B^6	D12	D^6
F2	0	A12	A^12	B9	B^7	D10	D^5
F1	0	A13	A^13	B10	B^8	D8	D^4
F3	0	A14	A^14	B12	B^9	D6	D^3
G1	0	A15	A^15	B13	B^10	D4	D^2
G2	0	I	-	B14	B^11	D2	D^1
G3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
H2	0	NC	-	C14	C^11	E2	E^1
H1	0	B15	B^15	C13	C^10	E4	E^2
H3	0	B14	B^14	C12	C^9	E6	E^3
J1	0	B13	B^13	C10	C^8	E8	E^4
J2	0	B12	B^12	C9	C^7	E10	E^5
J3	0	NC	-	C8	C^6	E12	E^6
K2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
K1	0	NC	-	C6	C^5	F2	F^1
K3	0	B11	B^11	C5	C^4	F4	F^2
L2	0	B10	B^10	C4	C^3	F6	F^3
L1	0	B9	B^9	C2	C^2	F8	F^4
L3	0	B8	B^8	C1	C^1	F10	F^5
M1	0	I	-	C0	C^0	F12	F^6
M2	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N1	-	TCK	-	TCK	-	TCK	-
P1	-	VCC	-	VCC	-	VCC	-
P2	-	GND	-	GND	-	GND	-
N2	0	I	-	D14	D^11	G12	G^6
P3	0	B7	B^7	D13	D^10	G10	G^5
M3	0	B6	B^6	D12	D^9	G8	G^4
N3	0	B5	B^5	D10	D^8	G6	G^3
P4	0	B4	B^4	D9	D^7	G4	G^2
M4	0	NC	-	D8	D^6	G2	G^1
N4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
P5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N5	0	NC	-	D6	D^5	H12	H^6
M5	0	B3	B^3	D5	D^4	H10	H^5
N6	0	B2	B^2	D4	D^3	H8	H^4
P6	0	B1	B^1	D2	D^2	H6	H^3
M6	0	B0	B^0	D1	D^1	H4	H^2
P7	0	NC	-	D0	D^0	H2	H^1
N7	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
M7	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
N8	-	VCC	-	VCC	-	VCC	-

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
86	1	F12	F^9	L8	L^4
87	1	F13	F^10	L6	L^3
88	1	F14	F^11	L4	L^2
89	1	NC[2]	-	I[2]	-
90	1	GND (Bank 1)[1]	-	NC[1]	-
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
92	1	NC[2]	-	I[2]	-
93	1	G14	G^11	M2	M^1
94	1	G13	G^10	M4	M^2
95	1	G12	G^9	M6	M^3
96	1	G10	G^8	M8	M^4
97	1	G9	G^7	M10	M^5
98	1	G8	G^6	M12	M^6
99	1	GND (Bank 1)	-	GND (Bank 1)	-
100	1	G6	G^5	N2	N^1
101	1	G5	G^4	N4	N^2
102	1	G4	G^3	N6	N^3
103	1	G2	G^2	N8	N^4
104	1	G1	G^1	N10	N^5
105	1	G0	G^0	N12	N^6
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
107	-	TDO	-	TDO	-
108	-	VCC	-	VCC	-
109	-	GND	-	GND	-
110	1	NC[2]	-	I[2]	-
111	1	H14	H^11	O12	O^6
112	1	H13	H^10	O10	O^5
113	1	H12	H^9	O8	O^4
114	1	H10	H^8	O6	O^3
115	1	H9	H^7	O4	O^2
116	1	H8	H^6	O2	O^1
117	1	NC[2]	-	I[2]	-
118	1	GND (Bank 1)	-	GND (Bank 1)	-
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
120	1	H6	H^5	P12	P^6
121	1	H5	H^4	P10	P^5
122	1	H4	H^3	P8	P^4
123	1	H2	H^2	P6	P^3
124	1	H1	H^1	P4	P^2
125	1	H0/GOE1	H^0	P2/GOE1	P^1
126	1	CLK3/I	-	CLK3/I	-
127	0	GND (Bank 0)	-	GND (Bank 0)	-
128	0	CLK0/I	-	CLK0/I	-

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E^7	E10	E^7	H14	H^7	J14	J^7
K3	0	NC	-	E12	E^8	G0	G^0	I0	I^0
K4	0	NC	-	E14	E^9	G2	G^1	I4	I^1
L1	0	NC	-	NC	-	I14	I^7	K0	K^0
L2	0	NC	-	NC	-	I12	I^6	K2	K^1
M1	0	NC	-	NC	-	NC	-	K4	K^2
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K^3
N1	0	NC	-	NC	-	I10	I^5	K8	K^4
M3	0	NC	-	NC	-	I8	I^4	K10	K^5
M4	0	NC	-	F0	F^0	G4	G^2	I8	I^2
N2	0	NC	-	F1	F^1	G6	G^3	I12	I^3
K5	0	F0	F^0	F2	F^2	J0	J^0	N0	N^0
P1	0	F2	F^1	F4	F^3	J2	J^1	N2	N^1
K6	0	F4	F^2	F6	F^4	J4	J^2	N4	N^2
N3	0	F6	F^3	F8	F^5	J6	J^3	N6	N^3
L5	0	F8	F^4	F9	F^6	J8	J^4	N8	N^4
P2	0	F10	F^5	F10	F^7	J10	J^5	N10	N^5
L6	0	F12	F^6	F12	F^8	J12	J^6	N12	N^6
R1	0	F14	F^7	F14	F^9	J14	J^7	N14	N^7
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G^9	I6	I^3	K12	K^6
M5	0	NC	-	G12	G^8	I4	I^2	K14	K^7
N4	0	G14	G^7	G10	G^7	K14	K^7	O14	O^7
T3	0	G12	G^6	G9	G^6	K12	K^6	O12	O^6
R3	0	G10	G^5	G8	G^5	K10	K^5	O10	O^5
M6	0	G8	G^4	G6	G^4	K8	K^4	O8	O^4
P4	0	G6	G^3	G4	G^3	K6	K^3	O6	O^3
L7	0	G4	G^2	G2	G^2	K4	K^2	O4	O^2
N5	0	G2	G^1	G1	G^1	K2	K^1	O2	O^1
M7	0	G0	G^0	G0	G^0	K0	K^0	O0	O^0
P5	0	NC	-	NC	-	G8	G^4	M0	M^0
R4	0	NC	-	NC	-	G10	G^5	M4	M^1
T4	0	NC	-	NC	-	NC	-	L0	L^0
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J^5	J10	J^7	N10	N^5	BX10	BX^5
P13	1	J12	J^6	J12	J^8	N12	N^6	BX12	BX^6
N13	1	J14	J^7	J14	J^9	N14	N^7	BX14	BX^7
M12	1	NC	-	NC	-	P4	P^2	FX0	FX^0
T15	1	NC	-	NC	-	P6	P^3	FX2	FX^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX^2
R16	1	NC	-	NC	-	P8	P^4	FX6	FX^3
N14	1	NC	-	NC	-	P10	P^5	FX8	FX^4
P15	1	K14	K^7	K14	K^9	O14	O^7	CX14	CX^7
L11	1	K12	K^6	K12	K^8	O12	O^6	CX12	CX^6
P16	1	K10	K^5	K10	K^7	O10	O^5	CX10	CX^5
K11	1	K8	K^4	K9	K^6	O8	O^4	CX8	CX^4
M14	1	K6	K^3	K8	K^5	O6	O^3	CX6	CX^3
K12	1	K4	K^2	K6	K^4	O4	O^2	CX4	CX^2
N15	1	K2	K^1	K4	K^3	O2	O^1	CX2	CX^1
N16	1	K0	K^0	K2	K^2	O0	O^0	CX0	CX^0
M15	1	NC	-	K1	K^1	BX6	BX^3	HX0	HX^0
M13	1	NC	-	K0	K^0	BX4	BX^2	HX4	HX^1
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX^5
L15	1	NC	-	NC	-	P12	P^6	FX12	FX^6
L16	1	NC	-	NC	-	P14	P^7	FX14	FX^7
J11	1	NC	-	L14	L^9	BX2	BX^1	HX8	HX^2
K15	1	NC	-	L12	L^8	BX0	BX^0	HX12	HX^3
J12	1	L14	L^7	L10	L^7	AX14	AX^7	GX14	GX^7
K13	1	L12	L^6	L9	L^6	AX12	AX^6	GX12	GX^6
K14	1	L10	L^5	L8	L^5	AX10	AX^5	GX10	GX^5
K16	1	L8	L^4	L6	L^4	AX8	AX^4	GX8	GX^4
J16	1	L6	L^3	L4	L^3	AX6	AX^3	GX6	GX^3
J15	1	L4	L^2	L2	L^2	AX4	AX^2	GX4	GX^2
H16	1	L2	L^1	L1	L^1	AX2	AX^1	GX2	GX^1
J13	1	L0	L^0	L0	L^0	AX0	AX^0	GX0	GX^0
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M^0	M0	M^0	DX0	DX^0	JX0	JX^0

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	tPD	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5M132I	64	1.8	5	csBGA	132	64	I
	LC4064ZC-75M132I	64	1.8	7.5	csBGA	132	64	I
	LC4064ZC-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064ZC-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064ZC-5M56I	64	1.8	5	csBGA	56	34	I
	LC4064ZC-75M56I	64	1.8	7.5	csBGA	56	34	I
	LC4064ZC-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064ZC-75T48I	64	1.8	7.5	TQFP	48	32	I
LC4128ZC	LC4128ZC-75M132I	128	1.8	7.5	csBGA	132	96	I
	LC4128ZC-75T100I	128	1.8	7.5	TQFP	100	64	I
LC4256ZC	LC4256ZC-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256ZC-75M132I	256	1.8	7.5	csBGA	132	96	I
	LC4256ZC-75T100I	256	1.8	7.5	TQFP	100	64	I

ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75T48E	32	1.8	7.5	TQFP	48	32	E
LC4064ZC	LC4064ZC-75T100E	64	1.8	7.5	TQFP	100	64	E
	LC4064ZC-75T48E	64	1.8	7.5	TQFP	48	32	E
LC4128ZC	LC4128ZC-75T100E	128	1.8	7.5	TQFP	100	64	E
LC4256ZC	LC4256ZC-75T176E	256	1.8	7.5	TQFP	176	128	E
	LC4256ZC-75T100E	256	1.8	7.5	TQFP	100	64	E

ispMACH 4000C (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25T48C	32	1.8	2.5	TQFP	48	32	C
	LC4032C-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032C-75T48C	32	1.8	7.5	TQFP	48	32	C
	LC4032C-25T44C	32	1.8	2.5	TQFP	44	30	C
	LC4032C-5T44C	32	1.8	5	TQFP	44	30	C
	LC4032C-75T44C	32	1.8	7.5	TQFP	44	30	C
LC4064C	LC4064C-25T100C	64	1.8	2.5	TQFP	100	64	C
	LC4064C-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064C-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064C-25T48C	64	1.8	2.5	TQFP	48	32	C
	LC4064C-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064C-75T48C	64	1.8	7.5	TQFP	48	32	C
	LC4064C-25T44C	64	1.8	2.5	TQFP	44	30	C
	LC4064C-5T44C	64	1.8	5	TQFP	44	30	C
	LC4064C-75T44C	64	1.8	7.5	TQFP	44	30	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI[1]	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI[1]	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI[1]	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI[1]	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI[1]	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI[1]	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I[1]	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I[1]	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I[1]	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I[1]	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I[1]	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I[1]	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points (0 ≤ VIN ≤ 3.6V).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided (VIN - VCCO) ≤ 3.6V.
		Improved LC4064ZC t_S to 2.5ns, t_{ST} to 2.7ns and f_{MAX} (Ext.) to 175MHz, LC4128ZC t_{CO} to 3.5ns and f_{MAX} (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs