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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	30
Operating Temperature	-40°C ~ 105°C (Tj)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032v-10tn44i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032v-10tn44i</a>

## I/O Recommended Operating Conditions

Standard	$V_{CCO}$ (V) <sup>1</sup>	
	Min.	Max.
LVTTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3 <sup>2</sup>	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for  $V_{CCO}$  are the average of the min. and max. values.

2. ispMACH 4000Z only.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input Leakage Current (ispMACH 4000Z)	$0 \leq V_{IN} < V_{CCO}$	—	0.5	1	$\mu A$
$I_{IH}^1$	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \leq 5.5V$	—	—	10	$\mu A$
$I_{IL}, I_{IH}^1$	Input Leakage Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$	—	—	10	$\mu A$
		$0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$	—	—	15	$\mu A$
$I_{IH}^{1,2}$	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	20	$\mu A$
		$3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V$	—	—	50	$\mu A$
$I_{PU}$	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-150	$\mu A$
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-200	$\mu A$
$I_{PD}$	I/O Weak Pull-down Resistor Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$	30	—	150	$\mu A$
$I_{BHLS}$	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	$\mu A$
$I_{BHHS}$	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	$\mu A$
$I_{BHLO}$	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{BHT}$	—	—	150	$\mu A$
$I_{BHHO}$	Bus Hold High Overdrive Current	$V_{BHT} \leq V_{IN} \leq V_{CCO}$	—	—	-150	$\mu A$
$V_{BHT}$	Bus Hold Trip Points	—	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
$C_1$	I/O Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_2$	Clock Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_3$	Global Input Capacitance <sup>3</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where  $3.0V \leq V_{CCO} \leq 3.6V$ .

3.  $T_A = 25^\circ C, f = 1.0MHz$

4.  $I_{IH}$  excursions of up to 1.5 $\mu A$  maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

### Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I <sub>CC</sub> <sup>4</sup>	Standby Power Supply Current	V <sub>CC</sub> = 3.3V	—	13	—	mA
		V <sub>CC</sub> = 2.5V	—	13	—	mA
		V <sub>CC</sub> = 1.8V	—	3	—	mA

1. T<sub>A</sub> = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I<sub>CC</sub> varies with specific device configuration and operating frequency.
4. T<sub>A</sub> = 25°C

### Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4032ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	50	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	58	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	60	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	70	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	10	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	13	20	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	15	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	22	—	μA
<b>ispMACH 4064ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	80	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	89	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	92	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	109	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	11	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	15	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	18	35	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	37	—	μA
<b>ispMACH 4128ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	168	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	190	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	195	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	212	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	12	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	16	35	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	19	50	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	42	—	μA

**Supply Current, ispMACH 4000Z (Cont.)**

**Over Recommended Operating Conditions**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4256ZC</b>						
ICC <sup>1,2,3,5</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	341	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	361	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	372	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	468	—	μA
ICC <sup>4,5</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	13	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 70°C	—	32	55	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 85°C	—	43	90	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 125°C	—	135	—	μA

1. T<sub>A</sub> = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I<sub>CC</sub> varies with specific device configuration and operating frequency.
4. V<sub>CCO</sub> = 3.6V, V<sub>IN</sub> = 0V or V<sub>CCO</sub>, bus maintenance turned off. V<sub>IN</sub> above V<sub>CCO</sub> will add transient current above the specified standby I<sub>CC</sub>.
5. Includes V<sub>CCO</sub> current without output loading.

## ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-25		-27		-3		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	3.5	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	4.2	ns
t <sub>S</sub>	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	2.7	ns
t <sub>R</sub>	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	4.5	ns
t <sub>RW</sub>	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	-	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	5.5	ns
t <sub>G<sub>P<sub>TOE/DIS</sub></sub></sub>	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	8.0	ns
t <sub>G<sub>OE/DIS</sub></sub>	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	4.5	ns
t <sub>CW</sub>	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	400	—	333	—	322	—	322	MHz
f <sub>MAX</sub> (Ext.)	Clock frequency with external feedback, [1/ (t <sub>S</sub> + t <sub>CO</sub> )]	—	250	—	222	—	212	—	212	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.3.2

2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

## ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t <sub>S</sub>	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t <sub>R</sub>	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t <sub>RW</sub>	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
t <sub>G<sub>P</sub>TOE/DIS</sub>	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
t <sub>G<sub>O</sub>E/DIS</sub>	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t <sub>CW</sub>	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f <sub>MAX</sub> (Ext.)	clock frequency with external feedback, [1 / (t <sub>S</sub> + t <sub>CO</sub> )]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

**ispMACH 4000Z Timing Adders <sup>1</sup>**

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.00	—	1.00	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing. Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

ispMACH 4000Z Timing Adders (Cont.)<sup>1</sup>

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.30	—	1.30	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.



**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:  
44-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
K5	0	A15	A <sup>15</sup>	B0	B <sup>0</sup>
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B <sup>0</sup>	C0	C <sup>0</sup>
K7	1	B1	B <sup>1</sup>	C1	C <sup>1</sup>
K8	1	B2	B <sup>2</sup>	C2	C <sup>2</sup>
K9	1	B3	B <sup>3</sup>	C4	C <sup>3</sup>
K10	1	B4	B <sup>4</sup>	C6	C <sup>4</sup>
J10	-	TMS	-	TMS	-
H8	1	B5	B <sup>5</sup>	C8	C <sup>5</sup>
H10	1	B6	B <sup>6</sup>	C10	C <sup>6</sup>
G10	1	B7	B <sup>7</sup>	C11	C <sup>7</sup>
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
F10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B <sup>8</sup>	D15	D <sup>7</sup>
D8	1	B9	B <sup>9</sup>	D12	D <sup>6</sup>
D10	1	B10	B <sup>10</sup>	D10	D <sup>5</sup>
C10	1	B11	B <sup>11</sup>	D8	D <sup>4</sup>
B10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A7	1	B12	B <sup>12</sup>	D6	D <sup>3</sup>
C7	1	B13	B <sup>13</sup>	D4	D <sup>2</sup>
C6	1	B14	B <sup>14</sup>	D2	D <sup>1</sup>
A6	1	B15/GOE1	B <sup>15</sup>	D0/GOE1	D <sup>0</sup>
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>
A4	0	A1	A <sup>1</sup>	A1	A <sup>1</sup>
A3	0	A2	A <sup>2</sup>	A2	A <sup>2</sup>
A2	0	A3	A <sup>3</sup>	A4	A <sup>3</sup>
A1	0	A4	A <sup>4</sup>	A6	A <sup>4</sup>

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C^1	E2	E^1	I6	I^1
43	1	C2	C^2	E4	E^2	I10	I^2
44	1	C3	C^3	E6	E^3	I12	I^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4	J2	J^0
48	1	C5	C^5	E10	E^5	J6	J^1
49	1	C6	C^6	E12	E^6	J10	J^2
50	1	C7	C^7	E14	E^7	J12	J^3
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0	K12	K^3
54	1	C9	C^9	F2	F^1	K10	K^2
55	1	C10	C^10	F4	F^2	K6	K^1
56	1	C11	C^11	F6	F^3	K2	K^0
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4	L12	L^3
59	1	C13	C^13	F10	F^5	L10	L^2
60	1	C14	C^14	F12	F^6	L6	L^1
61	1	C15	C^15	F13	F^7	L4	L^0
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7	M4	M^0
65	1	D14	D^14	G12	G^6	M6	M^1
66	1	D13	D^13	G10	G^5	M10	M^2
67	1	D12	D^12	G8	G^4	M12	M^3
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3	N2	N^0
70	1	D10	D^10	G5	G^2	N6	N^1
71	1	D9	D^9	G4	G^1	N10	N^2
72	1	D8	D^8	G2	G^0	N12	N^3
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D^7	H13	H^7	O12	O^3
79	1	D6	D^6	H12	H^6	O10	O^2
80	1	D5	D^5	H10	H^5	O6	O^1
81	1	D4	D^4	H8	H^4	O2	O^0
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D <sup>3</sup>	H6	H <sup>3</sup>	P12	P <sup>3</sup>
85	1	D2	D <sup>2</sup>	H4	H <sup>2</sup>	P10	P <sup>2</sup>
86	1	D1	D <sup>1</sup>	H2	H <sup>1</sup>	P6	P <sup>1</sup>
87	1	D0/GOE1	D <sup>0</sup>	H0/GOE1	H <sup>0</sup>	P2/OE1	P <sup>0</sup>
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>	A2/GOE0	A <sup>0</sup>
92	0	A1	A <sup>1</sup>	A2	A <sup>1</sup>	A6	A <sup>1</sup>
93	0	A2	A <sup>2</sup>	A4	A <sup>2</sup>	A10	A <sup>2</sup>
94	0	A3	A <sup>3</sup>	A6	A <sup>3</sup>	A12	A <sup>3</sup>
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A <sup>4</sup>	A8	A <sup>4</sup>	B2	B <sup>0</sup>
98	0	A5	A <sup>5</sup>	A10	A <sup>5</sup>	B6	B <sup>1</sup>
99	0	A6	A <sup>6</sup>	A12	A <sup>6</sup>	B10	B <sup>2</sup>
100	0	A7	A <sup>7</sup>	A14	A <sup>7</sup>	B12	B <sup>3</sup>

\*This pin is input only.

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B <sup>0</sup>
5	0	B1	B <sup>1</sup>
6	0	B2	B <sup>2</sup>
7	0	B4	B <sup>3</sup>
8	0	B5	B <sup>4</sup>
9	0	B6	B <sup>5</sup>
10	0	GND (Bank 0)	-
11	0	B8	B <sup>6</sup>
12	0	B9	B <sup>7</sup>
13	0	B10	B <sup>8</sup>
14	0	B12	B <sup>9</sup>
15	0	B13	B <sup>10</sup>
16	0	B14	B <sup>11</sup>
17	0	VCCO (Bank 0)	-
18	0	C14	C <sup>11</sup>

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D <sup>2</sup>	E4	E <sup>2</sup>	G4	G <sup>2</sup>
20	0	D2	D <sup>1</sup>	E2	E <sup>1</sup>	G2	G <sup>1</sup>
21	0	D0	D <sup>0</sup>	E0	E <sup>0</sup>	G0	G <sup>0</sup>
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E <sup>0</sup>	H0	H <sup>0</sup>	J0	J <sup>0</sup>
24	0	E2	E <sup>1</sup>	H2	H <sup>1</sup>	J2	J <sup>1</sup>
25	0	E4	E <sup>2</sup>	H4	H <sup>2</sup>	J4	J <sup>2</sup>
26	0	E6	E <sup>3</sup>	H6	H <sup>3</sup>	J6	J <sup>3</sup>
27	0	E8	E <sup>4</sup>	H8	H <sup>4</sup>	J8	J <sup>4</sup>
28	0	E10	E <sup>5</sup>	H10	H <sup>5</sup>	J10	J <sup>5</sup>
29	0	E12	E <sup>6</sup>	H12	H <sup>6</sup>	J12	J <sup>6</sup>
30	0	E14	E <sup>7</sup>	H14	H <sup>7</sup>	J14	J <sup>7</sup>
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F <sup>0</sup>	J0	J <sup>0</sup>	N0	N <sup>0</sup>
33	0	F2	F <sup>1</sup>	J2	J <sup>1</sup>	N2	N <sup>1</sup>
34	0	F4	F <sup>2</sup>	J4	J <sup>2</sup>	N4	N <sup>2</sup>
35	0	F6	F <sup>3</sup>	J6	J <sup>3</sup>	N6	N <sup>3</sup>
36	0	F8	F <sup>4</sup>	J8	J <sup>4</sup>	N8	N <sup>4</sup>
37	0	F10	F <sup>5</sup>	J10	J <sup>5</sup>	N10	N <sup>5</sup>
38	0	F12	F <sup>6</sup>	J12	J <sup>6</sup>	N12	N <sup>6</sup>
39	0	F14	F <sup>7</sup>	J14	J <sup>7</sup>	N14	N <sup>7</sup>
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G <sup>7</sup>	K14	K <sup>7</sup>	O14	O <sup>7</sup>
48	0	G12	G <sup>6</sup>	K12	K <sup>6</sup>	O12	O <sup>6</sup>
49	0	G10	G <sup>5</sup>	K10	K <sup>5</sup>	O10	O <sup>5</sup>
50	0	G8	G <sup>4</sup>	K8	K <sup>4</sup>	O8	O <sup>4</sup>
51	0	G6	G <sup>3</sup>	K6	K <sup>3</sup>	O6	O <sup>3</sup>
52	0	G4	G <sup>2</sup>	K4	K <sup>2</sup>	O4	O <sup>2</sup>
53	0	G2	G <sup>1</sup>	K2	K <sup>1</sup>	O2	O <sup>1</sup>
54	0	G0	G <sup>0</sup>	K0	K <sup>0</sup>	O0	O <sup>0</sup>
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H <sup>7</sup>	L14	L <sup>7</sup>	P14	P <sup>7</sup>
58	0	H12	H <sup>6</sup>	L12	L <sup>6</sup>	P12	P <sup>6</sup>
59	0	H10	H <sup>5</sup>	L10	L <sup>5</sup>	P10	P <sup>5</sup>

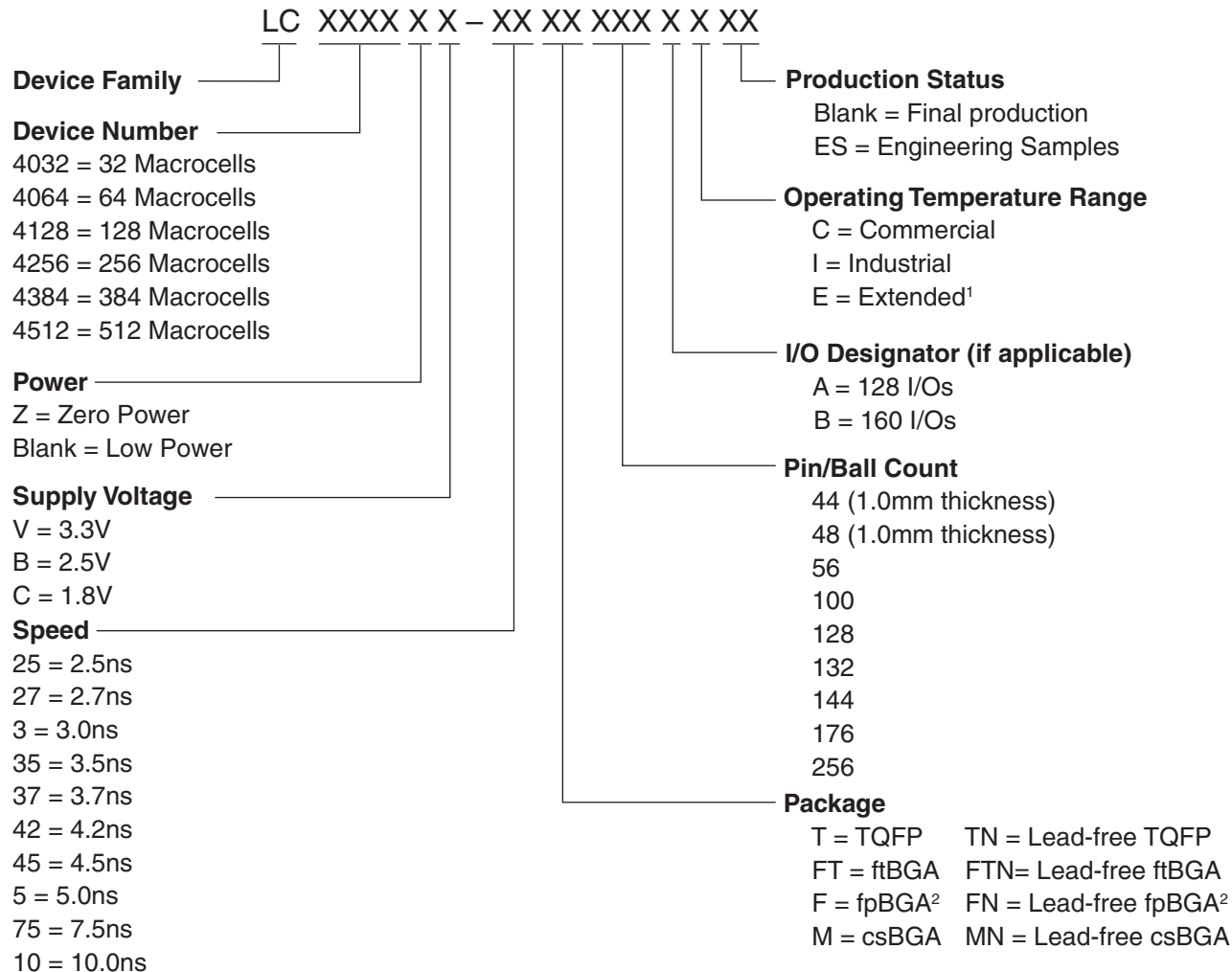
**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
142	1	O0	O <sup>0</sup>	GX0	GX <sup>0</sup>	OX0	OX <sup>0</sup>
143	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
145	1	P14	P <sup>7</sup>	HX14	HX <sup>7</sup>	PX14	PX <sup>7</sup>
146	1	P12	P <sup>6</sup>	HX12	HX <sup>6</sup>	PX12	PX <sup>6</sup>
147	1	P10	P <sup>5</sup>	HX10	HX <sup>5</sup>	PX10	PX <sup>5</sup>
148	1	P8	P <sup>4</sup>	HX8	HX <sup>4</sup>	PX8	PX <sup>4</sup>
149	1	P6	P <sup>3</sup>	HX6	HX <sup>3</sup>	PX6	PX <sup>3</sup>
150	1	P4	P <sup>2</sup>	HX4	HX <sup>2</sup>	PX4	PX <sup>2</sup>
151	1	P2/GOE1	P <sup>1</sup>	HX2/GOE1	HX <sup>1</sup>	PX2/GOE1	PX <sup>1</sup>
152	1	P0	P <sup>0</sup>	HX0	HX <sup>0</sup>	PX0	PX <sup>0</sup>
153	-	GND	-	GND	-	GND	-
154	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
155	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
156	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
157	-	VCC	-	VCC	-	VCC	-
158	0	A0	A <sup>0</sup>	A0	A <sup>0</sup>	A0	A <sup>0</sup>
159	0	A2/GOE0	A <sup>1</sup>	A2/GOE0	A <sup>1</sup>	A2/GOE0	A <sup>1</sup>
160	0	A4	A <sup>2</sup>	A4	A <sup>2</sup>	A4	A <sup>2</sup>
161	0	A6	A <sup>3</sup>	A6	A <sup>3</sup>	A6	A <sup>3</sup>
162	0	A8	A <sup>4</sup>	A8	A <sup>4</sup>	A8	A <sup>4</sup>
163	0	A10	A <sup>5</sup>	A10	A <sup>5</sup>	A10	A <sup>5</sup>
164	0	A12	A <sup>6</sup>	A12	A <sup>6</sup>	A12	A <sup>6</sup>
165	0	A14	A <sup>7</sup>	A14	A <sup>7</sup>	A14	A <sup>7</sup>
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
167	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
168	0	B0	B <sup>0</sup>	B0	B <sup>0</sup>	B0	B <sup>0</sup>
169	0	B2	B <sup>1</sup>	B2	B <sup>1</sup>	B2	B <sup>1</sup>
170	0	B4	B <sup>2</sup>	B4	B <sup>2</sup>	B4	B <sup>2</sup>
171	0	B6	B <sup>3</sup>	B6	B <sup>3</sup>	B6	B <sup>3</sup>
172	0	B8	B <sup>4</sup>	B8	B <sup>4</sup>	B8	B <sup>4</sup>
173	0	B10	B <sup>5</sup>	B10	B <sup>5</sup>	B10	B <sup>5</sup>
174	0	B12	B <sup>6</sup>	B12	B <sup>6</sup>	B12	B <sup>6</sup>
175	0	B14	B <sup>7</sup>	B14	B <sup>7</sup>	B14	B <sup>7</sup>
176	-	VCC	-	VCC	-	VCC	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E^7	E10	E^7	H14	H^7	J14	J^7
K3	0	NC	-	E12	E^8	G0	G^0	I0	I^0
K4	0	NC	-	E14	E^9	G2	G^1	I4	I^1
L1	0	NC	-	NC	-	I14	I^7	K0	K^0
L2	0	NC	-	NC	-	I12	I^6	K2	K^1
M1	0	NC	-	NC	-	NC	-	K4	K^2
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K^3
N1	0	NC	-	NC	-	I10	I^5	K8	K^4
M3	0	NC	-	NC	-	I8	I^4	K10	K^5
M4	0	NC	-	F0	F^0	G4	G^2	I8	I^2
N2	0	NC	-	F1	F^1	G6	G^3	I12	I^3
K5	0	F0	F^0	F2	F^2	J0	J^0	N0	N^0
P1	0	F2	F^1	F4	F^3	J2	J^1	N2	N^1
K6	0	F4	F^2	F6	F^4	J4	J^2	N4	N^2
N3	0	F6	F^3	F8	F^5	J6	J^3	N6	N^3
L5	0	F8	F^4	F9	F^6	J8	J^4	N8	N^4
P2	0	F10	F^5	F10	F^7	J10	J^5	N10	N^5
L6	0	F12	F^6	F12	F^8	J12	J^6	N12	N^6
R1	0	F14	F^7	F14	F^9	J14	J^7	N14	N^7
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G^9	I6	I^3	K12	K^6
M5	0	NC	-	G12	G^8	I4	I^2	K14	K^7
N4	0	G14	G^7	G10	G^7	K14	K^7	O14	O^7
T3	0	G12	G^6	G9	G^6	K12	K^6	O12	O^6
R3	0	G10	G^5	G8	G^5	K10	K^5	O10	O^5
M6	0	G8	G^4	G6	G^4	K8	K^4	O8	O^4
P4	0	G6	G^3	G4	G^3	K6	K^3	O6	O^3
L7	0	G4	G^2	G2	G^2	K4	K^2	O4	O^2
N5	0	G2	G^1	G1	G^1	K2	K^1	O2	O^1
M7	0	G0	G^0	G0	G^0	K0	K^0	O0	O^0
P5	0	NC	-	NC	-	G8	G^4	M0	M^0
R4	0	NC	-	NC	-	G10	G^5	M4	M^1
T4	0	NC	-	NC	-	NC	-	L0	L^0
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

### Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).  
 2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

### ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.



## ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC <sup>1</sup>	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC <sup>1</sup>	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC <sup>1</sup>	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC <sup>1</sup>	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC <sup>1</sup>	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC <sup>1</sup>	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
LC4256B-5T100C	256	2.5	5	TQFP	100	64	C	
LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C	
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C <sup>1</sup>	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C <sup>1</sup>	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C <sup>1</sup>	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C <sup>1</sup>	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C <sup>1</sup>	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C <sup>1</sup>	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75T48E	32	3.3	7.5	TQFP	48	32	E
	LC4032V-75T44E	32	3.3	7.5	TQFP	44	30	E
LC4064V	LC4064V-75T100E	64	3.3	7.5	TQFP	100	64	E
	LC4064V-75T48E	64	3.3	7.5	TQFP	48	32	E
	LC4064V-75T44E	64	3.3	7.5	TQFP	44	30	E
LC4128V	LC4128V-75T144E	128	3.3	7.5	TQFP	144	96	E
	LC4128V-75T128E	128	3.3	7.5	TQFP	128	92	E
	LC4128V-75T100E	128	3.3	7.5	TQFP	100	64	E
LC4256V	LC4256V-75T176E	256	3.3	7.5	TQFP	176	128	E
	LC4256V-75T144E	256	3.3	7.5	TQFP	144	96	E
	LC4256V-75T100E	256	3.3	7.5	TQFP	100	64	E

## ispMACH 4000B (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25TN48C	32	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4032B-5TN48C	32	2.5	5	Lead-Free TQFP	48	32	C
	LC4032B-75TN48C	32	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4032B-25TN44C	32	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4032B-5TN44C	32	2.5	5	Lead-Free TQFP	44	30	C
	LC4032B-75TN44C	32	2.5	7.5	Lead-Free TQFP	44	30	C
LC4064B	LC4064B-25TN100C	64	2.5	2.5	Lead-Free TQFP	100	64	C
	LC4064B-5TN100C	64	2.5	5	Lead-Free TQFP	100	64	C
	LC4064B-75TN100C	64	2.5	7.5	Lead-Free TQFP	100	64	C
	LC4064B-25TN48C	64	2.5	2.5	Lead-Free TQFP	48	32	C
	LC4064B-5TN48C	64	2.5	5	Lead-Free TQFP	48	32	C
	LC4064B-75TN48C	64	2.5	7.5	Lead-Free TQFP	48	32	C
	LC4064B-25TN44C	64	2.5	2.5	Lead-Free TQFP	44	30	C
	LC4064B-5TN44C	64	2.5	5	Lead-Free TQFP	44	30	C
LC4128B	LC4128B-27TN128C	128	2.5	2.7	Lead-Free TQFP	128	92	C
	LC4128B-5TN128C	128	2.5	5	Lead-Free TQFP	128	92	C
	LC4128B-75TN128C	128	2.5	7.5	Lead-Free TQFP	128	92	C
	LC4128B-27TN100C	128	2.5	2.7	Lead-Free TQFP	100	92	C
	LC4128B-5TN100C	128	2.5	5	Lead-Free TQFP	100	92	C
	LC4128B-75TN100C	128	2.5	7.5	Lead-Free TQFP	100	92	C
LC4256B	LC4256B-3FTN256AC	256	2.5	3	Lead-Free ftBGA	256	128	C
	LC4256B-5FTN256AC	256	2.5	5	Lead-Free ftBGA	256	128	C
	LC4256B-75FTN256AC	256	2.5	7.5	Lead-Free ftBGA	256	128	C
	LC4256B-3FTN256BC	256	2.5	3	Lead-Free ftBGA	256	160	C
	LC4256B-5FTN256BC	256	2.5	5	Lead-Free ftBGA	256	160	C
	LC4256B-75FTN256BC	256	2.5	7.5	Lead-Free ftBGA	256	160	C
	LC4256B-3FN256AC <sup>1</sup>	256	2.5	3	Lead-Free fpBGA	256	128	C
	LC4256B-5FN256AC <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	128	C
	LC4256B-75FN256AC <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	128	C
	LC4256B-3FN256BC <sup>1</sup>	256	2.5	3	Lead-Free fpBGA	256	160	C
	LC4256B-5FN256BC <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	160	C
	LC4256B-75FN256BC <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	160	C
	LC4256B-3TN176C	256	2.5	3	Lead-Free TQFP	176	128	C
	LC4256B-5TN176C	256	2.5	5	Lead-Free TQFP	176	128	C
	LC4256B-75TN176C	256	2.5	7.5	Lead-Free TQFP	176	128	C
	LC4256B-3TN100C	256	2.5	3	Lead-Free TQFP	100	64	C
	LC4256B-5TN100C	256	2.5	5	Lead-Free TQFP	100	64	C
LC4256B-75TN100C	256	2.5	7.5	Lead-Free TQFP	100	64	C	

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FTN256AI	256	3.3	5	Lead-free ftBGA	256	128	I
	LC4256V-75FTN256AI	256	3.3	7.5	Lead-free ftBGA	256	128	I
	LC4256V-10FTN256AI	256	3.3	10	Lead-free ftBGA	256	128	I
	LC4256V-5FTN256BI	256	3.3	5	Lead-free ftBGA	256	160	I
	LC4256V-75FTN256BI	256	3.3	7.5	Lead-free ftBGA	256	160	I
	LC4256V-10FTN256BI	256	3.3	10	Lead-free ftBGA	256	160	I
	LC4256V-5FN256AI <sup>1</sup>	256	3.3	5	Lead-free fpBGA	256	128	I
	LC4256V-75FN256AI <sup>1</sup>	256	3.3	7.5	Lead-free fpBGA	256	128	I
	LC4256V-10FN256AI <sup>1</sup>	256	3.3	10	Lead-free fpBGA	256	128	I
	LC4256V-5FN256BI <sup>1</sup>	256	3.3	5	Lead-free fpBGA	256	160	I
	LC4256V-75FN256BI <sup>1</sup>	256	3.3	7.5	Lead-free fpBGA	256	160	I
	LC4256V-10FN256BI <sup>1</sup>	256	3.3	10	Lead-free fpBGA	256	160	I
	LC4256V-5TN176I	256	3.3	5	Lead-free TQFP	176	128	I
	LC4256V-75TN176I	256	3.3	7.5	Lead-free TQFP	176	128	I
	LC4256V-10TN176I	256	3.3	10	Lead-free TQFP	176	128	I
	LC4256V-5TN144I	256	3.3	5	Lead-free TQFP	144	96	I
	LC4256V-75TN144I	256	3.3	7.5	Lead-free TQFP	144	96	I
	LC4256V-10TN144I	256	3.3	10	Lead-free TQFP	144	96	I
	LC4256V-5TN100I	256	3.3	5	Lead-free TQFP	100	64	I
	LC4256V-75TN100I	256	3.3	7.5	Lead-free TQFP	100	64	I
LC4256V-10TN100I	256	3.3	10	Lead-free TQFP	100	64	I	
LC4384V	LC4384V-5FTN256I	384	3.3	5	Lead-free ftBGA	256	192	I
	LC4384V-75FTN256I	384	3.3	7.5	Lead-free ftBGA	256	192	I
	LC4384V-10FTN256I	384	3.3	10	Lead-free ftBGA	256	192	I
	LC4384V-5FN256I <sup>1</sup>	384	3.3	5	Lead-free fpBGA	256	192	I
	LC4384V-75FN256I <sup>1</sup>	384	3.3	7.5	Lead-free fpBGA	256	192	I
	LC4384V-10FN256I <sup>1</sup>	384	3.3	10	Lead-free fpBGA	256	192	I
	LC4384V-5TN176I	384	3.3	5	Lead-free TQFP	176	128	I
	LC4384V-75TN176I	384	3.3	7.5	Lead-free TQFP	176	128	I
LC4384V-10TN176I	384	3.3	10	Lead-free TQFP	176	128	I	
LC4512V	LC4512V-5FTN256I	512	3.3	5	Lead-free ftBGA	256	208	I
	LC4512V-75FTN256I	512	3.3	7.5	Lead-free ftBGA	256	208	I
	LC4512V-10FTN256I	512	3.3	10	Lead-free ftBGA	256	208	I
	LC4512V-5FN256I <sup>1</sup>	512	3.3	5	Lead-free fpBGA	256	208	I
	LC4512V-75FN256I <sup>1</sup>	512	3.3	7.5	Lead-free fpBGA	256	208	I
	LC4512V-10FN256I <sup>1</sup>	512	3.3	10	Lead-free fpBGA	256	208	I
	LC4512V-5TN176I	512	3.3	5	Lead-free TQFP	176	128	I
	LC4512V-75TN176I	512	3.3	7.5	Lead-free TQFP	176	128	I
	LC4512V-10TN176I	512	3.3	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.