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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

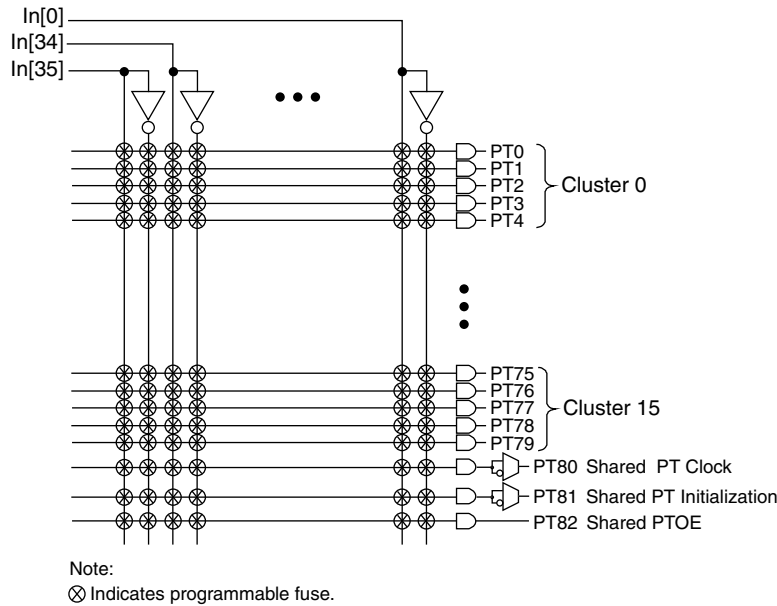
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032v-5tn48c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032v-5tn48c</a>

Figure 3. AND Array



### Enhanced Logic Allocator

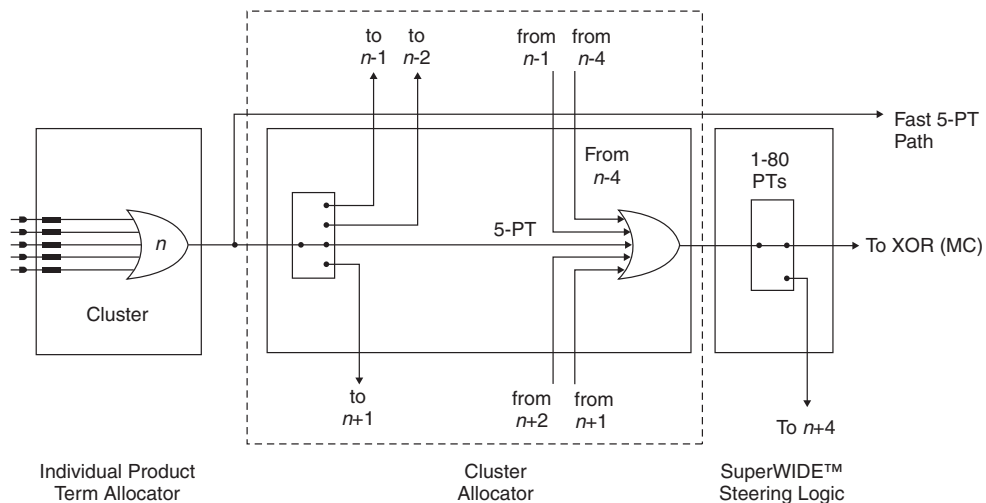
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



- LVTTTL
- LVC MOS 3.3
- LVC MOS 2.5
- LVC MOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

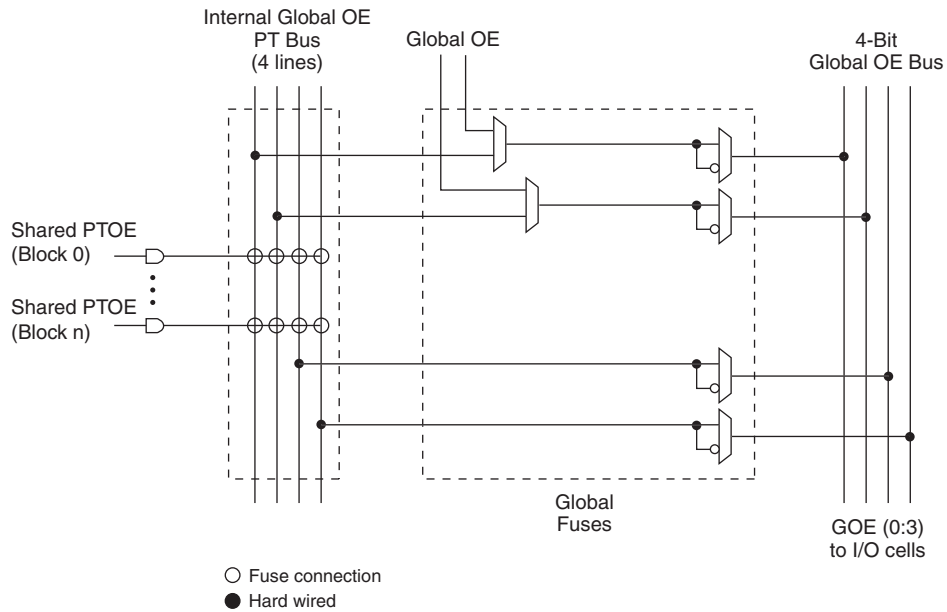
Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

### Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 device that has a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

**Figure 9. Global OE Generation for All Devices Except ispMACH 4032**



## I/O DC Electrical Characteristics

### Over Recommended Operating Conditions

Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$ Max (V)	$V_{OH}$ Min (V)	$I_{OL}^1$ (mA)	$I_{OH}^1$ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTTL	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	$0.35 * V_{CC}$	$0.65 * V_{CC}$	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	$0.3 * 3.3 * (V_{CC} / 1.8)$	$0.5 * 3.3 * (V_{CC} / 1.8)$	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed  $n * 8mA$ . Where  $n$  is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

## ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
t <sub>S</sub>	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
t <sub>R</sub>	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
t <sub>RW</sub>	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
t <sub>G<sub>P</sub>TOE/DIS</sub>	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
t <sub>GOE/DIS</sub>	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
t <sub>CW</sub>	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
f <sub>MAX</sub> (Ext.)	clock frequency with external feedback, [1 / (t <sub>S</sub> + t <sub>CO</sub> )]	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

### ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>GP</sub> TOE	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
t <sub>P</sub> TOE	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

## ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>								
t <sub>IN</sub>	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t <sub>GOE</sub>	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t <sub>GCLK_IN</sub>	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t <sub>BUF</sub>	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t <sub>EN</sub>	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t <sub>DIS</sub>	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
<b>Routing/GLB Delays</b>								
t <sub>ROUTE</sub>	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t <sub>MCELL</sub>	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t <sub>INREG</sub>	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t <sub>FBK</sub>	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t <sub>PDb</sub>	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t <sub>PDi</sub>	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
<b>Register/Latch Delays</b>								
t <sub>S</sub>	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>S_PT</sub>	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t <sub>ST</sub>	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t <sub>ST_PT</sub>	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t <sub>H</sub>	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>HT</sub>	T-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>SIR</sub>	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t <sub>SIR_PT</sub>	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t <sub>HIR</sub>	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t <sub>HIR_PT</sub>	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t <sub>COi</sub>	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t <sub>CES</sub>	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t <sub>CEH</sub>	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t <sub>SL</sub>	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>SL_PT</sub>	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t <sub>HL</sub>	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t <sub>GOi</sub>	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t <sub>PDLi</sub>	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t <sub>SRI</sub>	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t <sub>SRR</sub>	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
<b>Control Delays</b>								
t <sub>BCLK</sub>	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t <sub>PTCLK</sub>	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t <sub>BSR</sub>	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t <sub>PTSR</sub>	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

ispMACH 4000V/B/C Timing Adders<sup>1</sup> (Cont.)

Adder Type	Base Parameter	Description	-5		-75		-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
$t_{INDIO}$	$t_{INREG}$	Input register delay	—	1.00	—	1.00	—	1.00	ns
$t_{EXP}$	$t_{MCELL}$	Product term expander delay	—	0.33	—	0.33	—	0.33	ns
$t_{ORP}$	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	ns
$t_{BLA}$	$t_{ROUTE}$	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
<b><math>t_{IOI}</math> Input Adjusters</b>									
LVTTTL_in	$t_{IN}, t_{GCLK\_IN}, t_{GOE}$	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	$t_{IN}, t_{GCLK\_IN}, t_{GOE}$	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	$t_{IN}, t_{GCLK\_IN}, t_{GOE}$	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	$t_{IN}, t_{GCLK\_IN}, t_{GOE}$	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	$t_{IN}, t_{GCLK\_IN}, t_{GOE}$	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b><math>t_{IOO}</math> Output Adjusters</b>									
LVTTTL_out	$t_{BUF}, t_{EN}, t_{DIS}$	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	$t_{BUF}, t_{EN}, t_{DIS}$	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	$t_{BUF}, t_{EN}, t_{DIS}$	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	$t_{BUF}, t_{EN}, t_{DIS}$	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	$t_{BUF}, t_{EN}, t_{DIS}$	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	$t_{BUF}, t_{EN}$	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.3.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.



**ispMACH 4000Z Timing Adders (Cont.)<sup>1</sup>**

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.30	—	1.30	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

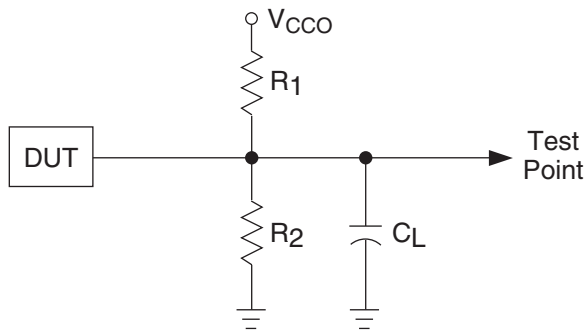
Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding use of these adders.

### Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 11.

**Figure 12. Output Test Load, LVTTTL and LVCMOS Standards**



0213A/ispM4k

**Table 11. Test Fixture Required Components**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub> <sup>1</sup>	Timing Ref.	V <sub>CCO</sub>
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V <sub>CCO</sub> /2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V <sub>CCO</sub> /2	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V <sub>OH</sub> - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V <sub>OL</sub> + 0.3	3.0V

1. C<sub>L</sub> includes test fixtures and probe capacitance.

**ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
K5	0	A15	A <sup>15</sup>	B0	B <sup>0</sup>
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B <sup>0</sup>	C0	C <sup>0</sup>
K7	1	B1	B <sup>1</sup>	C1	C <sup>1</sup>
K8	1	B2	B <sup>2</sup>	C2	C <sup>2</sup>
K9	1	B3	B <sup>3</sup>	C4	C <sup>3</sup>
K10	1	B4	B <sup>4</sup>	C6	C <sup>4</sup>
J10	-	TMS	-	TMS	-
H8	1	B5	B <sup>5</sup>	C8	C <sup>5</sup>
H10	1	B6	B <sup>6</sup>	C10	C <sup>6</sup>
G10	1	B7	B <sup>7</sup>	C11	C <sup>7</sup>
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
F10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B <sup>8</sup>	D15	D <sup>7</sup>
D8	1	B9	B <sup>9</sup>	D12	D <sup>6</sup>
D10	1	B10	B <sup>10</sup>	D10	D <sup>5</sup>
C10	1	B11	B <sup>11</sup>	D8	D <sup>4</sup>
B10	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC <sup>1</sup>	-	I <sup>1</sup>	-
A7	1	B12	B <sup>12</sup>	D6	D <sup>3</sup>
C7	1	B13	B <sup>13</sup>	D4	D <sup>2</sup>
C6	1	B14	B <sup>14</sup>	D2	D <sup>1</sup>
A6	1	B15/GOE1	B <sup>15</sup>	D0/GOE1	D <sup>0</sup>
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>
A4	0	A1	A <sup>1</sup>	A1	A <sup>1</sup>
A3	0	A2	A <sup>2</sup>	A2	A <sup>2</sup>
A2	0	A3	A <sup>3</sup>	A4	A <sup>3</sup>
A1	0	A4	A <sup>4</sup>	A6	A <sup>4</sup>

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:  
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E3	0	NC	-	B8	B^6	D12	D^6
F2	0	A12	A^12	B9	B^7	D10	D^5
F1	0	A13	A^13	B10	B^8	D8	D^4
F3	0	A14	A^14	B12	B^9	D6	D^3
G1	0	A15	A^15	B13	B^10	D4	D^2
G2	0	I	-	B14	B^11	D2	D^1
G3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
H2	0	NC	-	C14	C^11	E2	E^1
H1	0	B15	B^15	C13	C^10	E4	E^2
H3	0	B14	B^14	C12	C^9	E6	E^3
J1	0	B13	B^13	C10	C^8	E8	E^4
J2	0	B12	B^12	C9	C^7	E10	E^5
J3	0	NC	-	C8	C^6	E12	E^6
K2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
K1	0	NC	-	C6	C^5	F2	F^1
K3	0	B11	B^11	C5	C^4	F4	F^2
L2	0	B10	B^10	C4	C^3	F6	F^3
L1	0	B9	B^9	C2	C^2	F8	F^4
L3	0	B8	B^8	C1	C^1	F10	F^5
M1	0	I	-	C0	C^0	F12	F^6
M2	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N1	-	TCK	-	TCK	-	TCK	-
P1	-	VCC	-	VCC	-	VCC	-
P2	-	GND	-	GND	-	GND	-
N2	0	I	-	D14	D^11	G12	G^6
P3	0	B7	B^7	D13	D^10	G10	G^5
M3	0	B6	B^6	D12	D^9	G8	G^4
N3	0	B5	B^5	D10	D^8	G6	G^3
P4	0	B4	B^4	D9	D^7	G4	G^2
M4	0	NC	-	D8	D^6	G2	G^1
N4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
P5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
N5	0	NC	-	D6	D^5	H12	H^6
M5	0	B3	B^3	D5	D^4	H10	H^5
N6	0	B2	B^2	D4	D^3	H8	H^4
P6	0	B1	B^1	D2	D^2	H6	H^3
M6	0	B0	B^0	D1	D^1	H4	H^2
P7	0	NC	-	D0	D^0	H2	H^1
N7	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
M7	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
N8	-	VCC	-	VCC	-	VCC	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E <sup>7</sup>	E10	E <sup>7</sup>	H14	H <sup>7</sup>	J14	J <sup>7</sup>
K3	0	NC	-	E12	E <sup>8</sup>	G0	G <sup>0</sup>	I0	I <sup>0</sup>
K4	0	NC	-	E14	E <sup>9</sup>	G2	G <sup>1</sup>	I4	I <sup>1</sup>
L1	0	NC	-	NC	-	I14	I <sup>7</sup>	K0	K <sup>0</sup>
L2	0	NC	-	NC	-	I12	I <sup>6</sup>	K2	K <sup>1</sup>
M1	0	NC	-	NC	-	NC	-	K4	K <sup>2</sup>
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K <sup>3</sup>
N1	0	NC	-	NC	-	I10	I <sup>5</sup>	K8	K <sup>4</sup>
M3	0	NC	-	NC	-	I8	I <sup>4</sup>	K10	K <sup>5</sup>
M4	0	NC	-	F0	F <sup>0</sup>	G4	G <sup>2</sup>	I8	I <sup>2</sup>
N2	0	NC	-	F1	F <sup>1</sup>	G6	G <sup>3</sup>	I12	I <sup>3</sup>
K5	0	F0	F <sup>0</sup>	F2	F <sup>2</sup>	J0	J <sup>0</sup>	N0	N <sup>0</sup>
P1	0	F2	F <sup>1</sup>	F4	F <sup>3</sup>	J2	J <sup>1</sup>	N2	N <sup>1</sup>
K6	0	F4	F <sup>2</sup>	F6	F <sup>4</sup>	J4	J <sup>2</sup>	N4	N <sup>2</sup>
N3	0	F6	F <sup>3</sup>	F8	F <sup>5</sup>	J6	J <sup>3</sup>	N6	N <sup>3</sup>
L5	0	F8	F <sup>4</sup>	F9	F <sup>6</sup>	J8	J <sup>4</sup>	N8	N <sup>4</sup>
P2	0	F10	F <sup>5</sup>	F10	F <sup>7</sup>	J10	J <sup>5</sup>	N10	N <sup>5</sup>
L6	0	F12	F <sup>6</sup>	F12	F <sup>8</sup>	J12	J <sup>6</sup>	N12	N <sup>6</sup>
R1	0	F14	F <sup>7</sup>	F14	F <sup>9</sup>	J14	J <sup>7</sup>	N14	N <sup>7</sup>
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G <sup>9</sup>	I6	I <sup>3</sup>	K12	K <sup>6</sup>
M5	0	NC	-	G12	G <sup>8</sup>	I4	I <sup>2</sup>	K14	K <sup>7</sup>
N4	0	G14	G <sup>7</sup>	G10	G <sup>7</sup>	K14	K <sup>7</sup>	O14	O <sup>7</sup>
T3	0	G12	G <sup>6</sup>	G9	G <sup>6</sup>	K12	K <sup>6</sup>	O12	O <sup>6</sup>
R3	0	G10	G <sup>5</sup>	G8	G <sup>5</sup>	K10	K <sup>5</sup>	O10	O <sup>5</sup>
M6	0	G8	G <sup>4</sup>	G6	G <sup>4</sup>	K8	K <sup>4</sup>	O8	O <sup>4</sup>
P4	0	G6	G <sup>3</sup>	G4	G <sup>3</sup>	K6	K <sup>3</sup>	O6	O <sup>3</sup>
L7	0	G4	G <sup>2</sup>	G2	G <sup>2</sup>	K4	K <sup>2</sup>	O4	O <sup>2</sup>
N5	0	G2	G <sup>1</sup>	G1	G <sup>1</sup>	K2	K <sup>1</sup>	O2	O <sup>1</sup>
M7	0	G0	G <sup>0</sup>	G0	G <sup>0</sup>	K0	K <sup>0</sup>	O0	O <sup>0</sup>
P5	0	NC	-	NC	-	G8	G <sup>4</sup>	M0	M <sup>0</sup>
R4	0	NC	-	NC	-	G10	G <sup>5</sup>	M4	M <sup>1</sup>
T4	0	NC	-	NC	-	NC	-	L0	L <sup>0</sup>
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
C12	1	O0	O^0	O2	O^2	GX0	GX^0	OX0	OX^0
E10	1	NC	-	O1	O^1	CX8	CX^4	MX0	MX^0
A13	1	NC	-	O0	O^0	CX10	CX^5	MX4	MX^1
D12	1	NC	-	NC	-	NC	-	LX0	LX^0
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B12	1	NC	-	NC	-	NC	-	LX4	LX^1
A12	1	NC	-	NC	-	EX2	EX^1	LX8	LX^2
B11	1	NC	-	NC	-	EX0	EX^0	LX12	LX^3
A11	1	NC	-	P14	P^9	CX12	CX^6	MX8	MX^2
D10	1	NC	-	P12	P^8	CX14	CX^7	MX12	MX^3
C10	1	P14	P^7	P10	P^7	HX14	HX^7	PX14	PX^7
B10	1	P12	P^6	P9	P6	HX12	HX^6	PX12	PX^6
A10	1	P10	P^5	P8	P^5	HX10	HX^5	PX10	PX^5
A9	1	P8	P^4	P6	P^4	HX8	HX^4	PX8	PX^4
F9	1	P6	P^3	P4	P^3	HX6	HX^3	PX6	PX^3
B9	1	P4	P^2	P2	P^2	HX4	HX^2	PX4	PX^2
E9	1	P2/GOE1	P^1	P1/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE1	PX^1
C9	1	P0	P^0	P0	P^0	HX0	HX^0	PX0	PX^0
-	-	GND	-	GND	-	GND	-	GND	-
D9	1	CLK3/I	-	CLK3/I	-	CLK3/I	-	CLK3/I	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
B8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-	CLK0/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
D8	0	A0	A^0	A0	A^0	A0	A^0	A0	A^0
C8	0	A2/GOE0	A^1	A1/GOE0	A^1	A2/GOE0	A^1	A2/GOE0	A^1
A8	0	A4	A^2	A2	A^2	A4	A^2	A4	A^2
A7	0	A6	A^3	A4	A^3	A6	A^3	A6	A^3
B7	0	A8	A^4	A6	A^4	A8	A^4	A8	A^4
E8	0	A10	A^5	A8	A^5	A10	A^5	A10	A^5
D7	0	A12	A^6	A9	A^6	A12	A^6	A12	A^6
F8	0	A14	A^7	A10	A^7	A14	A^7	A14	A^7
C7	0	NC	-	A12	A^8	F14	F^7	D0	D^0
A6	0	NC	-	A14	A^9	F12	F^6	D4	D^1
B6	0	NC	-	NC	-	D14	D^7	E0	E^0
A5	0	NC	-	NC	-	D12	D^6	E4	E^1
B5	0	NC	-	NC	-	NC	-	E8	E^2
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
D5	0	NC	-	NC	-	NC	-	E12	E^3
A4	0	NC	-	B0	B^0	F10	F^5	D8	D^2

## ispMACH 4000C (1.8V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92	C
	LC4128C-5T128C	128	1.8	5	TQFP	128	92	C
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92	C
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64	C
	LC4128C-5T100C	128	1.8	5	TQFP	100	64	C
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256C	LC4256C-3FT256AC	256	1.8	3	ftBGA	256	128	C
	LC4256C-5FT256AC	256	1.8	5	ftBGA	256	128	C
	LC4256C-75FT256AC	256	1.8	7.5	ftBGA	256	128	C
	LC4256C-3FT256BC	256	1.8	3	ftBGA	256	160	C
	LC4256C-5FT256BC	256	1.8	5	ftBGA	256	160	C
	LC4256C-75FT256BC	256	1.8	7.5	ftBGA	256	160	C
	LC4256C-3F256AC <sup>1</sup>	256	1.8	3	fpBGA	256	128	C
	LC4256C-5F256AC <sup>1</sup>	256	1.8	5	fpBGA	256	128	C
	LC4256C-75F256AC <sup>1</sup>	256	1.8	7.5	fpBGA	256	128	C
	LC4256C-3F256BC <sup>1</sup>	256	1.8	3	fpBGA	256	160	C
	LC4256C-5F256BC <sup>1</sup>	256	1.8	5	fpBGA	256	160	C
	LC4256C-75F256BC <sup>1</sup>	256	1.8	7.5	fpBGA	256	160	C
	LC4256C-3T176C	256	1.8	3	TQFP	176	128	C
	LC4256C-5T176C	256	1.8	5	TQFP	176	128	C
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256C-3T100C	256	1.8	3	TQFP	100	64	C
LC4256C-5T100C	256	1.8	5	TQFP	100	64	C	
LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C	
LC4384C	LC4384C-35FT256C	384	1.8	3.5	ftBGA	256	192	C
	LC4384C-5FT256C	384	1.8	5	ftBGA	256	192	C
	LC4384C-75FT256C	384	1.8	7.5	ftBGA	256	192	C
	LC4384C-35F256C <sup>1</sup>	384	1.8	3.5	fpBGA	256	192	C
	LC4384C-5F256C <sup>1</sup>	384	1.8	5	fpBGA	256	192	C
	LC4384C-75F256C <sup>1</sup>	384	1.8	7.5	fpBGA	256	192	C
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128	C
	LC4384C-5T176C	384	1.8	5	TQFP	176	128	C
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128	C
LC4512C	LC4512C-35FT256C	512	1.8	3.5	ftBGA	256	208	C
	LC4512C-5FT256C	512	1.8	5	ftBGA	256	208	C
	LC4512C-75FT256C	512	1.8	7.5	ftBGA	256	208	C
	LC4512C-35F256C <sup>1</sup>	512	1.8	3.5	fpBGA	256	208	C
	LC4512C-5F256C <sup>1</sup>	512	1.8	5	fpBGA	256	208	C
	LC4512C-75F256C <sup>1</sup>	512	1.8	7.5	fpBGA	256	208	C
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
	LC4512C-5T176C	512	1.8	5	TQFP	176	128	C
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I <sup>1</sup>	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I <sup>1</sup>	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I <sup>1</sup>	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I <sup>1</sup>	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I <sup>1</sup>	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I <sup>1</sup>	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C



## ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-5FT256I	384	2.5	5	ftBGA	256	192	I
	LC4384B-75FT256I	384	2.5	7.5	ftBGA	256	192	I
	LC4384B-10FT256I	384	2.5	10	ftBGA	256	192	I
	LC4384B-5F256I <sup>1</sup>	384	2.5	5	fpBGA	256	192	I
	LC4384B-75F256I <sup>1</sup>	384	2.5	7.5	fpBGA	256	192	I
	LC4384B-10F256I <sup>1</sup>	384	2.5	10	fpBGA	256	192	I
	LC4384B-5T176I	384	2.5	5	TQFP	176	128	I
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128	I
	LC4384B-10T176I	384	2.5	10	TQFP	176	128	I
LC4512B	LC4512B-5FT256I	512	2.5	5	ftBGA	256	208	I
	LC4512B-75FT256I	512	2.5	7.5	ftBGA	256	208	I
	LC4512B-10FT256I	512	2.5	10	ftBGA	256	208	I
	LC4512B-5F256I <sup>1</sup>	512	2.5	5	fpBGA	256	208	I
	LC4512B-75F256I <sup>1</sup>	512	2.5	7.5	fpBGA	256	208	I
	LC4512B-10F256I <sup>1</sup>	512	2.5	10	fpBGA	256	208	I
	LC4512B-5T176I	512	2.5	5	TQFP	176	128	I
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
	LC4512B-10T176I	512	2.5	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32	C
	LC4032V-5T48C	32	3.3	5	TQFP	48	32	C
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32	C
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30	C
	LC4032V-5T44C	32	3.3	5	TQFP	44	30	C
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30	C
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64	C
	LC4064V-5T100C	64	3.3	5	TQFP	100	64	C
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64	C
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32	C
	LC4064V-5T48C	64	3.3	5	TQFP	48	32	C
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32	C
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30	C
	LC4064V-5T44C	64	3.3	5	TQFP	44	30	C
LC4064V-75T44C	64	3.3	7.5	TQFP	44	30	C	

## ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4512V	LC4512V-35FT256C	512	3.3	3.5	ftBGA	256	208	C
	LC4512V-5FT256C	512	3.3	5	ftBGA	256	208	C
	LC4512V-75FT256C	512	3.3	7.5	ftBGA	256	208	C
	LC4512V-35F256C <sup>1</sup>	512	3.3	3.5	fpBGA	256	208	C
	LC4512V-5F256C <sup>1</sup>	512	3.3	5	fpBGA	256	208	C
	LC4512V-75F256C <sup>1</sup>	512	3.3	7.5	fpBGA	256	208	C
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128	C
	LC4512V-5T176C	512	3.3	5	TQFP	176	128	C
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32	I
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32	I
	LC4032V-10T48I	32	3.3	10	TQFP	48	32	I
	LC4032V-5T44I	32	3.3	5	TQFP	44	30	I
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30	I
	LC4032V-10T44I	32	3.3	10	TQFP	44	30	I
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64	I
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64	I
	LC4064V-10T100I	64	3.3	10	TQFP	100	64	I
	LC4064V-5T48I	64	3.3	5	TQFP	48	32	I
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32	I
	LC4064V-10T48I	64	3.3	10	TQFP	48	32	I
	LC4064V-5T44I	64	3.3	5	TQFP	44	30	I
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30	I
	LC4064V-10T44I	64	3.3	10	TQFP	44	30	I
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96	I
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96	I
	LC4128V-10T144I	128	3.3	10	TQFP	144	96	I
	LC4128V-5T128I	128	3.3	5	TQFP	128	92	I
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92	I
	LC4128V-10T128I	128	3.3	10	TQFP	128	92	I
	LC4128V-5T100I	128	3.3	5	TQFP	100	64	I
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64	I
	LC4128V-10T100I	128	3.3	10	TQFP	100	64	I

## ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C <sup>1</sup>	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C <sup>1</sup>	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C <sup>1</sup>	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C <sup>1</sup>	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C <sup>1</sup>	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C <sup>1</sup>	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

## ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

## Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ( $0 \leq V_{IN} \leq 3.6V$ ).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided ( $V_{IN} - V_{CCO}$ ) $\leq$ 3.6V.
		Improved LC4064ZC t <sub>S</sub> to 2.5ns, t <sub>ST</sub> to 2.7ns and f <sub>MAX</sub> (Ext.) to 175MHz, LC4128ZC t <sub>CO</sub> to 3.5ns and f <sub>MAX</sub> (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs

**Revision History (Cont.)**

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated $I_{PU}$ (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 $\mu$ A to -200 $\mu$ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage ( $I_{IH}$ ) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to "LA" automotive data sheet under the "Broad Device Offering" bullet.
		Added footnote 1 to Part Number Description to reference the "LA" automotive data sheet.
		Changed device temperature references from 'Automotive' to "Extended Temperature" for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to $t_{CW}$ , $t_{GW}$ , $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to $t_{CW}$ , $t_{GW}$ , $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000V/B/C External Switching Characteristics table.