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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 105°C (Tj)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032zc-5tn48i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032zc-5tn48i</a>

## Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

**Table 3. Individual PT Steering**

Product Term	Logic	Control
PT $n$	Logic PT	Single PT for XOR/OR
PT $n+1$	Logic PT	Individual Clock (PT Clock)
PT $n+2$	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT $n+3$	Logic PT	Individual Initialization (PT Initialization)
PT $n+4$	Logic PT	Individual OE (PTOE)

## Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

**Table 4. Available Clusters for Each Macrocell**

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

## Wide Steering Logic

The wide steering logic allows the output of the cluster allocator  $n$  to be connected to the input of the cluster allocator  $n+4$ . Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.

## ispMACH 4000Z External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	3.5	—	3.7	—	4.2	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	4.4	—	4.7	—	5.7	ns
t <sub>S</sub>	GLB register setup time before clock	2.2	—	2.5	—	2.7	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	2.4	—	2.7	—	2.9	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.6	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.5	ns
t <sub>R</sub>	External reset pin to output delay	—	5.0	—	6.0	—	7.3	ns
t <sub>RW</sub>	External reset pulse duration	1.5	—	1.7	—	2.0	—	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.0	ns
t <sub>G<sub>P</sub>TOE/DIS</sub>	Input to output global product term output enable/disable	—	6.5	—	7.0	—	8.0	ns
t <sub>G<sub>O</sub>E/DIS</sub>	Global OE input to output enable/disable	—	4.5	—	4.5	—	4.8	ns
t <sub>CW</sub>	Global clock width, high or low	1.0	—	1.5	—	1.8	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	267	—	250	—	220	MHz
f <sub>MAX</sub> (Ext.)	clock frequency with external feedback, [1 / (t <sub>S</sub> + t <sub>CO</sub> )]	—	192	—	175	—	161	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

## ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description <sup>1, 2, 3</sup>	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t <sub>PD_MC</sub>	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t <sub>S</sub>	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t <sub>ST</sub>	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t <sub>SIR</sub>	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t <sub>SIRZ</sub>	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t <sub>H</sub>	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t <sub>HT</sub>	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t <sub>HIR</sub>	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t <sub>HIRZ</sub>	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t <sub>CO</sub>	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t <sub>R</sub>	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t <sub>RW</sub>	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
t <sub>P<sub>TOE/DIS</sub></sub>	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
t <sub>G<sub>P<sub>TOE/DIS</sub></sub></sub>	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
t <sub>G<sub>OE/DIS</sub></sub>	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t <sub>CW</sub>	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t <sub>GW</sub>	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t <sub>WIR</sub>	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f <sub>MAX</sub> <sup>4</sup>	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f <sub>MAX</sub> (Ext.)	clock frequency with external feedback, [1 / (t <sub>S</sub> + t <sub>CO</sub> )]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

**ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
$t_{PDLi}$	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
$t_{SRi}$	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
$t_{SRR}$	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
<b>Control Delays</b>										
$t_{BCLK}$	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
$t_{PTCLK}$	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
$t_{BSR}$	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
$t_{PTSR}$	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
$t_{GPtoE}$	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
$t_{PtoE}$	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

**ispMACH 4000V/B/C Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>GP</sub> TOE	Global PT OE Delay	—	5.58	—	5.58	—	5.78	ns
t <sub>P</sub> TOE	Macrocell PT OE Delay	—	3.58	—	4.28	—	4.28	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

## ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>								
t <sub>IN</sub>	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t <sub>GOE</sub>	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t <sub>GCLK_IN</sub>	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t <sub>BUF</sub>	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t <sub>EN</sub>	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t <sub>DIS</sub>	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
<b>Routing/GLB Delays</b>								
t <sub>ROUTE</sub>	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t <sub>MCELL</sub>	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t <sub>INREG</sub>	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t <sub>FBK</sub>	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t <sub>PDb</sub>	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t <sub>PDi</sub>	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
<b>Register/Latch Delays</b>								
t <sub>S</sub>	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>S_PT</sub>	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t <sub>ST</sub>	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t <sub>ST_PT</sub>	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t <sub>H</sub>	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>HT</sub>	T-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>SIR</sub>	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t <sub>SIR_PT</sub>	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t <sub>HIR</sub>	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t <sub>HIR_PT</sub>	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t <sub>COi</sub>	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t <sub>CES</sub>	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t <sub>CEH</sub>	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t <sub>SL</sub>	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>SL_PT</sub>	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t <sub>HL</sub>	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t <sub>GOi</sub>	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t <sub>PDLi</sub>	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t <sub>SRI</sub>	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t <sub>SRR</sub>	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
<b>Control Delays</b>								
t <sub>BCLK</sub>	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t <sub>PTCLK</sub>	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t <sub>BSR</sub>	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t <sub>PTSR</sub>	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

## ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>GP</sub> TOE	Global PT OE Delay	—	1.9	—	2.35	—	2.60	ns
t <sub>P</sub> TOE	Macrocell PT OE Delay	—	2.4	—	3.35	—	2.60	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.

Timing v.2.2



**ispMACH 4000Z Timing Adders <sup>1</sup>**

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Optional Delay Adders</b>									
t <sub>INDIO</sub>	t <sub>INREG</sub>	Input register delay	—	1.00	—	1.00	—	1.30	ns
t <sub>EXP</sub>	t <sub>MCELL</sub>	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t <sub>ORP</sub>	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t <sub>BLA</sub>	t <sub>ROUTE</sub>	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Adjusters</b>									
LVTTTL_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
<b>t<sub>IOO</sub> Output Adjusters</b>									
LVTTTL_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t <sub>BUF</sub> , t <sub>EN</sub> , t <sub>DIS</sub>	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t <sub>BUF</sub> , t <sub>EN</sub>	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing. Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:  
44-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:  
44-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A <sup>2</sup>	A4	A <sup>2</sup>
43	0	A3	A <sup>3</sup>	A6	A <sup>3</sup>
44	0	A4	A <sup>4</sup>	A8	A <sup>4</sup>

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:  
48-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-	TDI	-
2	0	A5	A <sup>5</sup>	A10	A <sup>5</sup>	A8	A <sup>5</sup>
3	0	A6	A <sup>6</sup>	A12	A <sup>6</sup>	A10	A <sup>6</sup>
4	0	A7	A <sup>7</sup>	A14	A <sup>7</sup>	A11	A <sup>7</sup>
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A <sup>8</sup>	B0	B <sup>0</sup>	B15	B <sup>7</sup>
8	0	A9	A <sup>9</sup>	B2	B <sup>1</sup>	B12	B <sup>6</sup>
9	0	A10	A <sup>10</sup>	B4	B <sup>2</sup>	B10	B <sup>5</sup>
10	0	A11	A <sup>11</sup>	B6	B <sup>3</sup>	B8	B <sup>4</sup>
11	-	TCK	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-	VCC	-
13	-	GND	-	GND	-	GND	-
14	0	A12	A <sup>12</sup>	B8	B <sup>4</sup>	B6	B <sup>3</sup>
15	0	A13	A <sup>13</sup>	B10	B <sup>5</sup>	B4	B <sup>2</sup>
16	0	A14	A <sup>14</sup>	B12	B <sup>6</sup>	B2	B <sup>1</sup>
17	0	A15	A <sup>15</sup>	B14	B <sup>7</sup>	B0	B <sup>0</sup>
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
20	1	B0	B <sup>0</sup>	C0	C <sup>0</sup>	C0	C <sup>0</sup>
21	1	B1	B <sup>1</sup>	C2	C <sup>1</sup>	C1	C <sup>1</sup>
22	1	B2	B <sup>2</sup>	C4	C <sup>2</sup>	C2	C <sup>2</sup>
23	1	B3	B <sup>3</sup>	C6	C <sup>3</sup>	C4	C <sup>3</sup>
24	1	B4	B <sup>4</sup>	C8	C <sup>4</sup>	C6	C <sup>4</sup>
25	-	TMS	-	TMS	-	TMS	-
26	1	B5	B <sup>5</sup>	C10	C <sup>5</sup>	C8	C <sup>5</sup>
27	1	B6	B <sup>6</sup>	C12	C <sup>6</sup>	C10	C <sup>6</sup>
28	1	B7	B <sup>7</sup>	C14	C <sup>7</sup>	C11	C <sup>7</sup>
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B <sup>8</sup>	D0	D <sup>0</sup>	D15	D <sup>7</sup>
32	1	B9	B <sup>9</sup>	D2	D <sup>1</sup>	D12	D <sup>6</sup>

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-

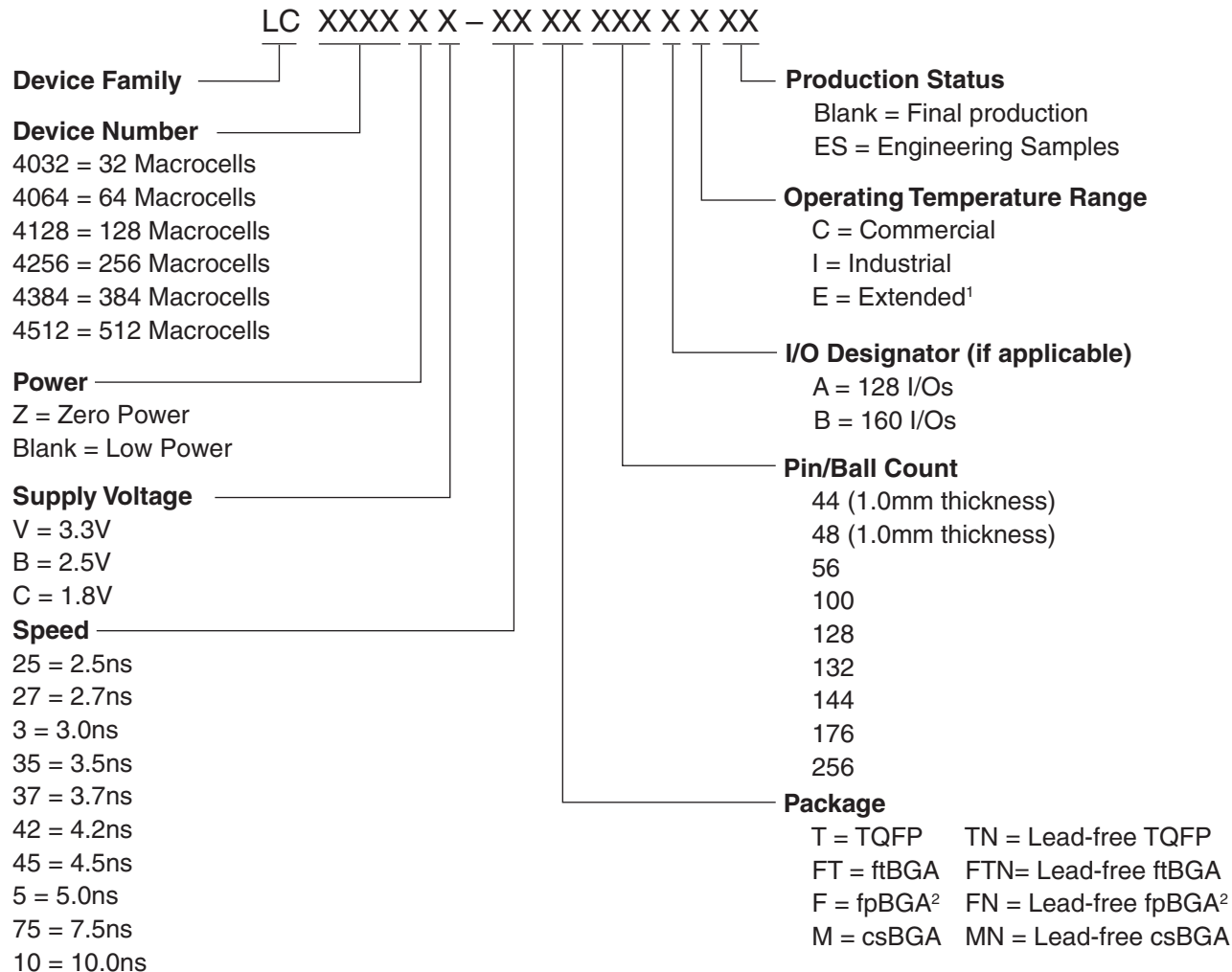
**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E <sup>7</sup>	E10	E <sup>7</sup>	H14	H <sup>7</sup>	J14	J <sup>7</sup>
K3	0	NC	-	E12	E <sup>8</sup>	G0	G <sup>0</sup>	I0	I <sup>0</sup>
K4	0	NC	-	E14	E <sup>9</sup>	G2	G <sup>1</sup>	I4	I <sup>1</sup>
L1	0	NC	-	NC	-	I14	I <sup>7</sup>	K0	K <sup>0</sup>
L2	0	NC	-	NC	-	I12	I <sup>6</sup>	K2	K <sup>1</sup>
M1	0	NC	-	NC	-	NC	-	K4	K <sup>2</sup>
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K <sup>3</sup>
N1	0	NC	-	NC	-	I10	I <sup>5</sup>	K8	K <sup>4</sup>
M3	0	NC	-	NC	-	I8	I <sup>4</sup>	K10	K <sup>5</sup>
M4	0	NC	-	F0	F <sup>0</sup>	G4	G <sup>2</sup>	I8	I <sup>2</sup>
N2	0	NC	-	F1	F <sup>1</sup>	G6	G <sup>3</sup>	I12	I <sup>3</sup>
K5	0	F0	F <sup>0</sup>	F2	F <sup>2</sup>	J0	J <sup>0</sup>	N0	N <sup>0</sup>
P1	0	F2	F <sup>1</sup>	F4	F <sup>3</sup>	J2	J <sup>1</sup>	N2	N <sup>1</sup>
K6	0	F4	F <sup>2</sup>	F6	F <sup>4</sup>	J4	J <sup>2</sup>	N4	N <sup>2</sup>
N3	0	F6	F <sup>3</sup>	F8	F <sup>5</sup>	J6	J <sup>3</sup>	N6	N <sup>3</sup>
L5	0	F8	F <sup>4</sup>	F9	F <sup>6</sup>	J8	J <sup>4</sup>	N8	N <sup>4</sup>
P2	0	F10	F <sup>5</sup>	F10	F <sup>7</sup>	J10	J <sup>5</sup>	N10	N <sup>5</sup>
L6	0	F12	F <sup>6</sup>	F12	F <sup>8</sup>	J12	J <sup>6</sup>	N12	N <sup>6</sup>
R1	0	F14	F <sup>7</sup>	F14	F <sup>9</sup>	J14	J <sup>7</sup>	N14	N <sup>7</sup>
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G <sup>9</sup>	I6	I <sup>3</sup>	K12	K <sup>6</sup>
M5	0	NC	-	G12	G <sup>8</sup>	I4	I <sup>2</sup>	K14	K <sup>7</sup>
N4	0	G14	G <sup>7</sup>	G10	G <sup>7</sup>	K14	K <sup>7</sup>	O14	O <sup>7</sup>
T3	0	G12	G <sup>6</sup>	G9	G <sup>6</sup>	K12	K <sup>6</sup>	O12	O <sup>6</sup>
R3	0	G10	G <sup>5</sup>	G8	G <sup>5</sup>	K10	K <sup>5</sup>	O10	O <sup>5</sup>
M6	0	G8	G <sup>4</sup>	G6	G <sup>4</sup>	K8	K <sup>4</sup>	O8	O <sup>4</sup>
P4	0	G6	G <sup>3</sup>	G4	G <sup>3</sup>	K6	K <sup>3</sup>	O6	O <sup>3</sup>
L7	0	G4	G <sup>2</sup>	G2	G <sup>2</sup>	K4	K <sup>2</sup>	O4	O <sup>2</sup>
N5	0	G2	G <sup>1</sup>	G1	G <sup>1</sup>	K2	K <sup>1</sup>	O2	O <sup>1</sup>
M7	0	G0	G <sup>0</sup>	G0	G <sup>0</sup>	K0	K <sup>0</sup>	O0	O <sup>0</sup>
P5	0	NC	-	NC	-	G8	G <sup>4</sup>	M0	M <sup>0</sup>
R4	0	NC	-	NC	-	G10	G <sup>5</sup>	M4	M <sup>1</sup>
T4	0	NC	-	NC	-	NC	-	L0	L <sup>0</sup>
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R5	0	NC	-	NC	-	NC	-	L4	L^1
T5	0	NC	-	NC	-	I2	I^1	L8	L^2
R6	0	NC	-	NC	-	I0	I^0	L12	L^3
T6	0	NC	-	H14	H^9	G12	G^6	M8	M^2
N7	0	NC	-	H12	H^8	G14	G^7	M12	M^3
P7	0	H14	H^7	H10	H^7	L14	L^7	P14	P^7
R7	0	H12	H^6	H9	H^6	L12	L^6	P12	P^6
L8	0	H10	H^5	H8	H^5	L10	L^5	P10	P^5
T7	0	H8	H^4	H6	H^4	L8	L^4	P8	P^4
M8	0	H6	H^3	H4	H^3	L6	L^3	P6	P^3
N8	0	H4	H^2	H2	H^2	L4	L^2	P4	P^2
R8	0	H2	H^1	H1	H^1	L2	L^1	P2	P^1
P8	0	H0	H^0	H0	H^0	L0	L^0	P0	P^0
-	-	GND	-	GND	-	GND	-	GND	-
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
P9	1	I0	I^0	I0	I^0	M0	M^0	AX0	AX^0
R9	1	I2	I^1	I1	I^1	M2	M^1	AX2	AX^1
T9	1	I4	I^2	I2	I^2	M4	M^2	AX4	AX^2
T10	1	I6	I^3	I4	I^3	M6	M^3	AX6	AX^3
R10	1	I8	I^4	I6	I^4	M8	M^4	AX8	AX^4
M9	1	I10	I^5	I8	I^5	M10	M^5	AX10	AX^5
P10	1	I12	I^6	I9	I^6	M12	M^6	AX12	AX^6
L9	1	I14	I^7	I10	I^7	M14	M^7	AX14	AX^7
N10	1	NC	-	I12	I^8	BX14	BX^7	DX0	DX^0
T11	1	NC	-	I14	I^9	BX12	BX^6	DX4	DX^1
R11	1	NC	-	NC	-	P0	P^0	EX0	EX^0
T12	1	NC	-	NC	-	P2	P^1	EX4	EX^1
N12	1	NC	-	NC	-	NC	-	EX8	EX^2
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
R12	1	NC	-	NC	-	NC	-	EX12	EX^3
T13	1	NC	-	J0	J^0	BX10	BX^5	DX8	DX^2
P12	1	NC	-	J1	J^1	BX8	BX^4	DX12	DX^3
M10	1	J0	J^0	J2	J^2	N0	N^0	BX0	BX^0
R13	1	J2	J^1	J4	J^3	N2	N^1	BX2	BX^1
L10	1	J4	J^2	J6	J^4	N4	N^2	BX4	BX^2
T14	1	J6	J^3	J8	J^5	N6	N^3	BX6	BX^3
M11	1	J8	J^4	J9	J^6	N8	N^4	BX8	BX^4

### Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).  
 2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

### ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

## Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispMACH 4000Z devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

## Conventional Packaging

### ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35M56C	32	1.8	3.5	csBGA	56	32	C
	LC4032ZC-5M56C	32	1.8	5	csBGA	56	32	C
	LC4032ZC-75M56C	32	1.8	7.5	csBGA	56	32	C
	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32	C
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32	C
LC4064ZC	LC4064ZC-37M132C	64	1.8	3.7	csBGA	132	64	C
	LC4064ZC-5M132C	64	1.8	5	csBGA	132	64	C
	LC4064ZC-75M132C	64	1.8	7.5	csBGA	132	64	C
	LC4064ZC-37T100C	64	1.8	3.7	TQFP	100	64	C
	LC4064ZC-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064ZC-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064ZC-37M56C	64	1.8	3.7	csBGA	56	32	C
	LC4064ZC-5M56C	64	1.8	5	csBGA	56	32	C
	LC4064ZC-75M56C	64	1.8	7.5	csBGA	56	32	C
	LC4064ZC-37T48C	64	1.8	3.7	TQFP	48	32	C
	LC4064ZC-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064ZC-75T48C	64	1.8	7.5	TQFP	48	32	C
LC4128ZC	LC4128ZC-42M132C	128	1.8	4.2	csBGA	132	96	C
	LC4128ZC-75M132C	128	1.8	7.5	csBGA	132	96	C
	LC4128ZC-42T100C	128	1.8	4.2	TQFP	100	64	C
	LC4128ZC-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256ZC	LC4256ZC-45T176C	256	1.8	4.5	TQFP	176	128	C
	LC4256ZC-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256ZC-45M132C	256	1.8	4.5	csBGA	132	96	C
	LC4256ZC-75M132C	256	1.8	7.5	csBGA	132	96	C
	LC4256ZC-45T100C	256	1.8	4.5	TQFP	100	64	C
	LC4256ZC-75T100C	256	1.8	7.5	TQFP	100	64	C

### ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5M56I	32	1.8	5	csBGA	56	32	I
	LC4032ZC-75M56I	32	1.8	7.5	csBGA	56	32	I
	LC4032ZC-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032ZC-75T48I	32	1.8	7.5	TQFP	48	32	I



## ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI <sup>1</sup>	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI <sup>1</sup>	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI <sup>1</sup>	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI <sup>1</sup>	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I	
LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I	
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I <sup>1</sup>	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I <sup>1</sup>	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I <sup>1</sup>	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I	
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I <sup>1</sup>	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I <sup>1</sup>	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I <sup>1</sup>	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I	

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4128B	LC4128B-5TN128I	128	2.5	5	Lead-Free TQFP	128	92	I
	LC4128B-75TN128I	128	2.5	7.5	Lead-Free TQFP	128	92	I
	LC4128B-10TN128I	128	2.5	10	Lead-Free TQFP	128	92	I
	LC4128B-5TN100I	128	2.5	5	Lead-Free TQFP	100	64	I
	LC4128B-75TN100I	128	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4128B-10TN100I	128	2.5	10	Lead-Free TQFP	100	64	I
LC4256B	LC4256B-5FTN256AI	256	2.5	5	Lead-Free ftBGA	256	128	I
	LC4256B-75FTN256AI	256	2.5	7.5	Lead-Free ftBGA	256	128	I
	LC4256B-10FTN256AI	256	2.5	10	Lead-Free ftBGA	256	128	I
	LC4256B-5FTN256BI	256	2.5	5	Lead-Free ftBGA	256	160	I
	LC4256B-75FTN256BI	256	2.5	7.5	Lead-Free ftBGA	256	160	I
	LC4256B-10FTN256BI	256	2.5	10	Lead-Free ftBGA	256	160	I
	LC4256B-5FN256AI <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	128	I
	LC4256B-75FN256AI <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	128	I
	LC4256B-10FN256AI <sup>1</sup>	256	2.5	10	Lead-Free fpBGA	256	128	I
	LC4256B-5FN256BI <sup>1</sup>	256	2.5	5	Lead-Free fpBGA	256	160	I
	LC4256B-75FN256BI <sup>1</sup>	256	2.5	7.5	Lead-Free fpBGA	256	160	I
	LC4256B-10FN256BI <sup>1</sup>	256	2.5	10	Lead-Free fpBGA	256	160	I
	LC4256B-5TN176I	256	2.5	5	Lead-Free TQFP	176	128	I
	LC4256B-75TN176I	256	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4256B-10TN176I	256	2.5	10	Lead-Free TQFP	176	128	I
	LC4256B-5TN100I	256	2.5	5	Lead-Free TQFP	100	64	I
LC4256B-75TN100I	256	2.5	7.5	Lead-Free TQFP	100	64	I	
LC4256B-10TN100I	256	2.5	10	Lead-Free TQFP	100	64	I	
LC4384B	LC4384B-5FTN256I	384	2.5	5	Lead-Free ftBGA	256	192	I
	LC4384B-75FTN256I	384	2.5	7.5	Lead-Free ftBGA	256	192	I
	LC4384B-10FTN256I	384	2.5	10	Lead-Free ftBGA	256	192	I
	LC4384B-5FN256I <sup>1</sup>	384	2.5	5	Lead-Free fpBGA	256	192	I
	LC4384B-75FN256I <sup>1</sup>	384	2.5	7.5	Lead-Free fpBGA	256	192	I
	LC4384B-10FN256I <sup>1</sup>	384	2.5	10	Lead-Free fpBGA	256	192	I
	LC4384B-5TN176I	384	2.5	5	Lead-Free TQFP	176	128	I
	LC4384B-75TN176I	384	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4384B-10TN176I	384	2.5	10	Lead-Free TQFP	176	128	I
LC4512B	LC4512B-5FTN256I	512	2.5	5	Lead-Free ftBGA	256	208	I
	LC4512B-75FTN256I	512	2.5	7.5	Lead-Free ftBGA	256	208	I
	LC4512B-10FTN256I	512	2.5	10	Lead-Free ftBGA	256	208	I
	LC4512B-5FN256I <sup>1</sup>	512	2.5	5	Lead-Free fpBGA	256	208	I
	LC4512B-75FN256I <sup>1</sup>	512	2.5	7.5	Lead-Free fpBGA	256	208	I
	LC4512B-10FN256I <sup>1</sup>	512	2.5	10	Lead-Free fpBGA	256	208	I
	LC4512B-5TN176I	512	2.5	5	Lead-Free TQFP	176	128	I
	LC4512B-75TN176I	512	2.5	7.5	Lead-Free TQFP	176	128	I
LC4512B-10TN176I	512	2.5	10	Lead-Free TQFP	176	128	I	

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25TN48C	32	3.3	2.5	Lead-free TQFP	48	32	C
	LC4032V-5TN48C	32	3.3	5	Lead-free TQFP	48	32	C
	LC4032V-75TN48C	32	3.3	7.5	Lead-free TQFP	48	32	C
	LC4032V-25TN44C	32	3.3	2.5	Lead-free TQFP	44	30	C
	LC4032V-5TN44C	32	3.3	5	Lead-free TQFP	44	30	C
	LC4032V-75TN44C	32	3.3	7.5	Lead-free TQFP	44	30	C
LC4064V	LC4064V-25TN100C	64	3.3	2.5	Lead-free TQFP	100	64	C
	LC4064V-5TN100C	64	3.3	5	Lead-free TQFP	100	64	C
	LC4064V-75TN100C	64	3.3	7.5	Lead-free TQFP	100	64	C
	LC4064V-25TN48C	64	3.3	2.5	Lead-free TQFP	48	32	C
	LC4064V-5TN48C	64	3.3	5	Lead-free TQFP	48	32	C
	LC4064V-75TN48C	64	3.3	7.5	Lead-free TQFP	48	32	C
	LC4064V-25TN44C	64	3.3	2.5	Lead-free TQFP	44	30	C
	LC4064V-5TN44C	64	3.3	5	Lead-free TQFP	44	30	C
LC4064V-75TN44C	64	3.3	7.5	Lead-free TQFP	44	30	C	
LC4128V	LC4128V-27TN144C	128	3.3	2.7	Lead-free TQFP	144	96	C
	LC4128V-5TN144C	128	3.3	5	Lead-free TQFP	144	96	C
	LC4128V-75TN144C	128	3.3	7.5	Lead-free TQFP	144	96	C
	LC4128V-27TN128C	128	3.3	2.7	Lead-free TQFP	128	92	C
	LC4128V-5TN128C	128	3.3	5	Lead-free TQFP	128	92	C
	LC4128V-75TN128C	128	3.3	7.5	Lead-free TQFP	128	92	C
	LC4128V-27TN100C	128	3.3	2.7	Lead-free TQFP	100	64	C
	LC4128V-5TN100C	128	3.3	5	Lead-free TQFP	100	64	C
LC4128V-75TN100C	128	3.3	7.5	Lead-free TQFP	100	64	C	

## ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FTN256AI	256	3.3	5	Lead-free ftBGA	256	128	I
	LC4256V-75FTN256AI	256	3.3	7.5	Lead-free ftBGA	256	128	I
	LC4256V-10FTN256AI	256	3.3	10	Lead-free ftBGA	256	128	I
	LC4256V-5FTN256BI	256	3.3	5	Lead-free ftBGA	256	160	I
	LC4256V-75FTN256BI	256	3.3	7.5	Lead-free ftBGA	256	160	I
	LC4256V-10FTN256BI	256	3.3	10	Lead-free ftBGA	256	160	I
	LC4256V-5FN256AI <sup>1</sup>	256	3.3	5	Lead-free fpBGA	256	128	I
	LC4256V-75FN256AI <sup>1</sup>	256	3.3	7.5	Lead-free fpBGA	256	128	I
	LC4256V-10FN256AI <sup>1</sup>	256	3.3	10	Lead-free fpBGA	256	128	I
	LC4256V-5FN256BI <sup>1</sup>	256	3.3	5	Lead-free fpBGA	256	160	I
	LC4256V-75FN256BI <sup>1</sup>	256	3.3	7.5	Lead-free fpBGA	256	160	I
	LC4256V-10FN256BI <sup>1</sup>	256	3.3	10	Lead-free fpBGA	256	160	I
	LC4256V-5TN176I	256	3.3	5	Lead-free TQFP	176	128	I
	LC4256V-75TN176I	256	3.3	7.5	Lead-free TQFP	176	128	I
	LC4256V-10TN176I	256	3.3	10	Lead-free TQFP	176	128	I
	LC4256V-5TN144I	256	3.3	5	Lead-free TQFP	144	96	I
	LC4256V-75TN144I	256	3.3	7.5	Lead-free TQFP	144	96	I
	LC4256V-10TN144I	256	3.3	10	Lead-free TQFP	144	96	I
	LC4256V-5TN100I	256	3.3	5	Lead-free TQFP	100	64	I
	LC4256V-75TN100I	256	3.3	7.5	Lead-free TQFP	100	64	I
LC4256V-10TN100I	256	3.3	10	Lead-free TQFP	100	64	I	
LC4384V	LC4384V-5FTN256I	384	3.3	5	Lead-free ftBGA	256	192	I
	LC4384V-75FTN256I	384	3.3	7.5	Lead-free ftBGA	256	192	I
	LC4384V-10FTN256I	384	3.3	10	Lead-free ftBGA	256	192	I
	LC4384V-5FN256I <sup>1</sup>	384	3.3	5	Lead-free fpBGA	256	192	I
	LC4384V-75FN256I <sup>1</sup>	384	3.3	7.5	Lead-free fpBGA	256	192	I
	LC4384V-10FN256I <sup>1</sup>	384	3.3	10	Lead-free fpBGA	256	192	I
	LC4384V-5TN176I	384	3.3	5	Lead-free TQFP	176	128	I
	LC4384V-75TN176I	384	3.3	7.5	Lead-free TQFP	176	128	I
LC4384V-10TN176I	384	3.3	10	Lead-free TQFP	176	128	I	
LC4512V	LC4512V-5FTN256I	512	3.3	5	Lead-free ftBGA	256	208	I
	LC4512V-75FTN256I	512	3.3	7.5	Lead-free ftBGA	256	208	I
	LC4512V-10FTN256I	512	3.3	10	Lead-free ftBGA	256	208	I
	LC4512V-5FN256I <sup>1</sup>	512	3.3	5	Lead-free fpBGA	256	208	I
	LC4512V-75FN256I <sup>1</sup>	512	3.3	7.5	Lead-free fpBGA	256	208	I
	LC4512V-10FN256I <sup>1</sup>	512	3.3	10	Lead-free fpBGA	256	208	I
	LC4512V-5TN176I	512	3.3	5	Lead-free TQFP	176	128	I
	LC4512V-75TN176I	512	3.3	7.5	Lead-free TQFP	176	128	I
	LC4512V-10TN176I	512	3.3	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

## Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ( $0 \leq V_{IN} \leq 3.6V$ ).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided ( $V_{IN} - V_{CCO}$ ) $\leq$ 3.6V.
		Improved LC4064ZC t <sub>S</sub> to 2.5ns, t <sub>ST</sub> to 2.7ns and f <sub>MAX</sub> (Ext.) to 175MHz, LC4128ZC t <sub>CO</sub> to 3.5ns and f <sub>MAX</sub> (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs