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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 130°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032zc-75tn48e">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032zc-75tn48e</a>

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

### Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

### Initialization Control

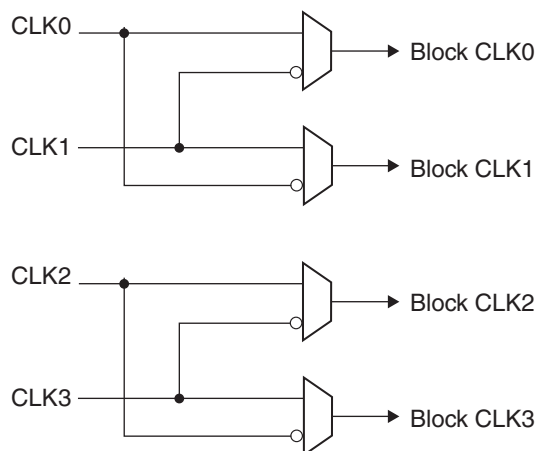
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

### GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

**Figure 6. GLB Clock Generator**



### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage ( $V_{CC}$ )	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage ( $V_{CCO}$ )	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied <sup>4, 5</sup>	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature ( $T_j$ ) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of ( $V_{IH}$  (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with  $V_{IN} > 3.6V$  is allowed.

### Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6 <sup>1, 2</sup>	1.9	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V	
	Supply Voltage for 3.3V Devices	3.0	3.6	V	
$T_j$	Junction Temperature (Commercial)	0	90	C	
	Junction Temperature (Industrial)	-40	105	C	
	Junction Temperature (Extended)	-40	130	C	

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

### Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

### Hot Socketing Characteristics<sup>1,2,3</sup>

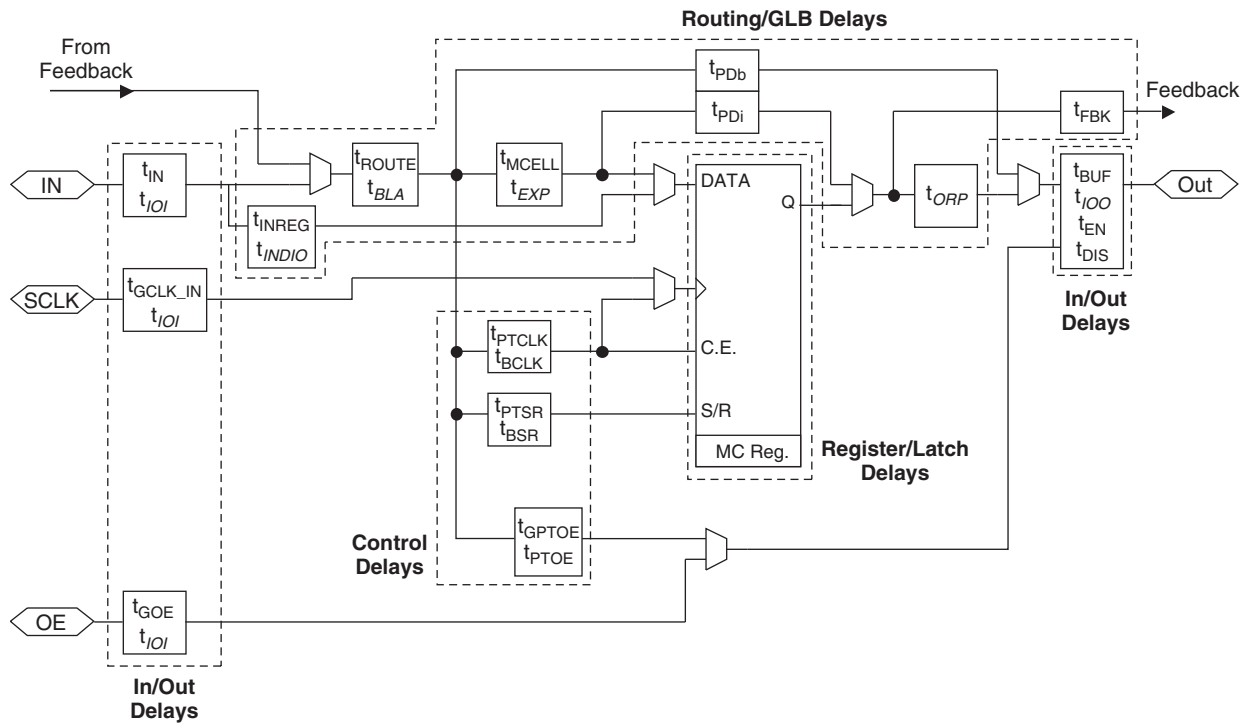
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DK}$	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$	—	±30	±200	µA

1. Insensitive to sequence of  $V_{CC}$  or  $V_{CCO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCO}$ , provided  $(V_{IN} - V_{CCO}) \leq 3.6V$ .
2.  $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}, I_{PD}$  or  $I_{BH}$ . Device defaults to pull-up until fuse circuitry is active.

## Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#).

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

**ispMACH 4000V/B/C Internal Timing Parameters (Cont.)****Over Recommended Operating Conditions**

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
$t_{PDLi}$	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
$t_{SRi}$	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
$t_{SRR}$	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
<b>Control Delays</b>										
$t_{BCLK}$	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
$t_{PTCLK}$	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
$t_{BSR}$	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
$t_{PTSR}$	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
$t_{GPtoE}$	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
$t_{PtoE}$	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

## ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>								
t <sub>IN</sub>	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t <sub>GOE</sub>	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t <sub>GCLK_IN</sub>	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t <sub>BUF</sub>	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t <sub>EN</sub>	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t <sub>DIS</sub>	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
<b>Routing/GLB Delays</b>								
t <sub>ROUTE</sub>	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t <sub>MCELL</sub>	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t <sub>INREG</sub>	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t <sub>FBK</sub>	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t <sub>PDb</sub>	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t <sub>PDi</sub>	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
<b>Register/Latch Delays</b>								
t <sub>S</sub>	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>S_PT</sub>	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t <sub>ST</sub>	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t <sub>ST_PT</sub>	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t <sub>H</sub>	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>HT</sub>	T-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t <sub>SIR</sub>	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t <sub>SIR_PT</sub>	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t <sub>HIR</sub>	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t <sub>HIR_PT</sub>	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t <sub>COi</sub>	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t <sub>CES</sub>	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t <sub>CEH</sub>	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t <sub>SL</sub>	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t <sub>SL_PT</sub>	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t <sub>HL</sub>	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t <sub>GOi</sub>	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t <sub>PDLi</sub>	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t <sub>SRI</sub>	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t <sub>SRR</sub>	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
<b>Control Delays</b>								
t <sub>BCLK</sub>	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t <sub>PTCLK</sub>	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t <sub>BSR</sub>	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t <sub>PTSR</sub>	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

**ispMACH 4000V/B/C/Z Power Supply and NC Connections<sup>1</sup>**

Signal	44-pin TQFP <sup>2</sup>	48-pin TQFP <sup>2</sup>	56-ball csBGA <sup>3</sup>	100-pin TQFP <sup>2</sup>	128-pin TQFP <sup>2</sup>
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	<b>4032Z:</b> A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:  
100-Pin TQFP**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0



**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

**ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	-
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	-
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	-
89	1	G6	G^5
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	-

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:  
132-Ball csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
D13	1	D10	D <sup>10</sup>	G4	G <sup>3</sup>	N6	N <sup>3</sup>
D14	1	D9	D <sup>9</sup>	G2	G <sup>2</sup>	N8	N <sup>4</sup>
D12	1	D8	D <sup>8</sup>	G1	G <sup>1</sup>	N10	N <sup>5</sup>
C14	1	I	-	G0	G <sup>0</sup>	N12	N <sup>6</sup>
C13	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B14	-	TDO	-	TDO	-	TDO	-
A14	-	VCC	-	VCC	-	VCC	-
A13	-	GND	-	GND	-	GND	-
B13	1	NC	-	H14	H <sup>11</sup>	O12	O <sup>6</sup>
A12	1	I	-	H13	H <sup>10</sup>	O10	O <sup>5</sup>
C12	1	D7	D <sup>7</sup>	H12	H <sup>9</sup>	O8	O <sup>4</sup>
B12	1	D6	D <sup>6</sup>	H10	H <sup>8</sup>	O6	O <sup>3</sup>
A11	1	D5	D <sup>5</sup>	H9	H <sup>7</sup>	O4	O <sup>2</sup>
C11	1	D4	D <sup>4</sup>	H8	H <sup>6</sup>	O2	O <sup>1</sup>
B11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B10	1	NC	-	H6	H <sup>5</sup>	P12	P <sup>6</sup>
C10	1	NC	-	H5	H <sup>4</sup>	P10	P <sup>5</sup>
B9	1	D3	D <sup>3</sup>	H4	H <sup>3</sup>	P8	P <sup>4</sup>
A9	1	D2	D <sup>2</sup>	H2	H <sup>2</sup>	P6	P <sup>3</sup>
C9	1	D1	D <sup>1</sup>	H1	H <sup>1</sup>	P4	P <sup>2</sup>
A8	1	D0/GOE1	D <sup>0</sup>	H0/GOE1	H <sup>0</sup>	P2/GOE1	P <sup>1</sup>
B8	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
C8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
B7	-	VCC	-	VCC	-	VCC	-
A7	0	NC <sup>1</sup>	-	NC <sup>1</sup>	-	I <sup>1</sup>	-
C7	0	A0/GOE0	A <sup>0</sup>	A0/GOE0	A <sup>0</sup>	A2/GOE0	A <sup>1</sup>
A6	0	A1	A <sup>1</sup>	A1	A <sup>1</sup>	A4	A <sup>2</sup>
B6	0	A2	A <sup>2</sup>	A2	A <sup>2</sup>	A6	A <sup>3</sup>
C6	0	A3	A <sup>3</sup>	A4	A <sup>3</sup>	A8	A <sup>4</sup>
B5	0	NC	-	A5	A <sup>4</sup>	A10	A <sup>5</sup>
A5	0	NC	-	A6	A <sup>5</sup>	A12	A <sup>6</sup>
C5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
A4	0	NC	-	A8	A <sup>6</sup>	B2	B <sup>1</sup>
C4	0	A4	A <sup>4</sup>	A9	A <sup>7</sup>	B4	B <sup>2</sup>
A3	0	A5	A <sup>5</sup>	A10	A <sup>8</sup>	B6	B <sup>3</sup>
B3	0	A6	A <sup>6</sup>	A12	A <sup>9</sup>	B8	B <sup>4</sup>
A2	0	A7	A <sup>7</sup>	A13	A <sup>10</sup>	B10	B <sup>5</sup>
A1	0	NC	-	A14	A <sup>11</sup>	B12	B <sup>6</sup>

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

**ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP**

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
4	0	B0	B^0	C12	C^6
5	0	B1	B^1	C10	C^5
6	0	B2	B^2	C8	C^4
7	0	B4	B^3	C6	C^3
8	0	B5	B^4	C4	C^2
9	0	B6	B^5	C2	C^1
10	0	GND (Bank 0)	-	GND (Bank 0)	-
11	0	B8	B^6	D14	D^7
12	0	B9	B^7	D12	D^6
13	0	B10	B^8	D10	D^5
14	0	B12	B^9	D8	D^4
15	0	B13	B^10	D6	D^3
16	0	B14	B^11	D4	D^2
17	-	NC <sup>2</sup>	-	I <sup>2</sup>	-
18	0	GND (Bank 0) <sup>1</sup>	-	NC <sup>1</sup>	-
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
20	0	NC <sup>2</sup>	-	I <sup>2</sup>	-
21	0	C14	C^11	E2	E^1
22	0	C13	C^10	E4	E^2
23	0	C12	C^9	E6	E^3
24	0	C10	C^8	E8	E^4
25	0	C9	C^7	E10	E^5
26	0	C8	C^6	E12	E^6
27	0	GND (Bank 0)	-	GND (Bank 0)	-
28	0	C6	C^5	F2	F^1
29	0	C5	C^4	F4	F^2
30	0	C4	C^3	F6	F^3
31	0	C2	C^2	F8	F^4
32	0	C1	C^1	F10	F^5
33	0	C0	C^0	F12	F^6
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
35	-	TCK	-	TCK	-
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	0	NC <sup>2</sup>	-	I <sup>2</sup>	-
39	0	D14	D^11	G12	G^6
40	0	D13	D^10	G10	G^5
41	0	D12	D^9	G8	G^4
42	0	D10	D^8	G6	G^3

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D <sup>2</sup>	E4	E <sup>2</sup>	G4	G <sup>2</sup>
20	0	D2	D <sup>1</sup>	E2	E <sup>1</sup>	G2	G <sup>1</sup>
21	0	D0	D <sup>0</sup>	E0	E <sup>0</sup>	G0	G <sup>0</sup>
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E <sup>0</sup>	H0	H <sup>0</sup>	J0	J <sup>0</sup>
24	0	E2	E <sup>1</sup>	H2	H <sup>1</sup>	J2	J <sup>1</sup>
25	0	E4	E <sup>2</sup>	H4	H <sup>2</sup>	J4	J <sup>2</sup>
26	0	E6	E <sup>3</sup>	H6	H <sup>3</sup>	J6	J <sup>3</sup>
27	0	E8	E <sup>4</sup>	H8	H <sup>4</sup>	J8	J <sup>4</sup>
28	0	E10	E <sup>5</sup>	H10	H <sup>5</sup>	J10	J <sup>5</sup>
29	0	E12	E <sup>6</sup>	H12	H <sup>6</sup>	J12	J <sup>6</sup>
30	0	E14	E <sup>7</sup>	H14	H <sup>7</sup>	J14	J <sup>7</sup>
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F <sup>0</sup>	J0	J <sup>0</sup>	N0	N <sup>0</sup>
33	0	F2	F <sup>1</sup>	J2	J <sup>1</sup>	N2	N <sup>1</sup>
34	0	F4	F <sup>2</sup>	J4	J <sup>2</sup>	N4	N <sup>2</sup>
35	0	F6	F <sup>3</sup>	J6	J <sup>3</sup>	N6	N <sup>3</sup>
36	0	F8	F <sup>4</sup>	J8	J <sup>4</sup>	N8	N <sup>4</sup>
37	0	F10	F <sup>5</sup>	J10	J <sup>5</sup>	N10	N <sup>5</sup>
38	0	F12	F <sup>6</sup>	J12	J <sup>6</sup>	N12	N <sup>6</sup>
39	0	F14	F <sup>7</sup>	J14	J <sup>7</sup>	N14	N <sup>7</sup>
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G <sup>7</sup>	K14	K <sup>7</sup>	O14	O <sup>7</sup>
48	0	G12	G <sup>6</sup>	K12	K <sup>6</sup>	O12	O <sup>6</sup>
49	0	G10	G <sup>5</sup>	K10	K <sup>5</sup>	O10	O <sup>5</sup>
50	0	G8	G <sup>4</sup>	K8	K <sup>4</sup>	O8	O <sup>4</sup>
51	0	G6	G <sup>3</sup>	K6	K <sup>3</sup>	O6	O <sup>3</sup>
52	0	G4	G <sup>2</sup>	K4	K <sup>2</sup>	O4	O <sup>2</sup>
53	0	G2	G <sup>1</sup>	K2	K <sup>1</sup>	O2	O <sup>1</sup>
54	0	G0	G <sup>0</sup>	K0	K <sup>0</sup>	O0	O <sup>0</sup>
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H <sup>7</sup>	L14	L <sup>7</sup>	P14	P <sup>7</sup>
58	0	H12	H <sup>6</sup>	L12	L <sup>6</sup>	P12	P <sup>6</sup>
59	0	H10	H <sup>5</sup>	L10	L <sup>5</sup>	P10	P <sup>5</sup>

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:  
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
60	0	H8	H <sup>4</sup>	L8	L <sup>4</sup>	P8	P <sup>4</sup>
61	0	H6	H <sup>3</sup>	L6	L <sup>3</sup>	P6	P <sup>3</sup>
62	0	H4	H <sup>2</sup>	L4	L <sup>2</sup>	P4	P <sup>2</sup>
63	0	H2	H <sup>1</sup>	L2	L <sup>1</sup>	P2	P <sup>1</sup>
64	0	H0	H <sup>0</sup>	L0	L <sup>0</sup>	P0	P <sup>0</sup>
65	-	GND	-	GND	-	GND	-
66	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
67	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
68	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
69	-	VCC	-	VCC	-	VCC	-
70	1	I0	I <sup>0</sup>	M0	M <sup>0</sup>	AX0	AX <sup>0</sup>
71	1	I2	I <sup>1</sup>	M2	M <sup>1</sup>	AX2	AX <sup>1</sup>
72	1	I4	I <sup>2</sup>	M4	M <sup>2</sup>	AX4	AX <sup>2</sup>
73	1	I6	I <sup>3</sup>	M6	M <sup>3</sup>	AX6	AX <sup>3</sup>
74	1	I8	I <sup>4</sup>	M8	M <sup>4</sup>	AX8	AX <sup>4</sup>
75	1	I10	I <sup>5</sup>	M10	M <sup>5</sup>	AX10	AX <sup>5</sup>
76	1	I12	I <sup>6</sup>	M12	M <sup>6</sup>	AX12	AX <sup>6</sup>
77	1	I14	I <sup>7</sup>	M14	M <sup>7</sup>	AX14	AX <sup>7</sup>
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
79	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
80	1	J0	J <sup>0</sup>	N0	N <sup>0</sup>	BX0	BX <sup>0</sup>
81	1	J2	J <sup>1</sup>	N2	N <sup>1</sup>	BX2	BX <sup>1</sup>
82	1	J4	J <sup>2</sup>	N4	N <sup>2</sup>	BX4	BX <sup>2</sup>
83	1	J6	J <sup>3</sup>	N6	N <sup>3</sup>	BX6	BX <sup>3</sup>
84	1	J8	J <sup>4</sup>	N8	N <sup>4</sup>	BX8	BX <sup>4</sup>
85	1	J10	J <sup>5</sup>	N10	N <sup>5</sup>	BX10	BX <sup>5</sup>
86	1	J12	J <sup>6</sup>	N12	N <sup>6</sup>	BX12	BX <sup>6</sup>
87	1	J14	J <sup>7</sup>	N14	N <sup>7</sup>	BX14	BX <sup>7</sup>
88	-	VCC	-	VCC	-	VCC	-
89	-	NC	-	NC	-	NC	-
90	-	GND	-	GND	-	GND	-
91	-	TMS	-	TMS	-	TMS	-
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
93	1	K14	K <sup>7</sup>	O14	O <sup>7</sup>	CX14	CX <sup>7</sup>
94	1	K12	K <sup>6</sup>	O12	O <sup>6</sup>	CX12	CX <sup>6</sup>
95	1	K10	K <sup>5</sup>	O10	O <sup>5</sup>	CX10	CX <sup>5</sup>
96	1	K8	K <sup>4</sup>	O8	O <sup>4</sup>	CX8	CX <sup>4</sup>
97	1	K6	K <sup>3</sup>	O6	O <sup>3</sup>	CX6	CX <sup>3</sup>
98	1	K4	K <sup>2</sup>	O4	O <sup>2</sup>	CX4	CX <sup>2</sup>
99	1	K2	K <sup>1</sup>	O2	O <sup>1</sup>	CX2	CX <sup>1</sup>
100	1	K0	K <sup>0</sup>	O0	O <sup>0</sup>	CX0	CX <sup>0</sup>

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
-	-	-	-	-	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
C3	-	TDI	-	TDI	-	TDI	-	TDI	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B1	0	C14	C^7	C14	C^9	C14	C^7	C14	C^7
F5	0	C12	C^6	C12	C^8	C12	C^6	C12	C^6
D3	0	C10	C^5	C10	C^7	C10	C^5	C10	C^5
C1	0	C8	C^4	C9	C^6	C8	C^4	C8	C^4
C2	0	C6	C^3	C8	C^5	C6	C^3	C6	C^3
E3	0	C4	C^2	C6	C^4	C4	C^2	C4	C^2
D2	0	C2	C^1	C4	C^3	C2	C^1	C2	C^1
F6	0	C0	C^0	C2	C^2	C0	C^0	C0	C^0
D1	0	NC	-	C1	C^1	F6	F^3	H0	H^0
E2	0	NC	-	C0	C^0	F4	F^2	H4	H^1
E4	0	NC	-	NC	-	D6	D^3	F4	F^2
G5	0	NC	-	NC	-	D4	D^2	F6	F^3
E1	0	NC	-	NC	-	NC	-	F8	F^4
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
F2	0	NC	-	NC	-	NC	-	F10	F^5
F1	0	NC	-	NC	-	D2	D^1	F12	F^6
G1	0	NC	-	NC	-	D0	D^0	F14	F^7
G6	0	NC	-	D14	D^9	F2	F^1	H8	H^2
G4	0	NC	-	D12	D^8	F0	F^0	H12	H^3
H6	0	D14	D^7	D10	D^7	E14	E^7	G14	G^7
G3	0	D12	D^6	D9	D^6	E12	E^6	G12	G^6
H5	0	D10	D^5	D8	D^5	E10	E^5	G10	G^5
G2	0	D8	D^4	D6	D^4	E8	E^4	G8	G^4
H1	0	D6	D^3	D4	D^3	E6	E^3	G6	G^3
H2	0	D4	D^2	D2	D^2	E4	E^2	G4	G^2
H3	0	D2	D^1	D1	D^1	E2	E^1	G2	G^1
H4	0	D0	D^0	D0	D^0	E0	E^0	G0	G^0
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
J4	0	E0	E^0	E0	E^0	H0	H^0	J0	J^0
J3	0	E2	E^1	E1	E^1	H2	H^1	J2	J^1
J2	0	E4	E^2	E2	E^2	H4	H^2	J4	J^2
J1	0	E6	E^3	E4	E^3	H6	H^3	J6	J^3
K1	0	E8	E^4	E6	E^4	H8	H^4	J8	J^4
J5	0	E10	E^5	E8	E^5	H10	H^5	J10	J^5
K2	0	E12	E^6	E9	E^6	H12	H^6	J12	J^6

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:  
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J^5	J10	J^7	N10	N^5	BX10	BX^5
P13	1	J12	J^6	J12	J^8	N12	N^6	BX12	BX^6
N13	1	J14	J^7	J14	J^9	N14	N^7	BX14	BX^7
M12	1	NC	-	NC	-	P4	P^2	FX0	FX^0
T15	1	NC	-	NC	-	P6	P^3	FX2	FX^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX^2
R16	1	NC	-	NC	-	P8	P^4	FX6	FX^3
N14	1	NC	-	NC	-	P10	P^5	FX8	FX^4
P15	1	K14	K^7	K14	K^9	O14	O^7	CX14	CX^7
L11	1	K12	K^6	K12	K^8	O12	O^6	CX12	CX^6
P16	1	K10	K^5	K10	K^7	O10	O^5	CX10	CX^5
K11	1	K8	K^4	K9	K^6	O8	O^4	CX8	CX^4
M14	1	K6	K^3	K8	K^5	O6	O^3	CX6	CX^3
K12	1	K4	K^2	K6	K^4	O4	O^2	CX4	CX^2
N15	1	K2	K^1	K4	K^3	O2	O^1	CX2	CX^1
N16	1	K0	K^0	K2	K^2	O0	O^0	CX0	CX^0
M15	1	NC	-	K1	K^1	BX6	BX^3	HX0	HX^0
M13	1	NC	-	K0	K^0	BX4	BX^2	HX4	HX^1
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX^5
L15	1	NC	-	NC	-	P12	P^6	FX12	FX^6
L16	1	NC	-	NC	-	P14	P^7	FX14	FX^7
J11	1	NC	-	L14	L^9	BX2	BX^1	HX8	HX^2
K15	1	NC	-	L12	L^8	BX0	BX^0	HX12	HX^3
J12	1	L14	L^7	L10	L^7	AX14	AX^7	GX14	GX^7
K13	1	L12	L^6	L9	L^6	AX12	AX^6	GX12	GX^6
K14	1	L10	L^5	L8	L^5	AX10	AX^5	GX10	GX^5
K16	1	L8	L^4	L6	L^4	AX8	AX^4	GX8	GX^4
J16	1	L6	L^3	L4	L^3	AX6	AX^3	GX6	GX^3
J15	1	L4	L^2	L2	L^2	AX4	AX^2	GX4	GX^2
H16	1	L2	L^1	L1	L^1	AX2	AX^1	GX2	GX^1
J13	1	L0	L^0	L0	L^0	AX0	AX^0	GX0	GX^0
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M^0	M0	M^0	DX0	DX^0	JX0	JX^0



## ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I <sup>1</sup>	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I <sup>1</sup>	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I <sup>1</sup>	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I <sup>1</sup>	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I <sup>1</sup>	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I <sup>1</sup>	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C

## ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC <sup>1</sup>	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC <sup>1</sup>	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC <sup>1</sup>	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC <sup>1</sup>	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC <sup>1</sup>	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC <sup>1</sup>	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
LC4256B-5T100C	256	2.5	5	TQFP	100	64	C	
LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C	
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C <sup>1</sup>	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C <sup>1</sup>	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C <sup>1</sup>	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C <sup>1</sup>	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C <sup>1</sup>	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C <sup>1</sup>	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

**Lead-Free Packaging****ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices**

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C	
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices**

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

## ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

## Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ( $0 \leq V_{IN} \leq 3.6V$ ).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided ( $V_{IN} - V_{CCO}$ ) $\leq$ 3.6V.
		Improved LC4064ZC t <sub>S</sub> to 2.5ns, t <sub>ST</sub> to 2.7ns and f <sub>MAX</sub> (Ext.) to 175MHz, LC4128ZC t <sub>CO</sub> to 3.5ns and f <sub>MAX</sub> (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs

**Revision History (Cont.)**

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated $I_{PU}$ (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 $\mu$ A to -200 $\mu$ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage ( $I_{IH}$ ) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to "LA" automotive data sheet under the "Broad Device Offering" bullet.
		Added footnote 1 to Part Number Description to reference the "LA" automotive data sheet.
		Changed device temperature references from 'Automotive' to "Extended Temperature" for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to $t_{CW}$ , $t_{GW}$ , $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to $t_{CW}$ , $t_{GW}$ , $t_{WIR}$ and $f_{MAX}$ parameters in ispMACH 4000V/B/C External Switching Characteristics table.