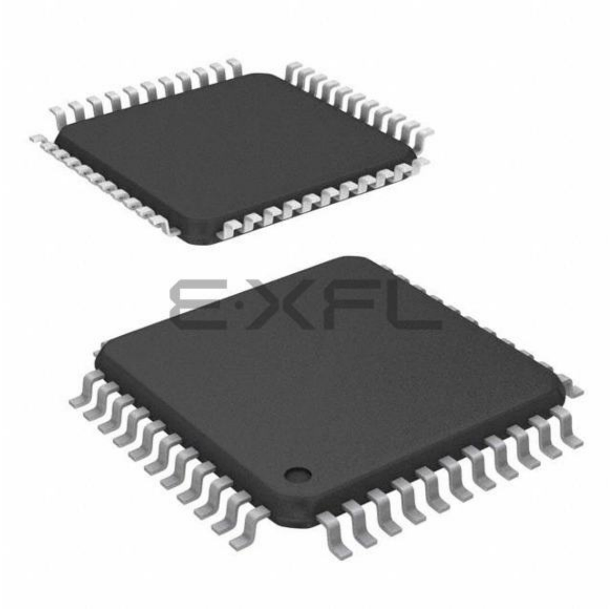


Welcome to E-XFL.COM

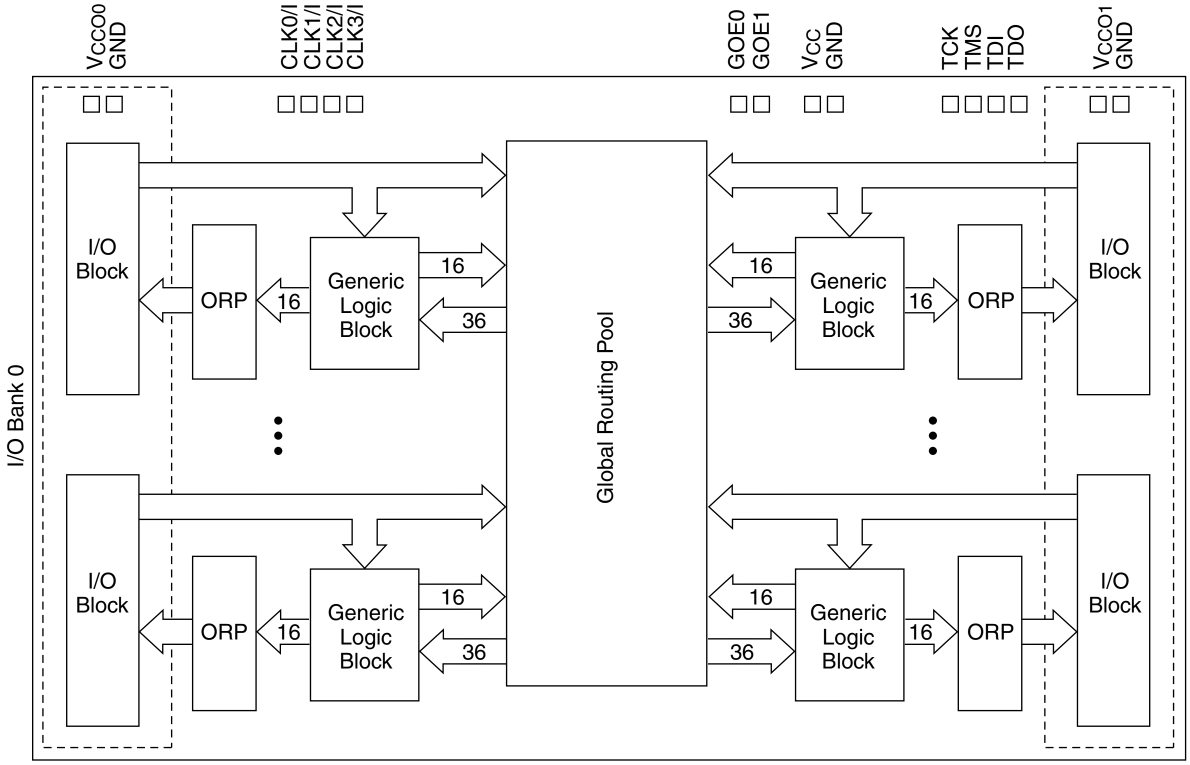
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	2.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	30
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064b-25tn44c

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

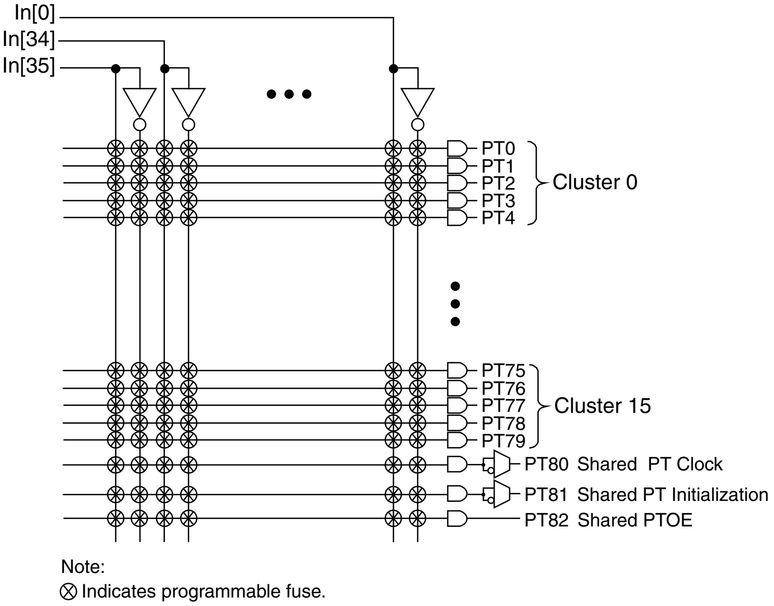
ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 3. AND Array



Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice

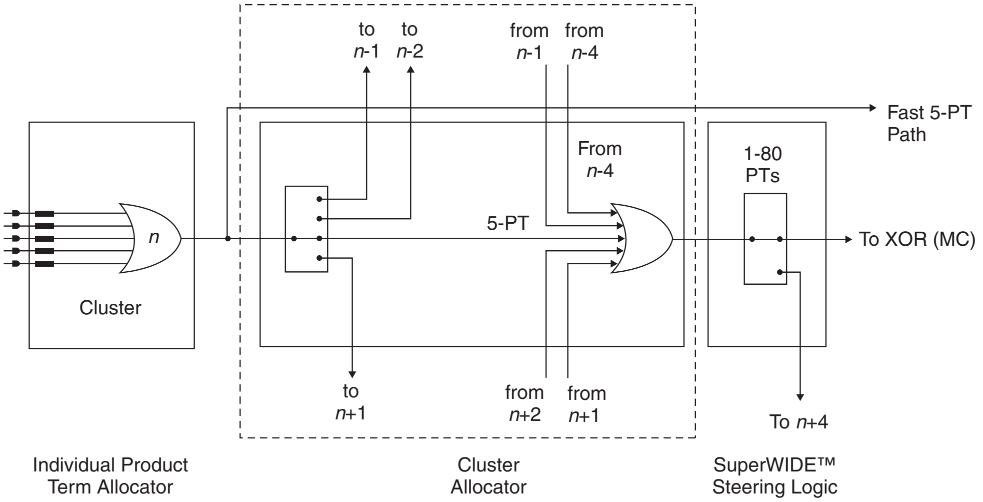
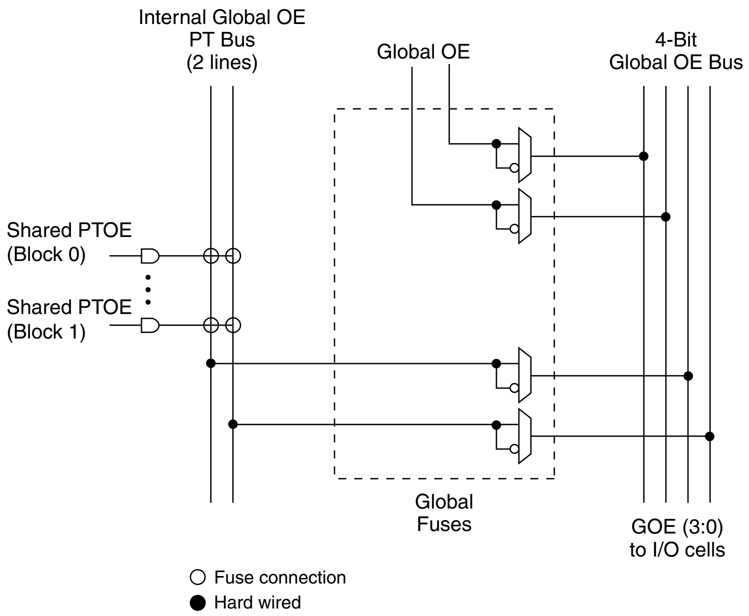


Figure 10. Global OE Generation for ispMACH 4032



Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C/Z (1.8V)	**ispMACH 4000B (2.5V)**	**ispMACH 4000V (3.3V)**
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95	V
		ispMACH 4000Z	1.7	1.9	V
		ispMACH 4000Z, Extended Functional Voltage Operation	1.6[1, 2]	1.9	V
	Supply Voltage for 2.5V Devices		2.3	2.7	V
	Supply Voltage for 3.3V Devices		3.0	3.6	V
T_j	Junction Temperature (Commercial)		0	90	C
	Junction Temperature (Industrial)		-40	105	C
	Junction Temperature (Extended)		-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

Supply Current, ispMACH 4000V/B/C

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032V/B/C						
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	11.8	—	mA
		Vcc = 2.5V	—	11.8	—	mA
		Vcc = 1.8V	—	1.8	—	mA
ICC^{4}	Standby Power Supply Current	Vcc = 3.3V	—	11.3	—	mA
		Vcc = 2.5V	—	11.3	—	mA
		Vcc = 1.8V	—	1.3	—	mA
ispMACH 4064V/B/C						
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
		Vcc = 2.5V	—	12	—	mA
		Vcc = 1.8V	—	2	—	mA
ICC^{5}	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
		Vcc = 2.5V	—	11.5	—	mA
		Vcc = 1.8V	—	1.5	—	mA
ispMACH 4128V/B/C						
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12	—	mA
		Vcc = 2.5V	—	12	—	mA
		Vcc = 1.8V	—	2	—	mA
ICC^{4}	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—	mA
		Vcc = 2.5V	—	11.5	—	mA
		Vcc = 1.8V	—	1.5	—	mA
ispMACH 4256V/B/C						
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12.5	—	mA
		Vcc = 2.5V	—	12.5	—	mA
		Vcc = 1.8V	—	2.5	—	mA
I_{CC}^{4}	Standby Power Supply Current	Vcc = 3.3V	—	12	—	mA
		Vcc = 2.5V	—	12	—	mA
		Vcc = 1.8V	—	2	—	mA
ispMACH 4384V/B/C						
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	13.5	—	mA
		Vcc = 2.5V	—	13.5	—	mA
		Vcc = 1.8V	—	3.5	—	mA
I_{CC}^{4}	Standby Power Supply Current	Vcc = 3.3V	—	12.5	—	mA
		Vcc = 2.5V	—	12.5	—	mA
		Vcc = 1.8V	—	2.5	—	mA
ispMACH 4512V/B/C						
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	14	—	mA
		Vcc = 2.5V	—	14	—	mA
		Vcc = 1.8V	—	4	—	mA

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{H}	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t_{GOE}	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t_{BUF}	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t_{EN}	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t_{DIS}	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t_{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
Register/Latch Delays								
t_{S}	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t_{H}	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t_{HT}	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t_{CES}	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t_{HL}	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.95	—	1.25	—	1.80	ns
t_{GOE}	Global OE Pin Delay	—	3.00	—	3.50	—	4.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.05	—	2.15	ns
t_{BUF}	Delay through Output Buffer	—	1.10	—	1.00	—	1.30	ns
t_{EN}	Output Enable Time	—	2.50	—	2.50	—	2.70	ns
t_{DIS}	Output Disable Time	—	2.50	—	2.50	—	2.70	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	2.25	—	2.05	—	2.50	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.65	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.35	—	0.05	—	0.05	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.20	—	0.70	—	1.90	ns
t_{PDi}	Macrocell Propagation Delay	—	0.45	—	0.65	—	1.00	ns
Register/Latch Delays								
t_S	D-Register Setup Time (Global Clock)	1.00	—	1.10	—	1.35	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	2.10	—	1.90	—	2.45	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.20	—	1.30	—	1.55	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	2.30	—	2.10	—	2.75	—	ns
t_H	D-Register Hold Time	1.90	—	1.90	—	3.15	—	ns
t_{HT}	T-Resister Hold Time	1.90	—	1.90	—	3.15	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.30	—	1.10	—	0.75	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.30	—	1.50	—	1.95	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.00	—	1.00	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.75	—	1.15	—	1.05	ns
t_{CES}	Clock Enable Setup Time	2.00	—	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.00	—	1.00	—	1.65	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	2.10	—	1.90	—	2.15	—	ns
t_{HL}	Latch Hold Time	2.00	—	2.00	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.97	—	0.97	—	0.28	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.80	—	1.80	—	1.67	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.83	—	1.83	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	4.30	—	4.20	—	3.50	ns

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
D13	1	D10	D^10	G4	G^3	N6	N^3
D14	1	D9	D^9	G2	G^2	N8	N^4
D12	1	D8	D^8	G1	G^1	N10	N^5
C14	1	I	-	G0	G^0	N12	N^6
C13	1	NC	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B14	-	TDO	-	TDO	-	TDO	-
A14	-	VCC	-	VCC	-	VCC	-
A13	-	GND	-	GND	-	GND	-
B13	1	NC	-	H14	H^11	O12	O^6
A12	1	I	-	H13	H^10	O10	O^5
C12	1	D7	D^7	H12	H^9	O8	O^4
B12	1	D6	D^6	H10	H^8	O6	O^3
A11	1	D5	D^5	H9	H^7	O4	O^2
C11	1	D4	D^4	H8	H^6	O2	O^1
B11	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A10	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B10	1	NC	-	H6	H^5	P12	P^6
C10	1	NC	-	H5	H^4	P10	P^5
B9	1	D3	D^3	H4	H^3	P8	P^4
A9	1	D2	D^2	H2	H^2	P6	P^3
C9	1	D1	D^1	H1	H^1	P4	P^2
A8	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/GOE1	P^1
B8	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
C8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
B7	-	VCC	-	VCC	-	VCC	-
A7	0	NC[1]	-	NC[1]	-	I[1]	-
C7	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^1
A6	0	A1	A^1	A1	A^1	A4	A^2
B6	0	A2	A^2	A2	A^2	A6	A^3
C6	0	A3	A^3	A4	A^3	A8	A^4
B5	0	NC	-	A5	A^4	A10	A^5
A5	0	NC	-	A6	A^5	A12	A^6
C5	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
B4	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
A4	0	NC	-	A8	A^6	B2	B^1
C4	0	A4	A^4	A9	A^7	B4	B^2
A3	0	A5	A^5	A10	A^8	B6	B^3
B3	0	A6	A^6	A12	A^9	B8	B^4
A2	0	A7	A^7	A13	A^10	B10	B^5
A1	0	NC	-	A14	A^11	B12	B^6

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-
2	-	TDI	-	TDI	-
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
4	0	B0	B^0	C12	C^6
5	0	B1	B^1	C10	C^5
6	0	B2	B^2	C8	C^4
7	0	B4	B^3	C6	C^3
8	0	B5	B^4	C4	C^2
9	0	B6	B^5	C2	C^1
10	0	GND (Bank 0)	-	GND (Bank 0)	-
11	0	B8	B^6	D14	D^7
12	0	B9	B^7	D12	D^6
13	0	B10	B^8	D10	D^5
14	0	B12	B^9	D8	D^4
15	0	B13	B^10	D6	D^3
16	0	B14	B^11	D4	D^2
17	-	NC[2]	-	I[2]	-
18	0	GND (Bank 0)[1]	-	NC[1]	-
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
20	0	NC[2]	-	I[2]	-
21	0	C14	C^11	E2	E^1
22	0	C13	C^10	E4	E^2
23	0	C12	C^9	E6	E^3
24	0	C10	C^8	E8	E^4
25	0	C9	C^7	E10	E^5
26	0	C8	C^6	E12	E^6
27	0	GND (Bank 0)	-	GND (Bank 0)	-
28	0	C6	C^5	F2	F^1
29	0	C5	C^4	F4	F^2
30	0	C4	C^3	F6	F^3
31	0	C2	C^2	F8	F^4
32	0	C1	C^1	F10	F^5
33	0	C0	C^0	F12	F^6
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
35	-	TCK	-	TCK	-
36	-	VCC	-	VCC	-
37	-	GND	-	GND	-
38	0	NC[2]	-	I[2]	-
39	0	D14	D^11	G12	G^6
40	0	D13	D^10	G10	G^5
41	0	D12	D^9	G8	G^4
42	0	D10	D^8	G6	G^3

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
J6	0	E14	E^7	E10	E^7	H14	H^7	J14	J^7
K3	0	NC	-	E12	E^8	G0	G^0	I0	I^0
K4	0	NC	-	E14	E^9	G2	G^1	I4	I^1
L1	0	NC	-	NC	-	I14	I^7	K0	K^0
L2	0	NC	-	NC	-	I12	I^6	K2	K^1
M1	0	NC	-	NC	-	NC	-	K4	K^2
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
M2	0	NC	-	NC	-	NC	-	K6	K^3
N1	0	NC	-	NC	-	I10	I^5	K8	K^4
M3	0	NC	-	NC	-	I8	I^4	K10	K^5
M4	0	NC	-	F0	F^0	G4	G^2	I8	I^2
N2	0	NC	-	F1	F^1	G6	G^3	I12	I^3
K5	0	F0	F^0	F2	F^2	J0	J^0	N0	N^0
P1	0	F2	F^1	F4	F^3	J2	J^1	N2	N^1
K6	0	F4	F^2	F6	F^4	J4	J^2	N4	N^2
N3	0	F6	F^3	F8	F^5	J6	J^3	N6	N^3
L5	0	F8	F^4	F9	F^6	J8	J^4	N8	N^4
P2	0	F10	F^5	F10	F^7	J10	J^5	N10	N^5
L6	0	F12	F^6	F12	F^8	J12	J^6	N12	N^6
R1	0	F14	F^7	F14	F^9	J14	J^7	N14	N^7
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
P3	-	TCK	-	TCK	-	TCK	-	TCK	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
T2	0	NC	-	G14	G^9	I6	I^3	K12	K^6
M5	0	NC	-	G12	G^8	I4	I^2	K14	K^7
N4	0	G14	G^7	G10	G^7	K14	K^7	O14	O^7
T3	0	G12	G^6	G9	G^6	K12	K^6	O12	O^6
R3	0	G10	G^5	G8	G^5	K10	K^5	O10	O^5
M6	0	G8	G^4	G6	G^4	K8	K^4	O8	O^4
P4	0	G6	G^3	G4	G^3	K6	K^3	O6	O^3
L7	0	G4	G^2	G2	G^2	K4	K^2	O4	O^2
N5	0	G2	G^1	G1	G^1	K2	K^1	O2	O^1
M7	0	G0	G^0	G0	G^0	K0	K^0	O0	O^0
P5	0	NC	-	NC	-	G8	G^4	M0	M^0
R4	0	NC	-	NC	-	G10	G^5	M4	M^1
T4	0	NC	-	NC	-	NC	-	L0	L^0
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC[1]	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC[1]	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC[1]	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC[1]	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC[1]	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC[1]	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C[1]	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C[1]	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C[1]	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C[1]	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C[1]	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C[1]	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI[1]	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI[1]	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI[1]	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI[1]	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI[1]	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI[1]	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

Lead-Free Packaging

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI[1]	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI[1]	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI[1]	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI[1]	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI[1]	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI[1]	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I[1]	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I[1]	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I[1]	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I[1]	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I[1]	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I[1]	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150µA to -200µA.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.