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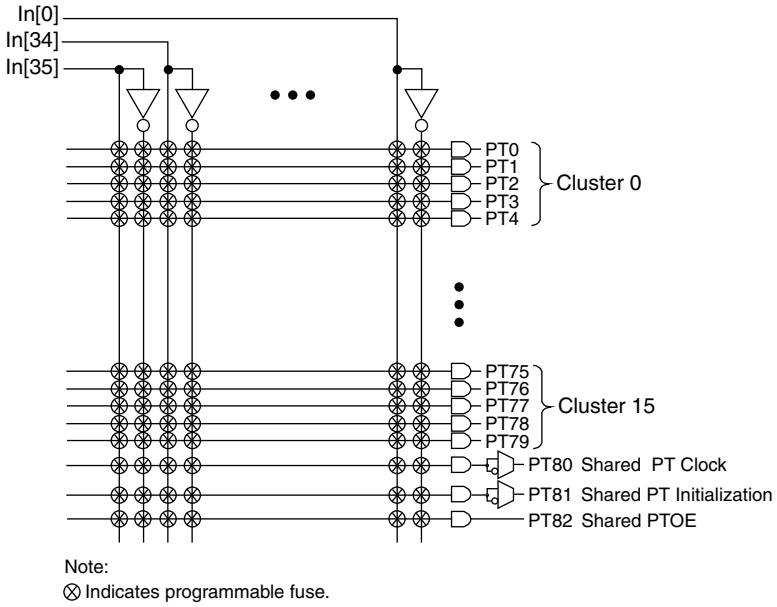
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064b-5t100i

Figure 3. AND Array



Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice

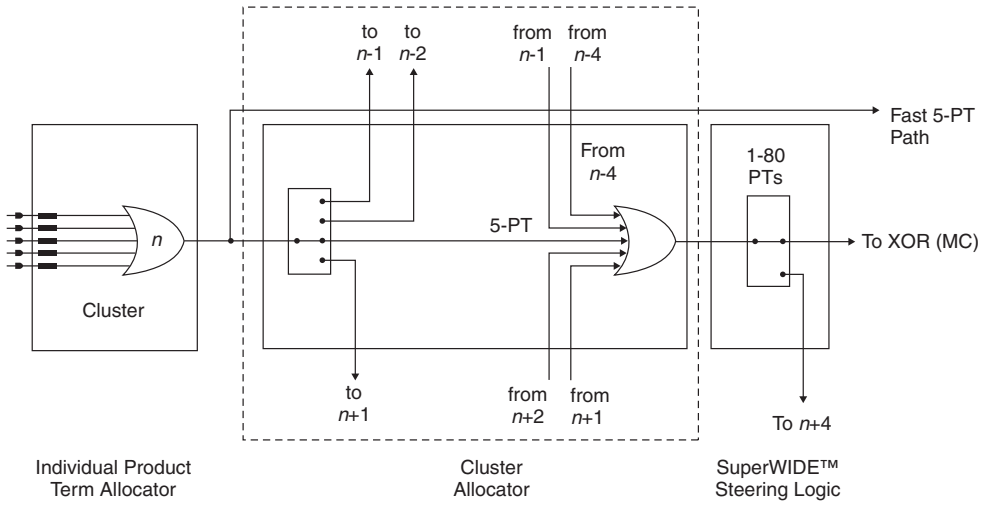


Table 5. Product Term Expansion Capability

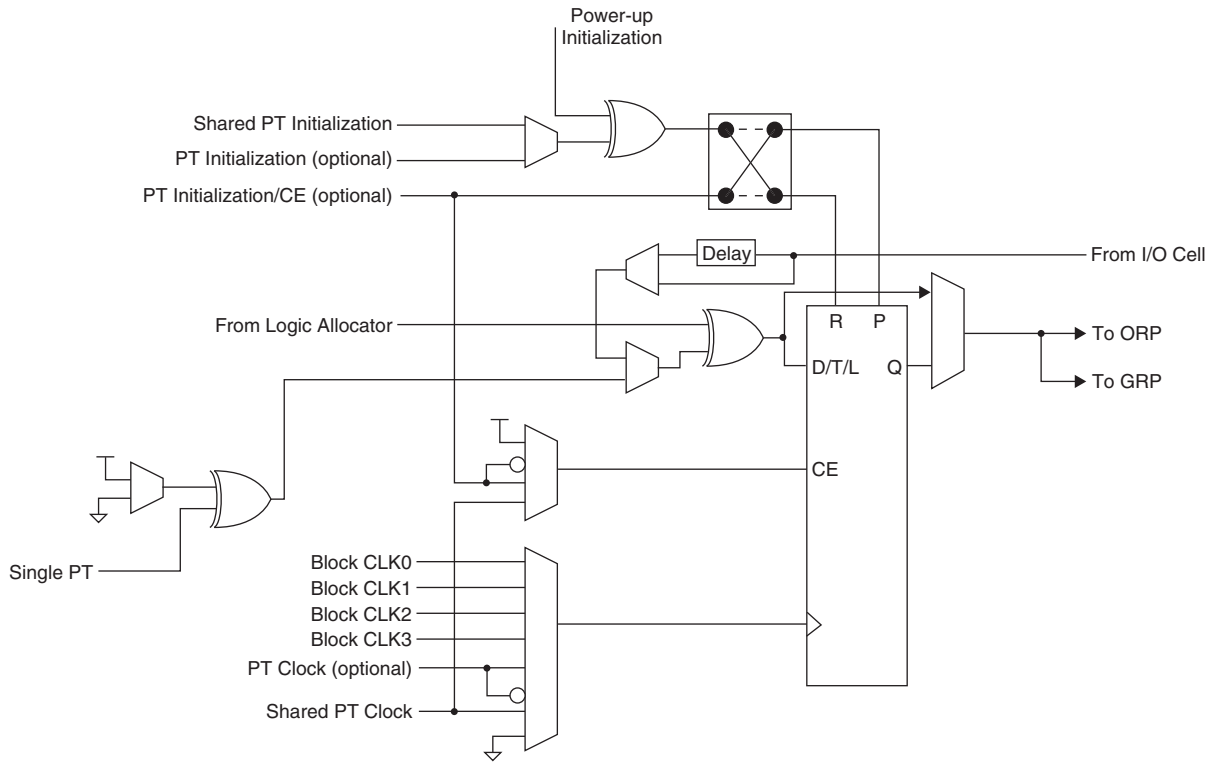
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 M4 M8 M12 M0	75
Chain-1	M1 M5 M9 M13 M1	80
Chain-2	M2 M6 M10 M14 M2	75
Chain-3	M3 M7 M11 M15 M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The ispMACH 4000 device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}[4]	Standby Power Supply Current	Vcc = 3.3V	—	13	—	mA
		Vcc = 2.5V	—	13	—	mA
		Vcc = 1.8V	—	3	—	mA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. T_A = 25°C

Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = 85°C	—	60	—	µA
		Vcc = 1.9V, T_A = 125°C	—	70	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 70°C	—	13	20	µA
		Vcc = 1.9V, T_A = 85°C	—	15	25	µA
		Vcc = 1.9V, T_A = 125°C	—	22	—	µA
ispMACH 4064ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = 85°C	—	92	—	µA
		Vcc = 1.9V, T_A = 125°C	—	109	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 70°C	—	15	25	µA
		Vcc = 1.9V, T_A = 85°C	—	18	35	µA
		Vcc = 1.9V, T_A = 125°C	—	37	—	µA
ispMACH 4128ZC						
ICC[1, 2, 3, 5]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = 85°C	—	195	—	µA
		Vcc = 1.9V, T_A = 125°C	—	212	—	µA
ICC[4, 5]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 70°C	—	16	35	µA
		Vcc = 1.9V, T_A = 85°C	—	19	50	µA
		Vcc = 1.9V, T_A = 125°C	—	42	—	µA

ispMACH 4000V/B/C External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	10.5	ns
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.4	—	4.5	—	6.0	ns
t_R	External reset pin to output delay	—	6.3	—	9.0	—	10.5	ns
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.0	—	10.5	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.0	—	10.3	—	12.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.0	—	7.0	—	8.0	ns
t_{CW}	Global clock width, high or low	2.2	—	2.8	—	4.0	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	2.8	—	4.0	—	ns
t_{WIR}	Input register clock width, high or low	2.2	—	2.8	—	4.0		ns
f_{MAX}[4]	Clock frequency with internal feedback	—	227	—	168	—	125	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	—	156	—	111	—	86	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

Timing v.3.2

ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t_S	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t_R	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t_{RW}	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t_{CW}	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f_{MAX} (Ext.)	clock frequency with external feedback, [1 / (t_S + t_{CO})]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t_S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_H	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.12	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.61	ns
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.33	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.83	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

ispMACH 4000Z Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.95	—	1.25	—	1.80	ns
t_{GOE}	Global OE Pin Delay	—	3.00	—	3.50	—	4.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.05	—	2.15	ns
t_{BUF}	Delay through Output Buffer	—	1.10	—	1.00	—	1.30	ns
t_{EN}	Output Enable Time	—	2.50	—	2.50	—	2.70	ns
t_{DIS}	Output Disable Time	—	2.50	—	2.50	—	2.70	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	2.25	—	2.05	—	2.50	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.65	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.35	—	0.05	—	0.05	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.20	—	0.70	—	1.90	ns
t_{PDi}	Macrocell Propagation Delay	—	0.45	—	0.65	—	1.00	ns
Register/Latch Delays								
t_{S}	D-Register Setup Time (Global Clock)	1.00	—	1.10	—	1.35	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	2.10	—	1.90	—	2.45	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.20	—	1.30	—	1.55	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	2.30	—	2.10	—	2.75	—	ns
t_{H}	D-Register Hold Time	1.90	—	1.90	—	3.15	—	ns
t_{HT}	T-Resister Hold Time	1.90	—	1.90	—	3.15	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.30	—	1.10	—	0.75	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.30	—	1.50	—	1.95	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.00	—	1.00	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.75	—	1.15	—	1.05	ns
t_{CES}	Clock Enable Setup Time	2.00	—	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.00	—	1.00	—	1.65	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	2.10	—	1.90	—	2.15	—	ns
t_{HL}	Latch Hold Time	2.00	—	2.00	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.97	—	0.97	—	0.28	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.80	—	1.80	—	1.67	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.55	—	1.55	—	1.25	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.83	—	1.83	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	4.30	—	4.20	—	3.50	ns

ispMACH 4000V/B/C Timing Adders[1]

Adder Type	Base Parameter	Description	-25		-27		-3		-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders											
t_{INDIO}	t_{INREG}	Input register delay	—	0.95	—	1.00	—	1.00	—	1.00	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	—	0.33	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	—	0.05	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.03	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters											
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters											
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.3.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

ispMACH 4000Z Timing Adders (Cont.)[1]

Adder Type	Base Parameter	Description	-45		-5		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t_{INDIO}	t_{INREG}	Input register delay	—	1.30	—	1.30	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.45	—	0.45	—	0.50	ns
t_{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.2

1. Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank.	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032	y: A-B
	ispMACH 4064	y: A-D
	ispMACH 4128	y: A-H
	ispMACH 4256	y: A-P
	ispMACH 4384	y: A-P, AX-HX
	ispMACH 4512	y: A-P, AX-PX

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

ispMACH 4000V/B/C ORP Reference Table

	4032V/B/C		4064V/B/C			4128V/B/C			4256V/B/C				4384V/B/C		4512V/B/C	
Number of I/Os	30[1]	32	30[2]	32	64	64	92[3]	96	64	96[4]	128	160	128	192	128	208
Number of GLBs	2	2	4	4	4	8	8	8	16	16	16	16	16	16	16	16
Number of I/Os / GLB	16	16	8	8	16	8	12	12	4	8	8	10	8	8	8	Mixture of 8 & 4[5]
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB		4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB	10 I/Os / GLB	8 I/Os / GLB		8 I/Os / GLB	8 I/Os / GLB 4 I/Os / GLB

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.
2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.
3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os
4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per
5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

ispMACH 4000Z ORP Reference Table

	4032Z	4064Z		4128Z		4256Z		
Number of I/Os	32	32	64	64	96	64	96[1]	128
Number of GLBs	2	4	4	8	8	16	16	16
Number of I/Os / GLB	16	8	16	8	12	4	8	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB	12 I/Os / GLB	4 I/Os / GLB	8 I/Os / GLB	8 I/Os / GLB

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	GND	-	GND	-	GND	-
2	-	TDI	-	TDI	-	TDI	-
3	0	A8	A^8	B0	B^0	C12	C^3
4	0	A9	A^9	B2	B^1	C10	C^2
5	0	A10	A^10	B4	B^2	C6	C^1
6	0	A11	A^11	B6	B^3	C2	C^0
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
8	0	A12	A^12	B8	B^4	D12	D^3
9	0	A13	A^13	B10	B^5	D10	D^2
10	0	A14	A^14	B12	B^6	D6	D^1
11	0	A15	A^15	B13	B^7	D4	D^0
12*	0	I	-	I	-	I	-
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
14	0	B15	B^15	C14	C^7	E4	E^0
15	0	B14	B^14	C12	C^6	E6	E^1
16	0	B13	B^13	C10	C^5	E10	E^2
17	0	B12	B^12	C8	C^4	E12	E^3
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
19	0	B11	B^11	C6	C^3	F2	F^0
20	0	B10	B^10	C5	C^2	F6	F^1
21	0	B9	B^9	C4	C^1	F10	F^2
22	0	B8	B^8	C2	C^0	F12	F^3
23*	0	I	-	I	-	I	-
24	-	TCK	-	TCK	-	TCK	-
25	-	VCC	-	VCC	-	VCC	-
26	-	GND	-	GND	-	GND	-
27*	0	I	-	I	-	I	-
28	0	B7	B^7	D13	D^7	G12	G^3
29	0	B6	B^6	D12	D^6	G10	G^2
30	0	B5	B^5	D10	D^5	G6	G^1
31	0	B4	B^4	D8	D^4	G2	G^0
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
34	0	B3	B^3	D6	D^3	H12	H^3
35	0	B2	B^2	D4	D^2	H10	H^2
36	0	B1	B^1	D2	D^1	H6	H^1
37	0	B0	B^0	D0	D^0	H2	H^0
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
40	-	VCC	-	VCC	-	VCC	-
41	1	C0	C^0	E0	E^0	I2	I^0

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	-
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^5
43	0	D5	D^4
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^6
61	1	E9	E^7

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D^7	G4	G^2
44	0	D8	D^6	G2	G^1
45	0	NC[2]	-	I[2]	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D^5	H12	H^6
49	0	D5	D^4	H10	H^5
50	0	D4	D^3	H8	H^4
51	0	D2	D^2	H6	H^3
52	0	D1	D^1	H4	H^2
53	0	D0	D^0	H2	H^1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E^0	I2	I^1
59	1	E1	E^1	I4	I^2
60	1	E2	E^2	I6	I^3
61	1	E4	E^3	I8	I^4
62	1	E5	E^4	I10	I^5
63	1	E6	E^5	I12	I^6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E^6	J2	J^1
67	1	E9	E^7	J4	J^2
68	1	E10	E^8	J6	J^3
69	1	E12	E^9	J8	J^4
70	1	E13	E^10	J10	J^5
71	1	E14	E^11	J12	J^6
72	1	NC[2]	-	I[2]	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F^0	K12	K^6
77	1	F1	F^1	K10	K^5
78	1	F2	F^2	K8	K^4
79	1	F4	F^3	K6	K^3
80	1	F5	F^4	K4	K^2
81	1	F6	F^5	K2	K^1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F^6	L14	L^7
84	1	F9	F^7	L12	L^6
85	1	F10	F^8	L10	L^5

ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D^2	E4	E^2	G4	G^2
20	0	D2	D^1	E2	E^1	G2	G^1
21	0	D0	D^0	E0	E^0	G0	G^0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E^0	H0	H^0	J0	J^0
24	0	E2	E^1	H2	H^1	J2	J^1
25	0	E4	E^2	H4	H^2	J4	J^2
26	0	E6	E^3	H6	H^3	J6	J^3
27	0	E8	E^4	H8	H^4	J8	J^4
28	0	E10	E^5	H10	H^5	J10	J^5
29	0	E12	E^6	H12	H^6	J12	J^6
30	0	E14	E^7	H14	H^7	J14	J^7
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F^0	J0	J^0	N0	N^0
33	0	F2	F^1	J2	J^1	N2	N^1
34	0	F4	F^2	J4	J^2	N4	N^2
35	0	F6	F^3	J6	J^3	N6	N^3
36	0	F8	F^4	J8	J^4	N8	N^4
37	0	F10	F^5	J10	J^5	N10	N^5
38	0	F12	F^6	J12	J^6	N12	N^6
39	0	F14	F^7	J14	J^7	N14	N^7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G^7	K14	K^7	O14	O^7
48	0	G12	G^6	K12	K^6	O12	O^6
49	0	G10	G^5	K10	K^5	O10	O^5
50	0	G8	G^4	K8	K^4	O8	O^4
51	0	G6	G^3	K6	K^3	O6	O^3
52	0	G4	G^2	K4	K^2	O4	O^2
53	0	G2	G^1	K2	K^1	O2	O^1
54	0	G0	G^0	K0	K^0	O0	O^0
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H^7	L14	L^7	P14	P^7
58	0	H12	H^6	L12	L^6	P12	P^6
59	0	H10	H^5	L10	L^5	P10	P^5

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
E7	0	NC	-	B1	B^1	F8	F^4	D12	D^3
A3	0	B0	B^0	B2	B^2	B0	B^0	B0	B^0
F7	0	B2	B^1	B4	B^3	B2	B^1	B2	B^1
B4	0	B4	B^2	B6	B^4	B4	B^2	B4	B^2
C5	0	B6	B^3	B8	B^5	B6	B^3	B6	B^3
A2	0	B8	B^4	B9	B^6	B8	B^4	B8	B^4
E6	0	B10	B^5	B10	B^7	B10	B^5	B10	B^5
B3	0	B12	B^6	B12	B^8	B12	B^6	B12	B^6
C4	0	B14	B^7	B14	B^9	B14	B^7	B14	B^7
D4	0	NC	-	NC	-	D10	D^5	F0	F^0
E5	0	NC	-	NC	-	D8	D^4	F2	F^1
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	-	-	-	-	GND	-	GND	-
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank 0)	-

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply and NC Connections table for VCC/ VCCO/GND pin definitions.

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B	LC4256B-3FT256AC	256	2.5	3	ftBGA	256	128	C
	LC4256B-5FT256AC	256	2.5	5	ftBGA	256	128	C
	LC4256B-75FT256AC	256	2.5	7.5	ftBGA	256	128	C
	LC4256B-3FT256BC	256	2.5	3	ftBGA	256	160	C
	LC4256B-5FT256BC	256	2.5	5	ftBGA	256	160	C
	LC4256B-75FT256BC	256	2.5	7.5	ftBGA	256	160	C
	LC4256B-3F256AC[1]	256	2.5	3	fpBGA	256	128	C
	LC4256B-5F256AC[1]	256	2.5	5	fpBGA	256	128	C
	LC4256B-75F256AC[1]	256	2.5	7.5	fpBGA	256	128	C
	LC4256B-3F256BC[1]	256	2.5	3	fpBGA	256	160	C
	LC4256B-5F256BC[1]	256	2.5	5	fpBGA	256	160	C
	LC4256B-75F256BC[1]	256	2.5	7.5	fpBGA	256	160	C
	LC4256B-3T176C	256	2.5	3	TQFP	176	128	C
	LC4256B-5T176C	256	2.5	5	TQFP	176	128	C
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
	LC4256B-3T100C	256	2.5	3	TQFP	100	64	C
	LC4256B-5T100C	256	2.5	5	TQFP	100	64	C
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4384B	LC4384B-35FT256C	384	2.5	3.5	ftBGA	256	192	C
	LC4384B-5FT256C	384	2.5	5	ftBGA	256	192	C
	LC4384B-75FT256C	384	2.5	7.5	ftBGA	256	192	C
	LC4384B-35F256C[1]	384	2.5	3.5	fpBGA	256	192	C
	LC4384B-5F256C[1]	384	2.5	5	fpBGA	256	192	C
	LC4384B-75F256C[1]	384	2.5	7.5	fpBGA	256	192	C
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128	C
	LC4384B-5T176C	384	2.5	5	TQFP	176	128	C
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128	C
LC4512B	LC4512B-35FT256C	512	2.5	3.5	ftBGA	256	208	C
	LC4512B-5FT256C	512	2.5	5	ftBGA	256	208	C
	LC4512B-75FT256C	512	2.5	7.5	ftBGA	256	208	C
	LC4512B-35F256C[1]	512	2.5	3.5	fpBGA	256	208	C
	LC4512B-5F256C[1]	512	2.5	5	fpBGA	256	208	C
	LC4512B-75F256C[1]	512	2.5	7.5	fpBGA	256	208	C
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
	LC4512B-5T176C	512	2.5	5	TQFP	176	128	C
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-25TN48C	32	3.3	2.5	Lead-free TQFP	48	32	C
	LC4032V-5TN48C	32	3.3	5	Lead-free TQFP	48	32	C
	LC4032V-75TN48C	32	3.3	7.5	Lead-free TQFP	48	32	C
	LC4032V-25TN44C	32	3.3	2.5	Lead-free TQFP	44	30	C
	LC4032V-5TN44C	32	3.3	5	Lead-free TQFP	44	30	C
	LC4032V-75TN44C	32	3.3	7.5	Lead-free TQFP	44	30	C
LC4064V	LC4064V-25TN100C	64	3.3	2.5	Lead-free TQFP	100	64	C
	LC4064V-5TN100C	64	3.3	5	Lead-free TQFP	100	64	C
	LC4064V-75TN100C	64	3.3	7.5	Lead-free TQFP	100	64	C
	LC4064V-25TN48C	64	3.3	2.5	Lead-free TQFP	48	32	C
	LC4064V-5TN48C	64	3.3	5	Lead-free TQFP	48	32	C
	LC4064V-75TN48C	64	3.3	7.5	Lead-free TQFP	48	32	C
	LC4064V-25TN44C	64	3.3	2.5	Lead-free TQFP	44	30	C
	LC4064V-5TN44C	64	3.3	5	Lead-free TQFP	44	30	C
	LC4064V-75TN44C	64	3.3	7.5	Lead-free TQFP	44	30	C
LC4128V	LC4128V-27TN144C	128	3.3	2.7	Lead-free TQFP	144	96	C
	LC4128V-5TN144C	128	3.3	5	Lead-free TQFP	144	96	C
	LC4128V-75TN144C	128	3.3	7.5	Lead-free TQFP	144	96	C
	LC4128V-27TN128C	128	3.3	2.7	Lead-free TQFP	128	92	C
	LC4128V-5TN128C	128	3.3	5	Lead-free TQFP	128	92	C
	LC4128V-75TN128C	128	3.3	7.5	Lead-free TQFP	128	92	C
	LC4128V-27TN100C	128	3.3	2.7	Lead-free TQFP	100	64	C
	LC4128V-5TN100C	128	3.3	5	Lead-free TQFP	100	64	C
	LC4128V-75TN100C	128	3.3	7.5	Lead-free TQFP	100	64	C

ispMACH 4000V (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-5TN48I	32	3.3	5	Lead-free TQFP	48	32	I
	LC4032V-75TN48I	32	3.3	7.5	Lead-free TQFP	48	32	I
	LC4032V-10TN48I	32	3.3	10	Lead-free TQFP	48	32	I
	LC4032V-5TN44I	32	3.3	5	Lead-free TQFP	44	30	I
	LC4032V-75TN44I	32	3.3	7.5	Lead-free TQFP	44	30	I
	LC4032V-10TN44I	32	3.3	10	Lead-free TQFP	44	30	I
LC4064V	LC4064V-5TN100I	64	3.3	5	Lead-free TQFP	100	64	I
	LC4064V-75TN100I	64	3.3	7.5	Lead-free TQFP	100	64	I
	LC4064V-10TN100I	64	3.3	10	Lead-free TQFP	100	64	I
	LC4064V-5TN48I	64	3.3	5	Lead-free TQFP	48	32	I
	LC4064V-75TN48I	64	3.3	7.5	Lead-free TQFP	48	32	I
	LC4064V-10TN48I	64	3.3	10	Lead-free TQFP	48	32	I
	LC4064V-5TN44I	64	3.3	5	Lead-free TQFP	44	30	I
	LC4064V-75TN44I	64	3.3	7.5	Lead-free TQFP	44	30	I
	LC4064V-10TN44I	64	3.3	10	Lead-free TQFP	44	30	I
LC4128V	LC4128V-5TN144I	128	3.3	5	Lead-free TQFP	144	96	I
	LC4128V-75TN144I	128	3.3	7.5	Lead-free TQFP	144	96	I
	LC4128V-10TN144I	128	3.3	10	Lead-free TQFP	144	96	I
	LC4128V-5TN128I	128	3.3	5	Lead-free TQFP	128	92	I
	LC4128V-75TN128I	128	3.3	7.5	Lead-free TQFP	128	92	I
	LC4128V-10TN128I	128	3.3	10	Lead-free TQFP	128	92	I
	LC4128V-5TN100I	128	3.3	5	Lead-free TQFP	100	64	I
	LC4128V-75TN100I	128	3.3	7.5	Lead-free TQFP	100	64	I
	LC4128V-10TN100I	128	3.3	10	Lead-free TQFP	100	64	I