# Lattice Semiconductor Corporation - LC4064C-5TN48I Datasheet

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5 ns |
| Voltage Supply - Internal | 1.65V ~ 1.95V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | - |
| Number of I/O | 32 |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064c-5tn48i |

*Table 2. ispMACH 4000Z Family Selection Guide*

| | ispMACH 4032ZC | ispMACH 4064ZC | ispMACH 4128ZC | ispMACH 4256ZC |
|---|---|---|---|---|
| Macrocells | 32 | 64 | 128 | 256 |
| I/O + Dedicated Inputs | 32+4/32+4 | 32+4/32+12/ 64+10/64+10 | 64+10/96+4 | 64+10/96+6/ 128+4 |
| $t_{PD}$ (ns) | 3.5 | 3.7 | 4.2 | 4.5 |
| $t_S$ (ns) | 2.2 | 2.5 | 2.7 | 2.9 |
| $t_{CO}$ (ns) | 3.0 | 3.2 | 3.5 | 3.8 |
| $f_{MAX}$ (MHz) | 267 | 250 | 220 | 200 |
| Supply Voltage (V) | 1.8 | 1.8 | 1.8 | 1.8 |
| Max. Standby Icc (µA) | 20 | 25 | 35 | 55 |
| Pins/Package | 48 TQFP<br>56 csBGA | 48 TQFP<br>56 csBGA<br>100 TQFP<br>132 csBGA | 100 TQFP<br>132csBGA | 100 TQFP<br>132 csBGA<br>176 TQFP |

## ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA) and Fine Pitch Thin BGA (ftBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2.5V (4000B) and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 3.3V/2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to $V_{CC}$ (logic core).

## Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

## Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

## Initialization Control

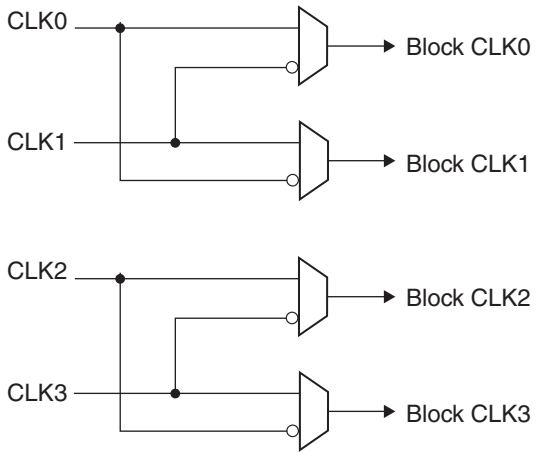
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the $V_{CC}$ rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

## GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

***Figure 6. GLB Clock Generator***



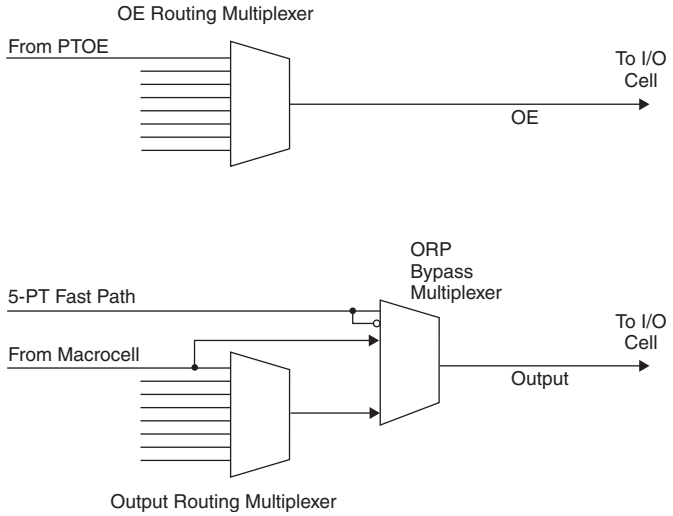
## Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

***Figure 7. ORP Slice***



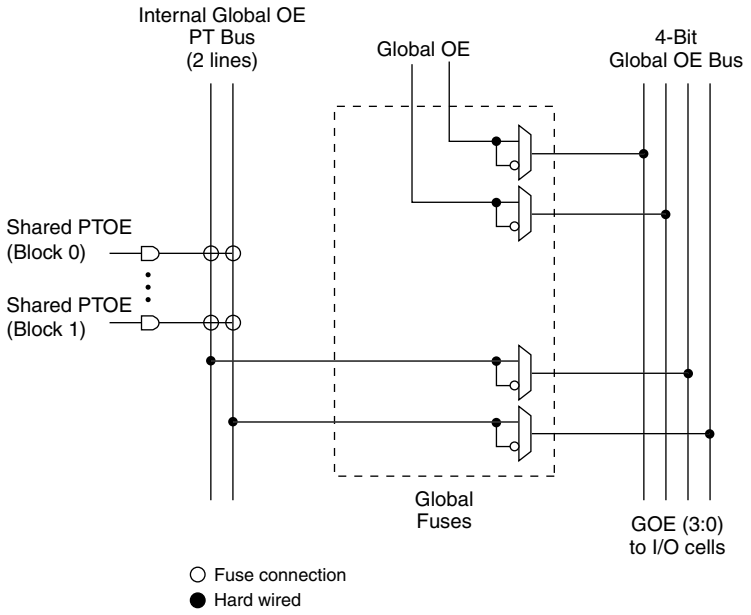

## Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

***Table 6. ORP Combinations for I/O Blocks with 8 I/Os***

| I/O Cell | Available Macrocells |
|---|---|
| I/O 0 | M0, M1, M2, M3, M4, M5, M6, M7 |
| I/O 1 | M2, M3, M4, M5, M6, M7, M8, M9 |
| I/O 2 | M4, M5, M6, M7, M8, M9, M10, M11 |
| I/O 3 | M6, M7, M8, M9, M10, M11, M12, M13 |
| I/O 4 | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O 5 | M10, M11, M12, M13, M14, M15, M0, M1 |
| I/O 6 | M12, M13, M14, M15, M0, M1, M2, M3 |
| I/O 7 | M14, M15, M0, M1, M2, M3, M4, M5 |

***Figure 10. Global OE Generation for ispMACH 4032***




## Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced $E^2$ low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

## IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

## I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

## IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

## User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in $E^2$CMOS memory. The ispMACH 4000 device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

## Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

## Density Migration

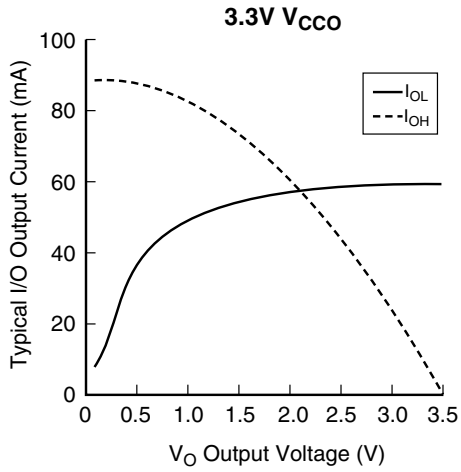
The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

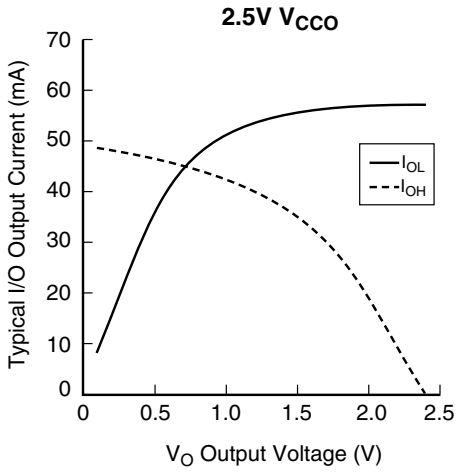
# Supply Current, ispMACH 4000Z (Cont.)

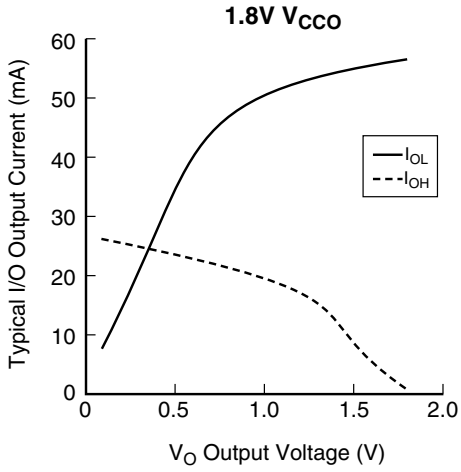
**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ispMACH 4256ZC** | | | | | | |
| ICC[1, 2, 3, 5] | Operating Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 341 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 70°C | — | 361 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 85°C | — | 372 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 125°C | — | 468 | — | µA |
| ICC[4, 5] | Standby Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 13 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 70°C | — | 32 | 55 | µA |
| | | Vcc = 1.9V, $T_A$ = 85°C | — | 43 | 90 | µA |
| | | Vcc = 1.9V, $T_A$ = 125°C | — | 135 | — | µA |

1. $T_A$ = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. $I_{CC}$ varies with specific device configuration and operating frequency.
4. $V_{CCO}$ = 3.6V, $V_{IN}$ = 0V or $V_{CCO,}$ bus maintenance turned off. $V_{IN}$ above $V_{CCO}$ will add transient current above the specified standby $I_{CC}$.
5. Includes $V_{CCO}$ current without output loading.


3.3V $V_{CCO}$
Typical I/O Output Current (mA)
100
80
60
40
20
0
0 0.5 1.0 1.5 2.0 2.5 3.0 3.5
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$


2.5V $V_{CCO}$
Typical I/O Output Current (mA)
70
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0 2.5
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$


1.8V $V_{CCO}$
Typical I/O Output Current (mA)
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0
$V_O$ Output Voltage (V)
$I_{OL}$
$I_{OH}$

# ispMACH 4000Z External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2, 3] | -35 | | -37 | | -42 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 5-PT bypass combinatorial propagation delay | — | 3.5 | — | 3.7 | — | 4.2 | ns |
| $t_{PD\_MC}$ | 20-PT combinatorial propagation delay through macrocell | — | 4.4 | — | 4.7 | — | 5.7 | ns |
| $t_S$ | GLB register setup time before clock | 2.2 | — | 2.5 | — | 2.7 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 2.4 | — | 2.7 | — | 2.9 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.0 | — | 1.1 | — | 1.3 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.0 | — | 2.1 | — | 2.6 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.0 | — | 1.0 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.0 | — | 3.2 | — | 3.5 | ns |
| $t_R$ | External reset pin to output delay | — | 5.0 | — | 6.0 | — | 7.3 | ns |
| $t_{RW}$ | External reset pulse duration | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 7.0 | — | 8.0 | — | 8.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 6.5 | — | 7.0 | — | 8.0 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 4.5 | — | 4.5 | — | 4.8 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | ns |
| $f_{MAX}$[4] | Clock frequency with internal feedback | — | 267 | — | 250 | — | 220 | MHz |
| $f_{MAX}$ (Ext.) | clock frequency with external feedback, $[1 / (t_S + t_{CO})]$ | — | 192 | — | 175 | — | 161 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

# ispMACH 4000V/B/C Internal Timing Parameters

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -75 | | -10 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 0.95 | — | 1.50 | — | 2.00 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 4.04 | — | 6.04 | — | 7.04 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 1.83 | — | 2.28 | — | 3.28 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 1.00 | — | 1.50 | — | 1.50 | ns |
| $t_{EN}$ | Output Enable Time | — | 0.96 | — | 0.96 | — | 0.96 | ns |
| $t_{DIS}$ | Output Disable Time | — | 0.96 | — | 0.96 | — | 0.96 | ns |
| **Routing/GLB Delays** | | | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 1.51 | — | 2.26 | — | 3.26 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 1.05 | — | 1.45 | — | 1.95 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 0.56 | — | 0.96 | — | 1.46 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.00 | — | 0.00 | — | 0.00 | ns |
| $t_{PDb}$ | 5-PT Bypass Propagation Delay | — | 1.54 | — | 2.24 | — | 3.24 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.94 | — | 1.24 | — | 1.74 | ns |
| **Register/Latch Delays** | | | | | | | | |
| $t_{S}$ | D-Register Setup Time (Global Clock) | 1.32 | — | 1.57 | — | 1.57 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 1.32 | — | 1.32 | — | 1.32 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.52 | — | 1.77 | — | 1.77 | — | ns |
| $t_{ST\_PT}$ | T-Register Setup Time (Product Term Clock) | 1.32 | — | 1.32 | — | 1.32 | — | ns |
| $t_{H}$ | D-Register Hold Time | 1.68 | — | 2.93 | — | 3.93 | — | ns |
| $t_{HT}$ | T-Register Hold Time | 1.68 | — | 2.93 | — | 3.93 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 1.52 | — | 1.57 | — | 1.57 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 0.68 | — | 1.18 | — | 1.18 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 0.68 | — | 1.18 | — | 1.18 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.52 | — | 0.67 | — | 1.17 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 2.25 | — | 2.25 | — | 2.25 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 1.88 | — | 1.88 | — | 1.88 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 1.32 | — | 1.57 | — | 1.57 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 1.32 | — | 1.32 | — | 1.32 | — | ns |
| $t_{HL}$ | Latch Hold Time | 1.17 | — | 1.17 | — | 1.17 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.33 | — | 0.33 | — | 0.33 | ns |
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | 0.28 | — | 0.28 | — | 0.28 | — | ns |
| $t_{SRR}$ | Asynchronous Reset or Set Recovery Time | 1.67 | — | 1.67 | — | 1.67 | — | ns |
| **Control Delays** | | | | | | | | |
| $t_{BCLK}$ | GLB PT Clock Delay | — | 1.12 | — | 1.12 | — | 0.62 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | — | 0.87 | — | 0.87 | — | 0.87 | ns |
| $t_{BSR}$ | GLB PT Set/Reset Delay | — | 1.83 | — | 1.83 | — | 1.83 | ns |
| $t_{PTSR}$ | Macrocell PT Set/Reset Delay | — | 2.51 | — | 3.41 | — | 3.41 | ns |

## Signal Descriptions

| Signal Names | Description | |
|---|---|---|
| TMS | Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine. | |
| TCK | Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine. | |
| TDI | Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data. | |
| TDO | Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out. | |
| GOE0/IO, GOE1/IO | These pins are configured to be either Global Output Enable Input or as general I/O pins. | |
| GND | Ground | |
| NC | Not Connected | |
| $V_{CC}$ | The power supply pins for logic core and JTAG port. | |
| CLK0/I, CLK1/I, CLK2/I, CLK3/I | These pins are configured to be either CLK input or as an input. | |
| $V_{CCO0}$, $V_{CCO1}$ | The power supply pins for each I/O bank. | |
| yzz | Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15. | |
| | ispMACH 4032 | y: A-B |
| | ispMACH 4064 | y: A-D |
| | ispMACH 4128 | y: A-H |
| | ispMACH 4256 | y: A-P |
| | ispMACH 4384 | y: A-P, AX-HX |
| | ispMACH 4512 | y: A-P, AX-PX |

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

## ispMACH 4000V/B/C ORP Reference Table

| | 4032V/B/C | | 4064V/B/C | | | 4128V/B/C | | | 4256V/B/C | | | | 4384V/B/C | | 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Number of I/Os | 30[1] | 32 | 30[2] | 32 | 64 | 64 | 92[3] | 96 | 64 | 96[4] | 128 | 160 | 128 | 192 | 128 | 208 |
| Number of GLBs | 2 | 2 | 4 | 4 | 4 | 8 | 8 | 8 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| Number of I/Os / GLB | 16 | 16 | 8 | 8 | 16 | 8 | 12 | 12 | 4 | 8 | 8 | 10 | 8 | 8 | 8 | Mixture of 8 & 4[5] |
| Reference ORP Table | 16 I/Os / GLB | | 8 I/Os / GLB | | 16 I/Os / GLB | 8 I/Os / GLB | 12 I/Os / GLB | | 4 I/Os / GLB | 8 I/Os / GLB | 8 I/Os / GLB | 10 I/Os / GLB | 8 I/Os / GLB | | 8 I/Os / GLB | 8 I/Os / GLB 4 I/Os / GLB |

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.
2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.
3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os
4. 256-macrocell device, 144 TQFP: 16 GLBs have 6 I/Os per
5. 512-macrocell device: 20 GLBs have 8 I/Os per, 12 GLBs have 4 I/Os per

## ispMACH 4000Z ORP Reference Table

| | 4032Z | 4064Z | | 4128Z | | 4256Z | | |
|---|---|---|---|---|---|---|---|---|
| Number of I/Os | 32 | 32 | 64 | 64 | 96 | 64 | 96[1] | 128 |
| Number of GLBs | 2 | 4 | 4 | 8 | 8 | 16 | 16 | 16 |
| Number of I/Os / GLB | 16 | 8 | 16 | 8 | 12 | 4 | 8 | 8 |
| Reference ORP Table | 16 I/Os / GLB | 8 I/Os / GLB | 16 I/Os / GLB | 8 I/Os / GLB | 12 I/Os / GLB | 4 I/Os / GLB | 8 I/Os / GLB | 8 I/Os / GLB |

1. 256-macrocell device, 132 csBGA: 16 GLBs have 6 I/Os per

## ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections: 100-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4064V/B/C/Z | | ispMACH 4128V/B/C/Z | | ispMACH 4256V/B/C/Z | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 83 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| 84 | 1 | D3 | D^3 | H6 | H^3 | P12 | P^3 |
| 85 | 1 | D2 | D^2 | H4 | H^2 | P10 | P^2 |
| 86 | 1 | D1 | D^1 | H2 | H^1 | P6 | P^1 |
| 87 | 1 | D0/GOE1 | D^0 | H0/GOE1 | H^0 | P2/OE1 | P^0 |
| 88 | 1 | CLK3/I | - | CLK3/I | - | CLK3/I | - |
| 89 | 0 | CLK0/I | - | CLK0/I | - | CLK0/I | - |
| 90 | - | VCC | - | VCC | - | VCC | - |
| 91 | 0 | A0/GOE0 | A^0 | A0/GOE0 | A^0 | A2/GOE0 | A^0 |
| 92 | 0 | A1 | A^1 | A2 | A^1 | A6 | A^1 |
| 93 | 0 | A2 | A^2 | A4 | A^2 | A10 | A^2 |
| 94 | 0 | A3 | A^3 | A6 | A^3 | A12 | A^3 |
| 95 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 96 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 97 | 0 | A4 | A^4 | A8 | A^4 | B2 | B^0 |
| 98 | 0 | A5 | A^5 | A10 | A^5 | B6 | B^1 |
| 99 | 0 | A6 | A^6 | A12 | A^6 | B10 | B^2 |
| 100 | 0 | A7 | A^7 | A14 | A^7 | B12 | B^3 |

*This pin is input only.

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 1 | 0 | GND | - |
| 2 | 0 | TDI | - |
| 3 | 0 | VCCO (Bank 0) | - |
| 4 | 0 | B0 | B^0 |
| 5 | 0 | B1 | B^1 |
| 6 | 0 | B2 | B^2 |
| 7 | 0 | B4 | B^3 |
| 8 | 0 | B5 | B^4 |
| 9 | 0 | B6 | B^5 |
| 10 | 0 | GND (Bank 0) | - |
| 11 | 0 | B8 | B^6 |
| 12 | 0 | B9 | B^7 |
| 13 | 0 | B10 | B^8 |
| 14 | 0 | B12 | B^9 |
| 15 | 0 | B13 | B^10 |
| 16 | 0 | B14 | B^11 |
| 17 | 0 | VCCO (Bank 0) | - |
| 18 | 0 | C14 | C^11 |

## ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4128V/B/C | |
|---|---|---|---|
| | | GLB/MC/Pad | ORP |
| 19 | 0 | C13 | C^10 |
| 20 | 0 | C12 | C^9 |
| 21 | 0 | C10 | C^8 |
| 22 | 0 | C9 | C^7 |
| 23 | 0 | C8 | C^6 |
| 24 | 0 | GND (Bank 0) | - |
| 25 | 0 | C6 | C^5 |
| 26 | 0 | C5 | C^4 |
| 27 | 0 | C4 | C^3 |
| 28 | 0 | C2 | C^2 |
| 29 | 0 | C0 | C^0 |
| 30 | 0 | VCCO (Bank 0) | - |
| 31 | 0 | TCK | - |
| 32 | 0 | VCC | - |
| 33 | 0 | GND | - |
| 34 | 0 | D14 | D^11 |
| 35 | 0 | D13 | D^10 |
| 36 | 0 | D12 | D^9 |
| 37 | 0 | D10 | D^8 |
| 38 | 0 | D9 | D^7 |
| 39 | 0 | D8 | D^6 |
| 40 | 0 | GND (Bank 0) | - |
| 41 | 0 | VCCO (Bank 0) | - |
| 42 | 0 | D6 | D^5 |
| 43 | 0 | D5 | D^4 |
| 44 | 0 | D4 | D^3 |
| 45 | 0 | D2 | D^2 |
| 46 | 0 | D1 | D^1 |
| 47 | 0 | D0 | D^0 |
| 48 | 0 | CLK1/I | - |
| 49 | 1 | GND (Bank 1) | - |
| 50 | 1 | CLK2/I | - |
| 51 | 1 | VCC | - |
| 52 | 1 | E0 | E^0 |
| 53 | 1 | E1 | E^1 |
| 54 | 1 | E2 | E^2 |
| 55 | 1 | E4 | E^3 |
| 56 | 1 | E5 | E^4 |
| 57 | 1 | E6 | E^5 |
| 58 | 1 | VCCO (Bank 1) | - |
| 59 | 1 | GND (Bank 1) | - |
| 60 | 1 | E8 | E^6 |
| 61 | 1 | E9 | E^7 |

# ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections: 132-Ball csBGA (Cont.)

| | | ispMACH 4064Z | | ispMACH 4128Z | | ispMACH 4256Z | |
|---|---|---|---|---|---|---|---|
| Ball Number | Bank Number | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| D13 | 1 | D10 | D^10 | G4 | G^3 | N6 | N^3 |
| D14 | 1 | D9 | D^9 | G2 | G^2 | N8 | N^4 |
| D12 | 1 | D8 | D^8 | G1 | G^1 | N10 | N^5 |
| C14 | 1 | I | - | G0 | G^0 | N12 | N^6 |
| C13 | 1 | NC | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| B14 | - | TDO | - | TDO | - | TDO | - |
| A14 | - | VCC | - | VCC | - | VCC | - |
| A13 | - | GND | - | GND | - | GND | - |
| B13 | 1 | NC | - | H14 | H^11 | O12 | O^6 |
| A12 | 1 | I | - | H13 | H^10 | O10 | O^5 |
| C12 | 1 | D7 | D^7 | H12 | H^9 | O8 | O^4 |
| B12 | 1 | D6 | D^6 | H10 | H^8 | O6 | O^3 |
| A11 | 1 | D5 | D^5 | H9 | H^7 | O4 | O^2 |
| C11 | 1 | D4 | D^4 | H8 | H^6 | O2 | O^1 |
| B11 | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| A10 | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| B10 | 1 | NC | - | H6 | H^5 | P12 | P^6 |
| C10 | 1 | NC | - | H5 | H^4 | P10 | P^5 |
| B9 | 1 | D3 | D^3 | H4 | H^3 | P8 | P^4 |
| A9 | 1 | D2 | D^2 | H2 | H^2 | P6 | P^3 |
| C9 | 1 | D1 | D^1 | H1 | H^1 | P4 | P^2 |
| A8 | 1 | D0/GOE1 | D^0 | H0/GOE1 | H^0 | P2/GOE1 | P^1 |
| B8 | 1 | CLK3/I | - | CLK3/I | - | CLK3/I | - |
| C8 | 0 | CLK0/I | - | CLK0/I | - | CLK0/I | - |
| B7 | - | VCC | - | VCC | - | VCC | - |
| A7 | 0 | NC[1] | - | NC[1] | - | I[1] | - |
| C7 | 0 | A0/GOE0 | A^0 | A0/GOE0 | A^0 | A2/GOE0 | A^1 |
| A6 | 0 | A1 | A^1 | A1 | A^1 | A4 | A^2 |
| B6 | 0 | A2 | A^2 | A2 | A^2 | A6 | A^3 |
| C6 | 0 | A3 | A^3 | A4 | A^3 | A8 | A^4 |
| B5 | 0 | NC | - | A5 | A^4 | A10 | A^5 |
| A5 | 0 | NC | - | A6 | A^5 | A12 | A^6 |
| C5 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| B4 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| A4 | 0 | NC | - | A8 | A^6 | B2 | B^1 |
| C4 | 0 | A4 | A^4 | A9 | A^7 | B4 | B^2 |
| A3 | 0 | A5 | A^5 | A10 | A^8 | B6 | B^3 |
| B3 | 0 | A6 | A^6 | A12 | A^9 | B8 | B^4 |
| A2 | 0 | A7 | A^7 | A13 | A^10 | B10 | B^5 |
| A1 | 0 | NC | - | A14 | A^11 | B12 | B^6 |

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4256Z device.

## ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections: 176-Pin TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4256V/B/C/Z | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| 19 | 0 | D4 | D^2 | E4 | E^2 | G4 | G^2 |
| 20 | 0 | D2 | D^1 | E2 | E^1 | G2 | G^1 |
| 21 | 0 | D0 | D^0 | E0 | E^0 | G0 | G^0 |
| 22 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 23 | 0 | E0 | E^0 | H0 | H^0 | J0 | J^0 |
| 24 | 0 | E2 | E^1 | H2 | H^1 | J2 | J^1 |
| 25 | 0 | E4 | E^2 | H4 | H^2 | J4 | J^2 |
| 26 | 0 | E6 | E^3 | H6 | H^3 | J6 | J^3 |
| 27 | 0 | E8 | E^4 | H8 | H^4 | J8 | J^4 |
| 28 | 0 | E10 | E^5 | H10 | H^5 | J10 | J^5 |
| 29 | 0 | E12 | E^6 | H12 | H^6 | J12 | J^6 |
| 30 | 0 | E14 | E^7 | H14 | H^7 | J14 | J^7 |
| 31 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 32 | 0 | F0 | F^0 | J0 | J^0 | N0 | N^0 |
| 33 | 0 | F2 | F^1 | J2 | J^1 | N2 | N^1 |
| 34 | 0 | F4 | F^2 | J4 | J^2 | N4 | N^2 |
| 35 | 0 | F6 | F^3 | J6 | J^3 | N6 | N^3 |
| 36 | 0 | F8 | F^4 | J8 | J^4 | N8 | N^4 |
| 37 | 0 | F10 | F^5 | J10 | J^5 | N10 | N^5 |
| 38 | 0 | F12 | F^6 | J12 | J^6 | N12 | N^6 |
| 39 | 0 | F14 | F^7 | J14 | J^7 | N14 | N^7 |
| 40 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 41 | - | TCK | - | TCK | - | TCK | - |
| 42 | - | VCC | - | VCC | - | VCC | - |
| 43 | - | NC | - | NC | - | NC | - |
| 44 | - | NC | - | NC | - | NC | - |
| 45 | - | NC | - | NC | - | NC | - |
| 46 | - | GND | - | GND (Bank 0) | - | GND | - |
| 47 | 0 | G14 | G^7 | K14 | K^7 | O14 | O^7 |
| 48 | 0 | G12 | G^6 | K12 | K^6 | O12 | O^6 |
| 49 | 0 | G10 | G^5 | K10 | K^5 | O10 | O^5 |
| 50 | 0 | G8 | G^4 | K8 | K^4 | O8 | O^4 |
| 51 | 0 | G6 | G^3 | K6 | K^3 | O6 | O^3 |
| 52 | 0 | G4 | G^2 | K4 | K^2 | O4 | O^2 |
| 53 | 0 | G2 | G^1 | K2 | K^1 | O2 | O^1 |
| 54 | 0 | G0 | G^0 | K0 | K^0 | O0 | O^0 |
| 55 | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| 56 | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| 57 | 0 | H14 | H^7 | L14 | L^7 | P14 | P^7 |
| 58 | 0 | H12 | H^6 | L12 | L^6 | P12 | P^6 |
| 59 | 0 | H10 | H^5 | L10 | L^5 | P10 | P^5 |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| R5 | 0 | NC | - | NC | - | NC | - | L4 | L^1 |
| T5 | 0 | NC | - | NC | - | I2 | I^1 | L8 | L^2 |
| R6 | 0 | NC | - | NC | - | I0 | I^0 | L12 | L^3 |
| T6 | 0 | NC | - | H14 | H^9 | G12 | G^6 | M8 | M^2 |
| N7 | 0 | NC | - | H12 | H^8 | G14 | G^7 | M12 | M^3 |
| P7 | 0 | H14 | H^7 | H10 | H^7 | L14 | L^7 | P14 | P^7 |
| R7 | 0 | H12 | H^6 | H9 | H^6 | L12 | L^6 | P12 | P^6 |
| L8 | 0 | H10 | H^5 | H8 | H^5 | L10 | L^5 | P10 | P^5 |
| T7 | 0 | H8 | H^4 | H6 | H^4 | L8 | L^4 | P8 | P^4 |
| M8 | 0 | H6 | H^3 | H4 | H^3 | L6 | L^3 | P6 | P^3 |
| N8 | 0 | H4 | H^2 | H2 | H^2 | L4 | L^2 | P4 | P^2 |
| R8 | 0 | H2 | H^1 | H1 | H^1 | L2 | L^1 | P2 | P^1 |
| P8 | 0 | H0 | H^0 | H0 | H^0 | L0 | L^0 | P0 | P^0 |
| - | - | GND | - | GND | - | GND | - | GND | - |
| T8 | 0 | CLK1/I | - | CLK1/I | - | CLK1/I | - | CLK1/I | - |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| N9 | 1 | CLK2/I | - | CLK2/I | - | CLK2/I | - | CLK2/I | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| P9 | 1 | I0 | I^0 | I0 | I^0 | M0 | M^0 | AX0 | AX^0 |
| R9 | 1 | I2 | I^1 | I1 | I^1 | M2 | M^1 | AX2 | AX^1 |
| T9 | 1 | I4 | I^2 | I2 | I^2 | M4 | M^2 | AX4 | AX^2 |
| T10 | 1 | I6 | I^3 | I4 | I^3 | M6 | M^3 | AX6 | AX^3 |
| R10 | 1 | I8 | I^4 | I6 | I^4 | M8 | M^4 | AX8 | AX^4 |
| M9 | 1 | I10 | I^5 | I8 | I^5 | M10 | M^5 | AX10 | AX^5 |
| P10 | 1 | I12 | I^6 | I9 | I^6 | M12 | M^6 | AX12 | AX^6 |
| L9 | 1 | I14 | I^7 | I10 | I^7 | M14 | M^7 | AX14 | AX^7 |
| N10 | 1 | NC | - | I12 | I^8 | BX14 | BX^7 | DX0 | DX^0 |
| T11 | 1 | NC | - | I14 | I^9 | BX12 | BX^6 | DX4 | DX^1 |
| R11 | 1 | NC | - | NC | - | P0 | P^0 | EX0 | EX^0 |
| T12 | 1 | NC | - | NC | - | P2 | P^1 | EX4 | EX^1 |
| N12 | 1 | NC | - | NC | - | NC | - | EX8 | EX^2 |
| - | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| R12 | 1 | NC | - | NC | - | NC | - | EX12 | EX^3 |
| T13 | 1 | NC | - | J0 | J^0 | BX10 | BX^5 | DX8 | DX^2 |
| P12 | 1 | NC | - | J1 | J^1 | BX8 | BX^4 | DX12 | DX^3 |
| M10 | 1 | J0 | J^0 | J2 | J^2 | N0 | N^0 | BX0 | BX^0 |
| R13 | 1 | J2 | J^1 | J4 | J^3 | N2 | N^1 | BX2 | BX^1 |
| L10 | 1 | J4 | J^2 | J6 | J^4 | N4 | N^2 | BX4 | BX^2 |
| T14 | 1 | J6 | J^3 | J8 | J^5 | N6 | N^3 | BX6 | BX^3 |
| M11 | 1 | J8 | J^4 | J9 | J^6 | N8 | N^4 | BX8 | BX^4 |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| H15 | 1 | M2 | M^1 | M1 | M^1 | DX2 | DX^1 | JX2 | JX^1 |
| H14 | 1 | M4 | M^2 | M2 | M^2 | DX4 | DX^2 | JX4 | JX^2 |
| H13 | 1 | M6 | M^3 | M4 | M^3 | DX6 | DX^3 | JX6 | JX^3 |
| G16 | 1 | M8 | M^4 | M6 | M^4 | DX8 | DX^4 | JX8 | JX^4 |
| H12 | 1 | M10 | M^5 | M8 | M^5 | DX10 | DX^5 | JX10 | JX^5 |
| G15 | 1 | M12 | M^6 | M9 | M^6 | DX12 | DX^6 | JX12 | JX^6 |
| H11 | 1 | M14 | M^7 | M10 | M^7 | DX14 | DX^7 | JX14 | JX^7 |
| F16 | 1 | NC | - | M12 | M^8 | CX0 | CX^0 | IX0 | IX^0 |
| G13 | 1 | NC | - | M14 | M^9 | CX2 | CX^1 | IX4 | IX^1 |
| G14 | 1 | NC | - | NC | - | EX14 | EX^7 | KX0 | KX^0 |
| F15 | 1 | NC | - | NC | - | EX12 | EX^6 | KX2 | KX^1 |
| E16 | 1 | NC | - | NC | - | NC | - | KX4 | KX^2 |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| - | 1 | - | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| E15 | 1 | NC | - | NC | - | NC | - | KX6 | KX^3 |
| G12 | 1 | NC | - | NC | - | EX10 | EX^5 | KX8 | KX^4 |
| E13 | 1 | NC | - | NC | - | EX8 | EX^4 | KX10 | KX^5 |
| D16 | 1 | NC | - | N0 | N^0 | CX4 | CX^2 | IX8 | IX^2 |
| E14 | 1 | NC | - | N1 | N^1 | CX6 | CX^3 | IX12 | IX^3 |
| G11 | 1 | N0 | N^0 | N2 | N^2 | FX0 | FX^0 | NX0 | NX^0 |
| D15 | 1 | N2 | N^1 | N4 | N^3 | FX2 | FX^1 | NX2 | NX^1 |
| F11 | 1 | N4 | N^2 | N6 | N^4 | FX4 | FX^2 | NX4 | NX^2 |
| C16 | 1 | N6 | N^3 | N8 | N^5 | FX6 | FX^3 | NX6 | NX^3 |
| F12 | 1 | N8 | N^4 | N9 | N^6 | FX8 | FX^4 | NX8 | NX^4 |
| D14 | 1 | N10 | N^5 | N10 | N^7 | FX10 | FX^5 | NX10 | NX^5 |
| C15 | 1 | N12 | N^6 | N12 | N^8 | FX12 | FX^6 | NX12 | NX^6 |
| B16 | 1 | N14 | N^7 | N14 | N^9 | FX14 | FX^7 | NX14 | NX^7 |
| - | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| C14 | - | TDO | - | TDO | - | TDO | - | TDO | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| - | - | GND | - | GND | - | GND | - | GND | - |
| - | 1 | - | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| A15 | 1 | NC | - | NC | - | EX6 | EX^3 | KX12 | KX^6 |
| B14 | 1 | NC | - | NC | - | EX4 | EX^2 | KX14 | KX^7 |
| E12 | 1 | O14 | O^7 | O14 | O^9 | GX14 | GX^7 | OX14 | OX^7 |
| A14 | 1 | O12 | O^6 | O12 | O^8 | GX12 | GX^6 | OX12 | OX^6 |
| C13 | 1 | O10 | O^5 | O10 | O^7 | GX10 | GX^5 | OX10 | OX^5 |
| D13 | 1 | O8 | O^4 | O9 | O^6 | GX8 | GX^4 | OX8 | OX^4 |
| E11 | 1 | O6 | O^3 | O8 | O^5 | GX6 | GX^3 | OX6 | OX^3 |
| B13 | 1 | O4 | O^2 | O6 | O^4 | GX4 | GX^2 | OX4 | OX^2 |
| F10 | 1 | O2 | O^1 | O4 | O^3 | GX2 | GX^1 | OX2 | OX^1 |

## ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections: 256-Ball ftBGA/fpBGA (Cont.)

| Ball Number | I/O Bank | ispMACH 4256V/B/C 128-I/O | | ispMACH 4256V/B/C 160-I/O | | ispMACH 4384V/B/C | | ispMACH 4512V/B/C | |
|---|---|---|---|---|---|---|---|---|---|
| | | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP | GLB/MC/Pad | ORP |
| C12 | 1 | O0 | O^0 | O2 | O^2 | GX0 | GX^0 | OX0 | OX^0 |
| E10 | 1 | NC | - | O1 | O^1 | CX8 | CX^4 | MX0 | MX^0 |
| A13 | 1 | NC | - | O0 | O^0 | CX10 | CX^5 | MX4 | MX^1 |
| D12 | 1 | NC | - | NC | - | NC | - | LX0 | LX^0 |
| - | 1 | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - | GND (Bank 1) | - |
| - | 1 | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - | VCCO (Bank 1) | - |
| B12 | 1 | NC | - | NC | - | NC | - | LX4 | LX^1 |
| A12 | 1 | NC | - | NC | - | EX2 | EX^1 | LX8 | LX^2 |
| B11 | 1 | NC | - | NC | - | EX0 | EX^0 | LX12 | LX^3 |
| A11 | 1 | NC | - | P14 | P^9 | CX12 | CX^6 | MX8 | MX^2 |
| D10 | 1 | NC | - | P12 | P^8 | CX14 | CX^7 | MX12 | MX^3 |
| C10 | 1 | P14 | P^7 | P10 | P^7 | HX14 | HX^7 | PX14 | PX^7 |
| B10 | 1 | P12 | P^6 | P9 | P6 | HX12 | HX^6 | PX12 | PX^6 |
| A10 | 1 | P10 | P^5 | P8 | P^5 | HX10 | HX^5 | PX10 | PX^5 |
| A9 | 1 | P8 | P^4 | P6 | P^4 | HX8 | HX^4 | PX8 | PX^4 |
| F9 | 1 | P6 | P^3 | P4 | P^3 | HX6 | HX^3 | PX6 | PX^3 |
| B9 | 1 | P4 | P^2 | P2 | P^2 | HX4 | HX^2 | PX4 | PX^2 |
| E9 | 1 | P2/GOE1 | P^1 | P1/GOE1 | P^1 | HX2/GOE1 | HX^1 | PX2/GOE1 | PX^1 |
| C9 | 1 | P0 | P^0 | P0 | P^0 | HX0 | HX^0 | PX0 | PX^0 |
| - | - | GND | - | GND | | GND | - | GND | - |
| D9 | 1 | CLK3/I | - | CLK3/I | - | CLK3/I | - | CLK3/I | - |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| B8 | 0 | CLK0/I | - | CLK0/I | - | CLK0/I | - | CLK0/I | - |
| - | - | VCC | - | VCC | - | VCC | - | VCC | - |
| D8 | 0 | A0 | A^0 | A0 | A^0 | A0 | A^0 | A0 | A^0 |
| C8 | 0 | A2/GOE0 | A^1 | A1/GOE0 | A^1 | A2/GOE0 | A^1 | A2/GOE0 | A^1 |
| A8 | 0 | A4 | A^2 | A2 | A^2 | A4 | A^2 | A4 | A^2 |
| A7 | 0 | A6 | A^3 | A4 | A^3 | A6 | A^3 | A6 | A^3 |
| B7 | 0 | A8 | A^4 | A6 | A^4 | A8 | A^4 | A8 | A^4 |
| E8 | 0 | A10 | A^5 | A8 | A^5 | A10 | A^5 | A10 | A^5 |
| D7 | 0 | A12 | A^6 | A9 | A^6 | A12 | A^6 | A12 | A^6 |
| F8 | 0 | A14 | A^7 | A10 | A^7 | A14 | A^7 | A14 | A^7 |
| C7 | 0 | NC | - | A12 | A^8 | F14 | F^7 | D0 | D^0 |
| A6 | 0 | NC | - | A14 | A^9 | F12 | F^6 | D4 | D^1 |
| B6 | 0 | NC | - | NC | - | D14 | D^7 | E0 | E^0 |
| A5 | 0 | NC | - | NC | - | D12 | D^6 | E4 | E^1 |
| B5 | 0 | NC | - | NC | - | NC | - | E8 | E^2 |
| - | 0 | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - | VCCO (Bank 0) | - |
| - | 0 | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - | GND (Bank 0) | - |
| D5 | 0 | NC | - | NC | - | NC | - | E12 | E^3 |
| A4 | 0 | NC | - | B0 | B^0 | F10 | F^5 | D8 | D^2 |

## Part Number Description

LC XXXX X X – XX XX XXX X X XX

**Device Family**

**Device Number**
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells
4384 = 384 Macrocells
4512 = 512 Macrocells

**Power**
Z = Zero Power
Blank = Low Power

**Supply Voltage**
V = 3.3V
B = 2.5V
C = 1.8V

**Speed**
25 = 2.5ns
27 = 2.7ns
3 = 3.0ns
35 = 3.5ns
37 = 3.7ns
42 = 4.2ns
45 = 4.5ns
5 = 5.0ns
75 = 7.5ns
10 = 10.0ns

**Package**

| | |
|---|---|
| T = TQFP | TN = Lead-free TQFP |
| FT = ftBGA | FTN= Lead-free ftBGA |
| F = fpBGA[2] | FN = Lead-free fpBGA[2] |
| M = csBGA | MN = Lead-free csBGA |

**Pin/Ball Count**
44 (1.0mm thickness)
48 (1.0mm thickness)
56
100
128
132
144
176
256

**I/O Designator (if applicable)**
A = 128 I/Os
B = 160 I/Os

**Operating Temperature Range**
C = Commercial
I = Industrial
E = Extended[1]

**Production Status**
Blank = Final production
ES = Engineering Samples

1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).

2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

## ispMACH 4000 Family Speed Grade Offering

| | -25 | -27 | -3 | -35 | -37 | -42 | -45 | -5 | | -75 | | | -10 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Com | Com | Com | Com | Com | Com | Com | Com | Ind | Com | Ind | Ext | Ind |
| ispMACH 4032V/B/C | | | | | | | | | | | | 1 | |
| ispMACH 4064V/B/C | | | | | | | | | | | | 1 | |
| ispMACH 4128V/B/C | | | | | | | | | | | | 1 | |
| ispMACH 4256V/B/C | | | | | | | | | | | | | |
| ispMACH 4384V/B/C | | | | | | | | | | | | | |
| ispMACH 4512V/B/C | | | | | | | | | | | | | |
| ispMACH 4032ZC | | | | | | | | | | | | 1 | |
| ispMACH 4064ZC | | | | | | | | | | | | 1 | |
| ispMACH 4128ZC | | | | | | | | | | | | 1 | |
| ispMACH 4256ZC | | | | | | | | | | | | | |

1. 3.3V only.

**ispMACH 4000V (3.3V) Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4128V | LC4128V-27T144C | 128 | 3.3 | 2.7 | TQFP | 144 | 96 | C |
| | LC4128V-5T144C | 128 | 3.3 | 5 | TQFP | 144 | 96 | C |
| | LC4128V-75T144C | 128 | 3.3 | 7.5 | TQFP | 144 | 96 | C |
| | LC4128V-27T128C | 128 | 3.3 | 2.7 | TQFP | 128 | 92 | C |
| | LC4128V-5T128C | 128 | 3.3 | 5 | TQFP | 128 | 92 | C |
| | LC4128V-75T128C | 128 | 3.3 | 7.5 | TQFP | 128 | 92 | C |
| | LC4128V-27T100C | 128 | 3.3 | 2.7 | TQFP | 100 | 64 | C |
| | LC4128V-5T100C | 128 | 3.3 | 5 | TQFP | 100 | 64 | C |
| | LC4128V-75T100C | 128 | 3.3 | 7.5 | TQFP | 100 | 64 | C |
| LC4256V | LC4256V-3FT256AC | 256 | 3.3 | 3 | ftBGA | 256 | 128 | C |
| | LC4256V-5FT256AC | 256 | 3.3 | 5 | ftBGA | 256 | 128 | C |
| | LC4256V-75FT256AC | 256 | 3.3 | 7.5 | ftBGA | 256 | 128 | C |
| | LC4256V-3FT256BC | 256 | 3.3 | 3 | ftBGA | 256 | 160 | C |
| | LC4256V-5FT256BC | 256 | 3.3 | 5 | ftBGA | 256 | 160 | C |
| | LC4256V-75FT256BC | 256 | 3.3 | 7.5 | ftBGA | 256 | 160 | C |
| | LC4256V-3F256AC[1] | 256 | 3.3 | 3 | fpBGA | 256 | 128 | C |
| | LC4256V-5F256AC[1] | 256 | 3.3 | 5 | fpBGA | 256 | 128 | C |
| | LC4256V-75F256AC[1] | 256 | 3.3 | 7.5 | fpBGA | 256 | 128 | C |
| | LC4256V-3F256BC[1] | 256 | 3.3 | 3 | fpBGA | 256 | 160 | C |
| | LC4256V-5F256BC[1] | 256 | 3.3 | 5 | fpBGA | 256 | 160 | C |
| | LC4256V-75F256BC[1] | 256 | 3.3 | 7.5 | fpBGA | 256 | 160 | C |
| | LC4256V-3T176C | 256 | 3.3 | 3 | TQFP | 176 | 128 | C |
| | LC4256V-5T176C | 256 | 3.3 | 5 | TQFP | 176 | 128 | C |
| | LC4256V-75T176C | 256 | 3.3 | 7.5 | TQFP | 176 | 128 | C |
| | LC4256V-3T144C | 256 | 3.3 | 3 | TQFP | 144 | 96 | C |
| | LC4256V-5T144C | 256 | 3.3 | 5 | TQFP | 144 | 96 | C |
| | LC4256V-75T144C | 256 | 3.3 | 7.5 | TQFP | 144 | 96 | C |
| | LC4256V-3T100C | 256 | 3.3 | 3 | TQFP | 100 | 64 | C |
| | LC4256V-5T100C | 256 | 3.3 | 5 | TQFP | 100 | 64 | C |
| | LC4256V-75T100C | 256 | 3.3 | 7.5 | TQFP | 100 | 64 | C |
| LC4384V | LC4384V-35FT256C | 384 | 3.3 | 3.5 | ftBGA | 256 | 192 | C |
| | LC4384V-5FT256C | 384 | 3.3 | 5 | ftBGA | 256 | 192 | C |
| | LC4384V-75FT256C | 384 | 3.3 | 7.5 | ftBGA | 256 | 192 | C |
| | LC4384V-35F256C[1] | 384 | 3.3 | 3.5 | fpBGA | 256 | 192 | C |
| | LC4384V-5F256C[1] | 384 | 3.3 | 5 | fpBGA | 256 | 192 | C |
| | LC4384V-75F256C[1] | 384 | 3.3 | 7.5 | fpBGA | 256 | 192 | C |
| | LC4384V-35T176C | 384 | 3.3 | 3.5 | TQFP | 176 | 128 | C |
| | LC4384V-5T176C | 384 | 3.3 | 5 | TQFP | 176 | 128 | C |
| | LC4384V-75T176C | 384 | 3.3 | 7.5 | TQFP | 176 | 128 | C |

**ispMACH 4000C (1.8V) Lead-Free Commercial Devices (Cont.)**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4064C | LC4064C-25TN100C | 64 | 1.8 | 2.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064C-5TN100C | 64 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064C-75TN100C | 64 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| | LC4064C-25TN48C | 64 | 1.8 | 2.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064C-5TN48C | 64 | 1.8 | 5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064C-75TN48C | 64 | 1.8 | 7.5 | Lead-free TQFP | 48 | 32 | C |
| | LC4064C-25TN44C | 64 | 1.8 | 2.5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064C-5TN44C | 64 | 1.8 | 5 | Lead-free TQFP | 44 | 30 | C |
| | LC4064C-75TN44C | 64 | 1.8 | 7.5 | Lead-free TQFP | 44 | 30 | C |
| LC4128C | LC4128C-27TN128C | 128 | 1.8 | 2.7 | Lead-free TQFP | 128 | 92 | C |
| | LC4128C-5TN128C | 128 | 1.8 | 5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128C-75TN128C | 128 | 1.8 | 7.5 | Lead-free TQFP | 128 | 92 | C |
| | LC4128C-27TN100C | 128 | 1.8 | 2.7 | Lead-free TQFP | 100 | 64 | C |
| | LC4128C-5TN100C | 128 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4128C-75TN100C | 128 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| LC4256C | LC4256C-3FTN256AC | 256 | 1.8 | 3 | Lead-free ftBGA | 256 | 128 | C |
| | LC4256C-5FTN256AC | 256 | 1.8 | 5 | Lead-free ftBGA | 256 | 128 | C |
| | LC4256C-75FTN256AC | 256 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 128 | C |
| | LC4256C-3FTN256BC | 256 | 1.8 | 3 | Lead-free ftBGA | 256 | 160 | C |
| | LC4256C-5FTN256BC | 256 | 1.8 | 5 | Lead-free ftBGA | 256 | 160 | C |
| | LC4256C-75FTN256BC | 256 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 160 | C |
| | LC4256C-3FN256AC[1] | 256 | 1.8 | 3 | Lead-free fpBGA | 256 | 128 | C |
| | LC4256C-5FN256AC[1] | 256 | 1.8 | 5 | Lead-free fpBGA | 256 | 128 | C |
| | LC4256C-75FN256AC[1] | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 128 | C |
| | LC4256C-3FN256BC[1] | 256 | 1.8 | 3 | Lead-free fpBGA | 256 | 160 | C |
| | LC4256C-5FN256BC[1] | 256 | 1.8 | 5 | Lead-free fpBGA | 256 | 160 | C |
| | LC4256C-75FN256BC[1] | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 160 | C |
| | LC4256C-3TN176C | 256 | 1.8 | 3 | Lead-free TQFP | 176 | 128 | C |
| | LC4256C-5TN176C | 256 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | C |
| | LC4256C-75TN176C | 256 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | C |
| | LC4256C-3TN100C | 256 | 1.8 | 3 | Lead-free TQFP | 100 | 64 | C |
| | LC4256C-5TN100C | 256 | 1.8 | 5 | Lead-free TQFP | 100 | 64 | C |
| | LC4256C-75TN100C | 256 | 1.8 | 7.5 | Lead-free TQFP | 100 | 64 | C |
| LC4384C | LC4384C-35FTN256C | 384 | 1.8 | 3.5 | Lead-free ftBGA | 256 | 192 | C |
| | LC4384C-5FTN256C | 384 | 1.8 | 5 | Lead-free ftBGA | 256 | 192 | C |
| | LC4384C-75FTN256C | 384 | 1.8 | 7.5 | Lead-free ftBGA | 256 | 192 | C |
| | LC4384C-35FN256C[1] | 384 | 1.8 | 3.5 | Lead-free fpBGA | 256 | 192 | C |
| | LC4384C-5FN256C[1] | 384 | 1.8 | 5 | Lead-free fpBGA | 256 | 192 | C |
| | LC4384C-75FN256C[1] | 384 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 192 | C |
| | LC4384C-35TN176C | 384 | 1.8 | 3.5 | Lead-free TQFP | 176 | 128 | C |
| | LC4384C-5TN176C | 384 | 1.8 | 5 | Lead-free TQFP | 176 | 128 | C |
| | LC4384C-75TN176C | 384 | 1.8 | 7.5 | Lead-free TQFP | 176 | 128 | C |