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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064v-10t48i

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

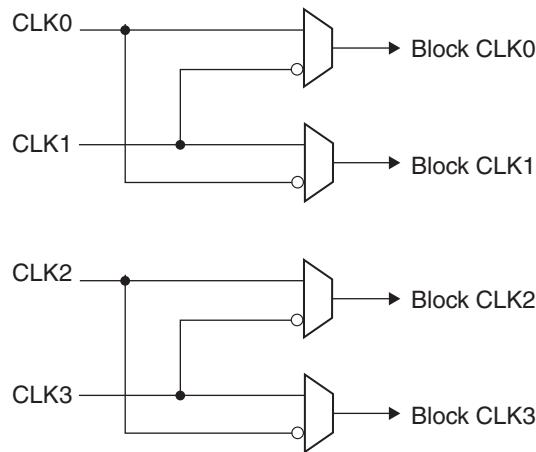
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



- LVTTL
- LVC MOS 1.8
- LVC MOS 3.3
- 3.3V PCI Compatible
- LVC MOS 2.5

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 device that has a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except ispMACH 4032

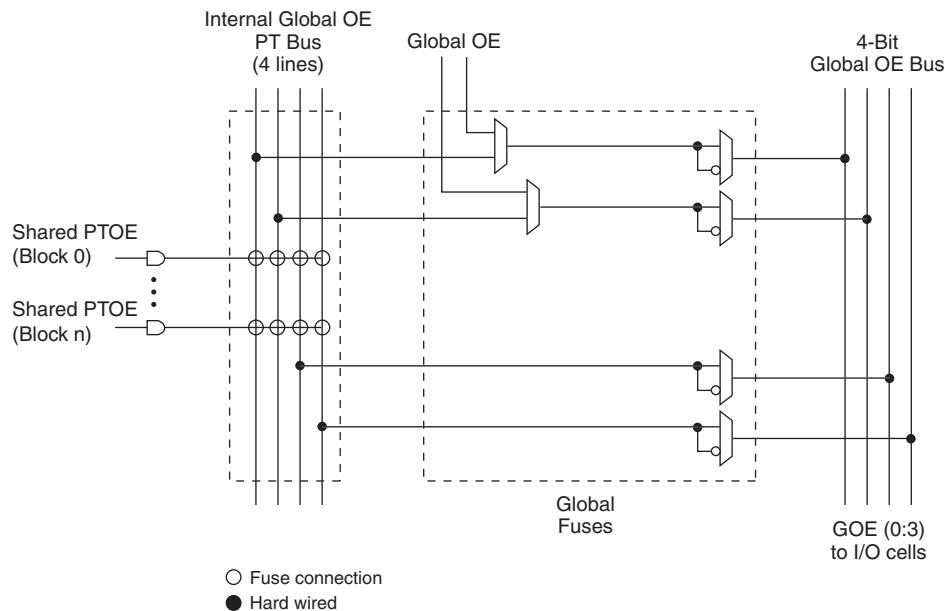


Figure 10. Global OE Generation for ispMACH 4032

Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E² low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative circuit design changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM® System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings^{1, 2, 3}

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMACH 4000V (3.3V)
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied ^{4, 5}	-0.5 to 5.5V	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duration of < 20ns.
5. Maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	ispMACH 4000C	1.65	1.95	V
	ispMACH 4000Z	1.7	1.9	V
	ispMACH 4000Z, Extended Functional Voltage Operation	1.6 ^{1, 2}	1.9	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V
T_j	Supply Voltage for 3.3V Devices	3.0	3.6	V
	Junction Temperature (Commercial)	0	90	C
	Junction Temperature (Industrial)	-40	105	C
	Junction Temperature (Extended)	-40	130	C

1. Devices operating at 1.6V can expect performance degradation up to 35%.
2. Applicable for devices with 2004 date codes and later. Contact factory for ordering instructions.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^{\circ}C$	—	± 30	± 150	μA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^{\circ}C$	—	± 30	± 200	μA

1. In insensitive to sequence of V_{CC} or V_{CCO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided $(V_{IN} - V_{CCO}) \leq 3.6V$.

2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).

3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} . Device defaults to pull-up until fuse circuitry is active.

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC ^{1, 2, 3, 5}	Operating Power Supply Current	Vcc = 1.8V, TA = 25°C	—	341	—	µA
		Vcc = 1.9V, TA = 70°C	—	361	—	µA
		Vcc = 1.9V, TA = 85°C	—	372	—	µA
		Vcc = 1.9V, TA = 125°C	—	468	—	µA
ICC ^{4, 5}	Standby Power Supply Current	Vcc = 1.8V, TA = 25°C	—	13	—	µA
		Vcc = 1.9V, TA = 70°C	—	32	55	µA
		Vcc = 1.9V, TA = 85°C	—	43	90	µA
		Vcc = 1.9V, TA = 125°C	—	135	—	µA

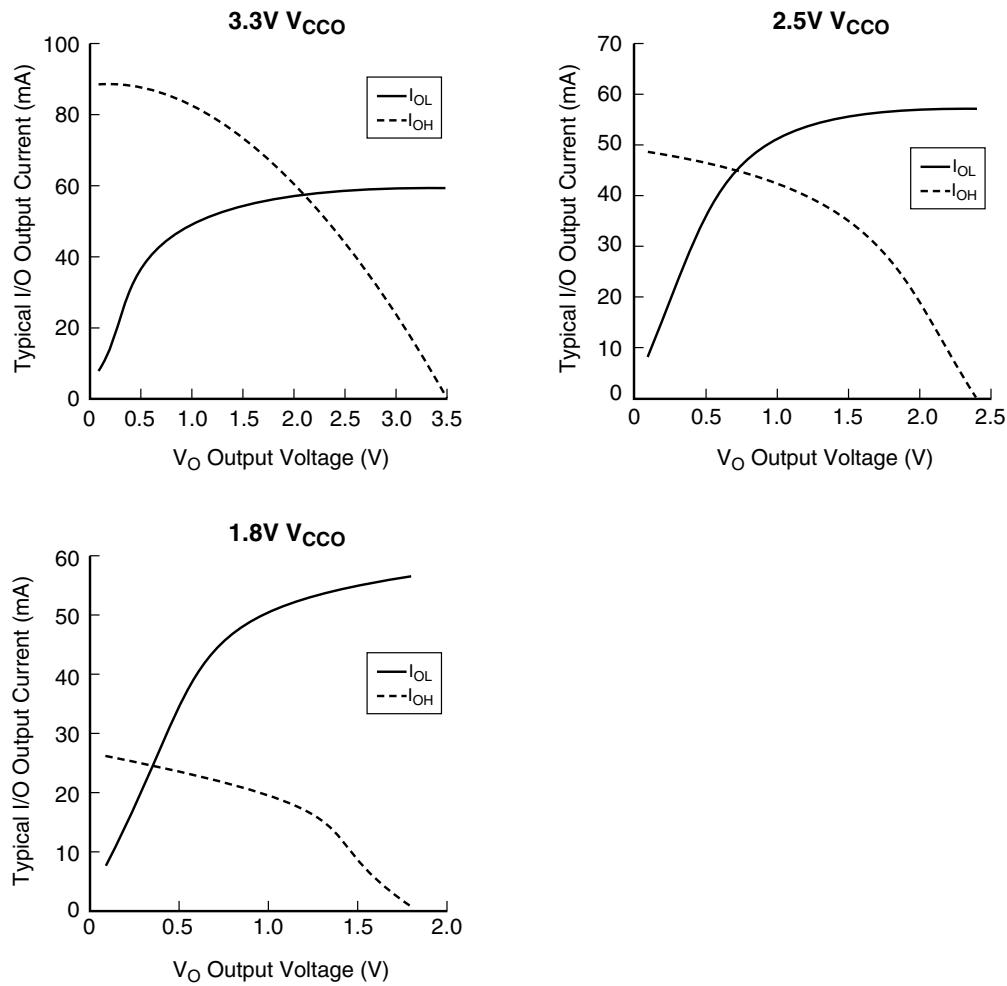
1. TA = 25°C, frequency = 1.0 MHz.

2. Device configured with 16-bit counters.

3. ICC varies with specific device configuration and operating frequency.

4. VCCO = 3.6V, VIN = 0V or VCCO, bus maintenance turned off. VIN above VCCO will add transient current above the specified standby ICC.

5. Includes VCCO current without output loading.



ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t_{IN}	Input Buffer Delay	—	0.95	—	1.50	—	2.00	ns
t_{GOE}	Global OE Pin Delay	—	4.04	—	6.04	—	7.04	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.83	—	2.28	—	3.28	ns
t_{BUF}	Delay through Output Buffer	—	1.00	—	1.50	—	1.50	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays								
t_{ROUTE}	Delay through GRP	—	1.51	—	2.26	—	3.26	ns
t_{MCELL}	Macrocell Delay	—	1.05	—	1.45	—	1.95	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.56	—	0.96	—	1.46	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	ns
t_{PD_b}	5-PT Bypass Propagation Delay	—	1.54	—	2.24	—	3.24	ns
t_{PD_i}	Macrocell Propagation Delay	—	0.94	—	1.24	—	1.74	ns
Register/Latch Delays								
t_S	D-Register Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.52	—	1.77	—	1.77	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t_H	D-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t_{HT}	T-Register Hold Time	1.68	—	2.93	—	3.93	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.52	—	1.57	—	1.57	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.68	—	1.18	—	1.18	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.68	—	1.18	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.67	—	1.17	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.32	—	1.57	—	1.57	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	ns
Control Delays								
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	0.62	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.51	—	3.41	—	3.41	ns

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹ (Cont.)

Signal	132-ball csBGA ⁷	144-pin TQFP ⁴	176-pin TQFP ⁴	256-ball ftBGA/fpBGA ^{2, 3, 7, 9}
VCC	P1, A14, B7, N8	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
VCCO0 VCCO (Bank 0)	G3, P5, C1 ⁸ , M2 ⁸ , C5	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1 VCCO (Bank 1)	M10, M14 ⁸ , H12, A10, C13 ⁸	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	B1, P2, N14, A13	1, 37, 73, 109	2, 46 ⁵ , 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank 0)	E2, K2, N4, B4	10, 18 ⁶ , 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	N11, K13, E13, B11	55, 65, 82, 90 ⁶ , 99, 118	67, 79, 101, 119, 143	
NC	4064Z: C1, C3, E1, E3, H2, J3, K1, M2, M4, N5, P7, P8, M8, P10, P11, P14, M12, K14, K12, G13, G14, E14, C13, B13, B10, C10, A7, B5, A5, A4, A1 4128Z: P8, A7	4128V: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 4256V: 18, 90	1, 43, 44, 45, 89, 131, 132, 133	4256V/B/C, 128 I/O: A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15 4256V/B/C, 160 I/O: A5, A12, A15, B5, B6, B11, B12, B14, D4, D5, D12, E1, E4, E5, E13, E15, E16, F1, F2, F15, G1, G5, G12, G14, L1, L2, L12, L15, L16, M1, M2, M3, M12, M16, N1, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T4, T5, T12, T15 4384V/B/C: B5, B12, D5, D12, E1, E15, E16, F2, L12, M1, M2, M16, N12, R5, R12, T4 4512V/B/C: None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. V_{CCO} balls connect to two power planes within the package, one for V_{CCO0} and one for V_{CCO1}.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
8. ispMACH 4128Z and 4256Z only. NC for ispMACH 4064Z.
9. Use 256 ftBGA package for all new designs. Refer to PCN#14A-07 for 256 fpBGA package discontinuance.

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:
44-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	-	TCK	-	TCK	-
11	-	VCC	-	VCC	-
12	-	GND	-	GND	-
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	-	CLK2/I	-
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	-	TMS	-	TMS	-
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	-	GND (Bank 1)	-
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	-	TDO	-	TDO	-
33	-	VCC	-	VCC	-
34	-	GND	-	GND	-
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	-	CLK0/I	-
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D^3	H6	H^3	P12	P^3
85	1	D2	D^2	H4	H^2	P10	P^2
86	1	D1	D^1	H2	H^1	P6	P^1
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	P^0
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	A^0
92	0	A1	A^1	A2	A^1	A6	A^1
93	0	A2	A^2	A4	A^2	A10	A^2
94	0	A3	A^3	A6	A^3	A12	A^3
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A^4	A8	A^4	B2	B^0
98	0	A5	A^5	A10	A^5	B6	B^1
99	0	A6	A^6	A12	A^6	B10	B^2
100	0	A7	A^7	A14	A^7	B12	B^3

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	-
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	-
18	0	C14	C^11

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
19	0	D4	D^2	E4	E^2	G4	G^2
20	0	D2	D^1	E2	E^1	G2	G^1
21	0	D0	D^0	E0	E^0	G0	G^0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E^0	H0	H^0	J0	J^0
24	0	E2	E^1	H2	H^1	J2	J^1
25	0	E4	E^2	H4	H^2	J4	J^2
26	0	E6	E^3	H6	H^3	J6	J^3
27	0	E8	E^4	H8	H^4	J8	J^4
28	0	E10	E^5	H10	H^5	J10	J^5
29	0	E12	E^6	H12	H^6	J12	J^6
30	0	E14	E^7	H14	H^7	J14	J^7
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F^0	J0	J^0	N0	N^0
33	0	F2	F^1	J2	J^1	N2	N^1
34	0	F4	F^2	J4	J^2	N4	N^2
35	0	F6	F^3	J6	J^3	N6	N^3
36	0	F8	F^4	J8	J^4	N8	N^4
37	0	F10	F^5	J10	J^5	N10	N^5
38	0	F12	F^6	J12	J^6	N12	N^6
39	0	F14	F^7	J14	J^7	N14	N^7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-	VCC	-
43	-	NC	-	NC	-	NC	-
44	-	NC	-	NC	-	NC	-
45	-	NC	-	NC	-	NC	-
46	-	GND	-	GND (Bank 0)	-	GND	-
47	0	G14	G^7	K14	K^7	O14	O^7
48	0	G12	G^6	K12	K^6	O12	O^6
49	0	G10	G^5	K10	K^5	O10	O^5
50	0	G8	G^4	K8	K^4	O8	O^4
51	0	G6	G^3	K6	K^3	O6	O^3
52	0	G4	G^2	K4	K^2	O4	O^2
53	0	G2	G^1	K2	K^1	O2	O^1
54	0	G0	G^0	K0	K^0	O0	O^0
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H^7	L14	L^7	P14	P^7
58	0	H12	H^6	L12	L^6	P12	P^6
59	0	H10	H^5	L10	L^5	P10	P^5

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
H15	1	M2	M^1	M1	M^1	DX2	DX^1	JX2	JX^1
H14	1	M4	M^2	M2	M^2	DX4	DX^2	JX4	JX^2
H13	1	M6	M^3	M4	M^3	DX6	DX^3	JX6	JX^3
G16	1	M8	M^4	M6	M^4	DX8	DX^4	JX8	JX^4
H12	1	M10	M^5	M8	M^5	DX10	DX^5	JX10	JX^5
G15	1	M12	M^6	M9	M^6	DX12	DX^6	JX12	JX^6
H11	1	M14	M^7	M10	M^7	DX14	DX^7	JX14	JX^7
F16	1	NC	-	M12	M^8	CX0	CX^0	IX0	IX^0
G13	1	NC	-	M14	M^9	CX2	CX^1	IX4	IX^1
G14	1	NC	-	NC	-	EX14	EX^7	KX0	KX^0
F15	1	NC	-	NC	-	EX12	EX^6	KX2	KX^1
E16	1	NC	-	NC	-	NC	-	KX4	KX^2
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E15	1	NC	-	NC	-	NC	-	KX6	KX^3
G12	1	NC	-	NC	-	EX10	EX^5	KX8	KX^4
E13	1	NC	-	NC	-	EX8	EX^4	KX10	KX^5
D16	1	NC	-	N0	N^0	CX4	CX^2	IX8	IX^2
E14	1	NC	-	N1	N^1	CX6	CX^3	IX12	IX^3
G11	1	N0	N^0	N2	N^2	FX0	FX^0	NX0	NX^0
D15	1	N2	N^1	N4	N^3	FX2	FX^1	NX2	NX^1
F11	1	N4	N^2	N6	N^4	FX4	FX^2	NX4	NX^2
C16	1	N6	N^3	N8	N^5	FX6	FX^3	NX6	NX^3
F12	1	N8	N^4	N9	N^6	FX8	FX^4	NX8	NX^4
D14	1	N10	N^5	N10	N^7	FX10	FX^5	NX10	NX^5
C15	1	N12	N^6	N12	N^8	FX12	FX^6	NX12	NX^6
B16	1	N14	N^7	N14	N^9	FX14	FX^7	NX14	NX^7
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
C14	-	TDO	-	TDO	-	TDO	-	TDO	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
A15	1	NC	-	NC	-	EX6	EX^3	KX12	KX^6
B14	1	NC	-	NC	-	EX4	EX^2	KX14	KX^7
E12	1	O14	O^7	O14	O^9	GX14	GX^7	OX14	OX^7
A14	1	O12	O^6	O12	O^8	GX12	GX^6	OX12	OX^6
C13	1	O10	O^5	O10	O^7	GX10	GX^5	OX10	OX^5
D13	1	O8	O^4	O9	O^6	GX8	GX^4	OX8	OX^4
E11	1	O6	O^3	O8	O^5	GX6	GX^3	OX6	OX^3
B13	1	O4	O^2	O6	O^4	GX4	GX^2	OX4	OX^2
F10	1	O2	O^1	O4	O^3	GX2	GX^1	OX2	OX^1

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
C12	1	O0	O^0	O2	O^2	GX0	GX^0	OX0	OX^0
E10	1	NC	-	O1	O^1	CX8	CX^4	MX0	MX^0
A13	1	NC	-	O0	O^0	CX10	CX^5	MX4	MX^1
D12	1	NC	-	NC	-	NC	-	LX0	LX^0
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
B12	1	NC	-	NC	-	NC	-	LX4	LX^1
A12	1	NC	-	NC	-	EX2	EX^1	LX8	LX^2
B11	1	NC	-	NC	-	EX0	EX^0	LX12	LX^3
A11	1	NC	-	P14	P^9	CX12	CX^6	MX8	MX^2
D10	1	NC	-	P12	P^8	CX14	CX^7	MX12	MX^3
C10	1	P14	P^7	P10	P^7	HX14	HX^7	PX14	PX^7
B10	1	P12	P^6	P9	P6	HX12	HX^6	PX12	PX^6
A10	1	P10	P^5	P8	P^5	HX10	HX^5	PX10	PX^5
A9	1	P8	P^4	P6	P^4	HX8	HX^4	PX8	PX^4
F9	1	P6	P^3	P4	P^3	HX6	HX^3	PX6	PX^3
B9	1	P4	P^2	P2	P^2	HX4	HX^2	PX4	PX^2
E9	1	P2/GOE1	P^1	P1/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE1	PX^1
C9	1	P0	P^0	P0	P^0	HX0	HX^0	PX0	PX^0
-	-	GND	-	GND	-	GND	-	GND	-
D9	1	CLK3/I	-	CLK3/I	-	CLK3/I	-	CLK3/I	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
B8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-	CLK0/I	-
-	-	VCC	-	VCC	-	VCC	-	VCC	-
D8	0	A0	A^0	A0	A^0	A0	A^0	A0	A^0
C8	0	A2/GOE0	A^1	A1/GOE0	A^1	A2/GOE0	A^1	A2/GOE0	A^1
A8	0	A4	A^2	A2	A^2	A4	A^2	A4	A^2
A7	0	A6	A^3	A4	A^3	A6	A^3	A6	A^3
B7	0	A8	A^4	A6	A^4	A8	A^4	A8	A^4
E8	0	A10	A^5	A8	A^5	A10	A^5	A10	A^5
D7	0	A12	A^6	A9	A^6	A12	A^6	A12	A^6
F8	0	A14	A^7	A10	A^7	A14	A^7	A14	A^7
C7	0	NC	-	A12	A^8	F14	F^7	D0	D^0
A6	0	NC	-	A14	A^9	F12	F^6	D4	D^1
B6	0	NC	-	NC	-	D14	D^7	E0	E^0
A5	0	NC	-	NC	-	D12	D^6	E4	E^1
B5	0	NC	-	NC	-	NC	-	E8	E^2
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
D5	0	NC	-	NC	-	NC	-	E12	E^3
A4	0	NC	-	B0	B^0	F10	F^5	D8	D^2

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5M132I	64	1.8	5	csBGA	132	64	I
	LC4064ZC-75M132I	64	1.8	7.5	csBGA	132	64	I
	LC4064ZC-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064ZC-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064ZC-5M56I	64	1.8	5	csBGA	56	34	I
	LC4064ZC-75M56I	64	1.8	7.5	csBGA	56	34	I
	LC4064ZC-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064ZC-75T48I	64	1.8	7.5	TQFP	48	32	I
LC4128ZC	LC4128ZC-75M132I	128	1.8	7.5	csBGA	132	96	I
	LC4128ZC-75T100I	128	1.8	7.5	TQFP	100	64	I
LC4256ZC	LC4256ZC-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256ZC-75M132I	256	1.8	7.5	csBGA	132	96	I
	LC4256ZC-75T100I	256	1.8	7.5	TQFP	100	64	I

ispMACH 4000ZC (1.8V, Zero Power) Extended Temperature Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75T48E	32	1.8	7.5	TQFP	48	32	E
LC4064ZC	LC4064ZC-75T100E	64	1.8	7.5	TQFP	100	64	E
	LC4064ZC-75T48E	64	1.8	7.5	TQFP	48	32	E
LC4128ZC	LC4128ZC-75T100E	128	1.8	7.5	TQFP	100	64	E
LC4256ZC	LC4256ZC-75T176E	256	1.8	7.5	TQFP	176	128	E
	LC4256ZC-75T100E	256	1.8	7.5	TQFP	100	64	E

ispMACH 4000C (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25T48C	32	1.8	2.5	TQFP	48	32	C
	LC4032C-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032C-75T48C	32	1.8	7.5	TQFP	48	32	C
	LC4032C-25T44C	32	1.8	2.5	TQFP	44	30	C
	LC4032C-5T44C	32	1.8	5	TQFP	44	30	C
	LC4032C-75T44C	32	1.8	7.5	TQFP	44	30	C
LC4064C	LC4064C-25T100C	64	1.8	2.5	TQFP	100	64	C
	LC4064C-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064C-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064C-25T48C	64	1.8	2.5	TQFP	48	32	C
	LC4064C-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064C-75T48C	64	1.8	7.5	TQFP	48	32	C
	LC4064C-25T44C	64	1.8	2.5	TQFP	44	30	C
	LC4064C-5T44C	64	1.8	5	TQFP	44	30	C
	LC4064C-75T44C	64	1.8	7.5	TQFP	44	30	C

ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384C	LC4384C-5FT256I	384	1.8	5	ftBGA	256	192	I
	LC4384C-75FT256I	384	1.8	7.5	ftBGA	256	192	I
	LC4384C-10FT256I	384	1.8	10	ftBGA	256	192	I
	LC4384C-5F256I ¹	384	1.8	5	fpBGA	256	192	I
	LC4384C-75F256I ¹	384	1.8	7.5	fpBGA	256	192	I
	LC4384C-10F256I ¹	384	1.8	10	fpBGA	256	192	I
	LC4384C-5T176I	384	1.8	5	TQFP	176	128	I
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128	I
	LC4384C-10T176I	384	1.8	10	TQFP	176	128	I
LC4512C	LC4512C-5FT256I	512	1.8	5	ftBGA	256	208	I
	LC4512C-75FT256I	512	1.8	7.5	ftBGA	256	208	I
	LC4512C-10FT256I	512	1.8	10	ftBGA	256	208	I
	LC4512C-5F256I ¹	512	1.8	5	fpBGA	256	208	I
	LC4512C-75F256I ¹	512	1.8	7.5	fpBGA	256	208	I
	LC4512C-10F256I ¹	512	1.8	10	fpBGA	256	208	I
	LC4512C-5T176I	512	1.8	5	TQFP	176	128	I
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
	LC4512C-10T176I	512	1.8	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32	C
	LC4032B-5T48C	32	2.5	5	TQFP	48	32	C
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32	C
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30	C
	LC4032B-5T44C	32	2.5	5	TQFP	44	30	C
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30	C
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64	C
	LC4064B-5T100C	64	2.5	5	TQFP	100	64	C
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64	C
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32	C
	LC4064B-5T48C	64	2.5	5	TQFP	48	32	C
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32	C
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30	C
	LC4064B-5T44C	64	2.5	5	TQFP	44	30	C
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92	C
	LC4128B-5T128C	128	2.5	5	TQFP	128	92	C
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92	C
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64	C
	LC4128B-5T100C	128	2.5	5	TQFP	100	64	C
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64	C

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
	LC4064B-10T44I	64	2.5	10	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI ¹	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI ¹	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI ¹	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI ¹	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI ¹	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI ¹	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

Lead-Free Packaging**ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Commercial Devices**

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35MN56C	32	1.8	3.5	Lead-free csBGA	56	32	C
	LC4032ZC-5MN56C	32	1.8	5	Lead-free csBGA	56	32	C
	LC4032ZC-75MN56C	32	1.8	7.5	Lead-free csBGA	56	32	C
	LC4032ZC-35TN48C	32	1.8	3.5	Lead-free TQFP	48	32	C
	LC4032ZC-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032ZC-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
LC4064ZC	LC4064ZC-37MN132C	64	1.8	3.7	Lead-free csBGA	132	64	C
	LC4064ZC-5MN132C	64	1.8	5	Lead-free csBGA	132	64	C
	LC4064ZC-75MN132C	64	1.8	7.5	Lead-free csBGA	132	64	C
	LC4064ZC-37TN100C	64	1.8	3.7	Lead-free TQFP	100	64	C
	LC4064ZC-5TN100C	64	1.8	5	Lead-free TQFP	100	64	C
	LC4064ZC-75TN100C	64	1.8	7.5	Lead-free TQFP	100	64	C
	LC4064ZC-37MN56C	64	1.8	3.7	Lead-free csBGA	56	32	C
	LC4064ZC-5MN56C	64	1.8	5	Lead-free csBGA	56	32	C
	LC4064ZC-75MN56C	64	1.8	7.5	Lead-free csBGA	56	32	C
	LC4064ZC-37TN48C	64	1.8	3.7	Lead-free TQFP	48	32	C
	LC4064ZC-5TN48C	64	1.8	5	Lead-free TQFP	48	32	C
	LC4064ZC-75TN48C	64	1.8	7.5	Lead-free TQFP	48	32	C
LC4128ZC	LC4128ZC-42MN132C	128	1.8	4.2	Lead-free csBGA	132	96	C
	LC4128ZC-75MN132C	128	1.8	7.5	Lead-free csBGA	132	96	C
	LC4128ZC-42TN100C	128	1.8	4.2	Lead-free TQFP	100	64	C
	LC4128ZC-75TN100C	128	1.8	7.5	Lead-free TQFP	100	64	C
LC4256ZC	LC4256ZC-45TN176C	256	1.8	4.5	Lead-free TQFP	176	128	C
	LC4256ZC-75TN176C	256	1.8	7.5	Lead-free TQFP	176	128	C
	LC4256ZC-45MN132C	256	1.8	4.5	Lead-free csBGA	132	96	C
	LC4256ZC-75MN132C	256	1.8	7.5	Lead-free csBGA	132	96	C
	LC4256ZC-45TN100C	256	1.8	4.5	Lead-free TQFP	100	64	C
	LC4256ZC-75TN100C	256	1.8	7.5	Lead-free TQFP	100	64	C

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5MN56I	32	1.8	5	Lead-free csBGA	56	32	I
	LC4032ZC-75MN56I	32	1.8	7.5	Lead-free csBGA	56	32	I
	LC4032ZC-5TN48I	32	1.8	5	Lead-free TQFP	48	32	I
	LC4032ZC-75TN48I	32	1.8	7.5	Lead-free TQFP	48	32	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4064ZC	LC4064ZC-5MN132I	64	1.8	5	Lead-free csBGA	132	64	I
	LC4064ZC-75MN132I	64	1.8	7.5	Lead-free csBGA	132	64	I
	LC4064ZC-5TN100I	64	1.8	5	Lead-free TQFP	100	64	I
	LC4064ZC-75TN100I	64	1.8	7.5	Lead-free TQFP	100	64	I
	LC4064ZC-5MN56I	64	1.8	5	Lead-free csBGA	56	32	I
	LC4064ZC-75MN56I	64	1.8	7.5	Lead-free csBGA	56	32	I
	LC4064ZC-5TN48I	64	1.8	5	Lead-free TQFP	48	32	I
	LC4064ZC-75TN48I	64	1.8	7.5	Lead-free TQFP	48	32	I
LC4128ZC	LC4128ZC-75MN132I	128	1.8	7.5	Lead-free csBGA	132	96	I
	LC4128ZC-75TN100I	128	1.8	7.5	Lead-free TQFP	100	64	I
LC4256ZC	LC4256ZC-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256ZC-75MN132I	256	1.8	7.5	Lead-free csBGA	132	96	I
	LC4256ZC-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I

ispMACH 4000Z (Zero Power, 1.8V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LC4064ZC	LC4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LC4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LC4128ZC	LC4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E
LC4256ZC	LC4256ZC-75TN176E	256	1.8	7.5	Lead-free TQFP	176	128	E
	LC4256ZC-75TN100E	256	1.8	7.5	Lead-free TQFP	100	64	E

ispMACH 4000C (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-25TN48C	32	1.8	2.5	Lead-free TQFP	48	32	C
	LC4032C-5TN48C	32	1.8	5	Lead-free TQFP	48	32	C
	LC4032C-75TN48C	32	1.8	7.5	Lead-free TQFP	48	32	C
	LC4032C-25TN44C	32	1.8	2.5	Lead-free TQFP	44	30	C
	LC4032C-5TN44C	32	1.8	5	Lead-free TQFP	44	30	C
	LC4032C-75TN44C	32	1.8	7.5	Lead-free TQFP	44	30	C

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI ¹	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI ¹	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI ¹	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI ¹	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI ¹	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI ¹	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I ¹	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I ¹	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I ¹	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I ¹	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I ¹	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I ¹	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FTN256AI	256	3.3	5	Lead-free ftBGA	256	128	I
	LC4256V-75FTN256AI	256	3.3	7.5	Lead-free ftBGA	256	128	I
	LC4256V-10FTN256AI	256	3.3	10	Lead-free ftBGA	256	128	I
	LC4256V-5FTN256BI	256	3.3	5	Lead-free ftBGA	256	160	I
	LC4256V-75FTN256BI	256	3.3	7.5	Lead-free ftBGA	256	160	I
	LC4256V-10FTN256BI	256	3.3	10	Lead-free ftBGA	256	160	I
	LC4256V-5FN256AI ¹	256	3.3	5	Lead-free fpBGA	256	128	I
	LC4256V-75FN256AI ¹	256	3.3	7.5	Lead-free fpBGA	256	128	I
	LC4256V-10FN256AI ¹	256	3.3	10	Lead-free fpBGA	256	128	I
	LC4256V-5FN256BI ¹	256	3.3	5	Lead-free fpBGA	256	160	I
	LC4256V-75FN256BI ¹	256	3.3	7.5	Lead-free fpBGA	256	160	I
	LC4256V-10FN256BI ¹	256	3.3	10	Lead-free fpBGA	256	160	I
	LC4256V-5TN176I	256	3.3	5	Lead-free TQFP	176	128	I
	LC4256V-75TN176I	256	3.3	7.5	Lead-free TQFP	176	128	I
	LC4256V-10TN176I	256	3.3	10	Lead-free TQFP	176	128	I
	LC4256V-5TN144I	256	3.3	5	Lead-free TQFP	144	96	I
	LC4256V-75TN144I	256	3.3	7.5	Lead-free TQFP	144	96	I
	LC4256V-10TN144I	256	3.3	10	Lead-free TQFP	144	96	I
	LC4256V-5TN100I	256	3.3	5	Lead-free TQFP	100	64	I
	LC4256V-75TN100I	256	3.3	7.5	Lead-free TQFP	100	64	I
	LC4256V-10TN100I	256	3.3	10	Lead-free TQFP	100	64	I
LC4384V	LC4384V-5FTN256I	384	3.3	5	Lead-free ftBGA	256	192	I
	LC4384V-75FTN256I	384	3.3	7.5	Lead-free ftBGA	256	192	I
	LC4384V-10FTN256I	384	3.3	10	Lead-free ftBGA	256	192	I
	LC4384V-5FN256I ¹	384	3.3	5	Lead-free fpBGA	256	192	I
	LC4384V-75FN256I ¹	384	3.3	7.5	Lead-free fpBGA	256	192	I
	LC4384V-10FN256I ¹	384	3.3	10	Lead-free fpBGA	256	192	I
	LC4384V-5TN176I	384	3.3	5	Lead-free TQFP	176	128	I
	LC4384V-75TN176I	384	3.3	7.5	Lead-free TQFP	176	128	I
LC4512V	LC4512V-5FTN256I	512	3.3	5	Lead-free ftBGA	256	208	I
	LC4512V-75FTN256I	512	3.3	7.5	Lead-free ftBGA	256	208	I
	LC4512V-10FTN256I	512	3.3	10	Lead-free ftBGA	256	208	I
	LC4512V-5FN256I ¹	512	3.3	5	Lead-free fpBGA	256	208	I
	LC4512V-75FN256I ¹	512	3.3	7.5	Lead-free fpBGA	256	208	I
	LC4512V-10FN256I ¹	512	3.3	10	Lead-free fpBGA	256	208	I
	LC4512V-5TN176I	512	3.3	5	Lead-free TQFP	176	128	I
	LC4512V-75TN176I	512	3.3	7.5	Lead-free TQFP	176	128	I
	LC4512V-10TN176I	512	3.3	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.