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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

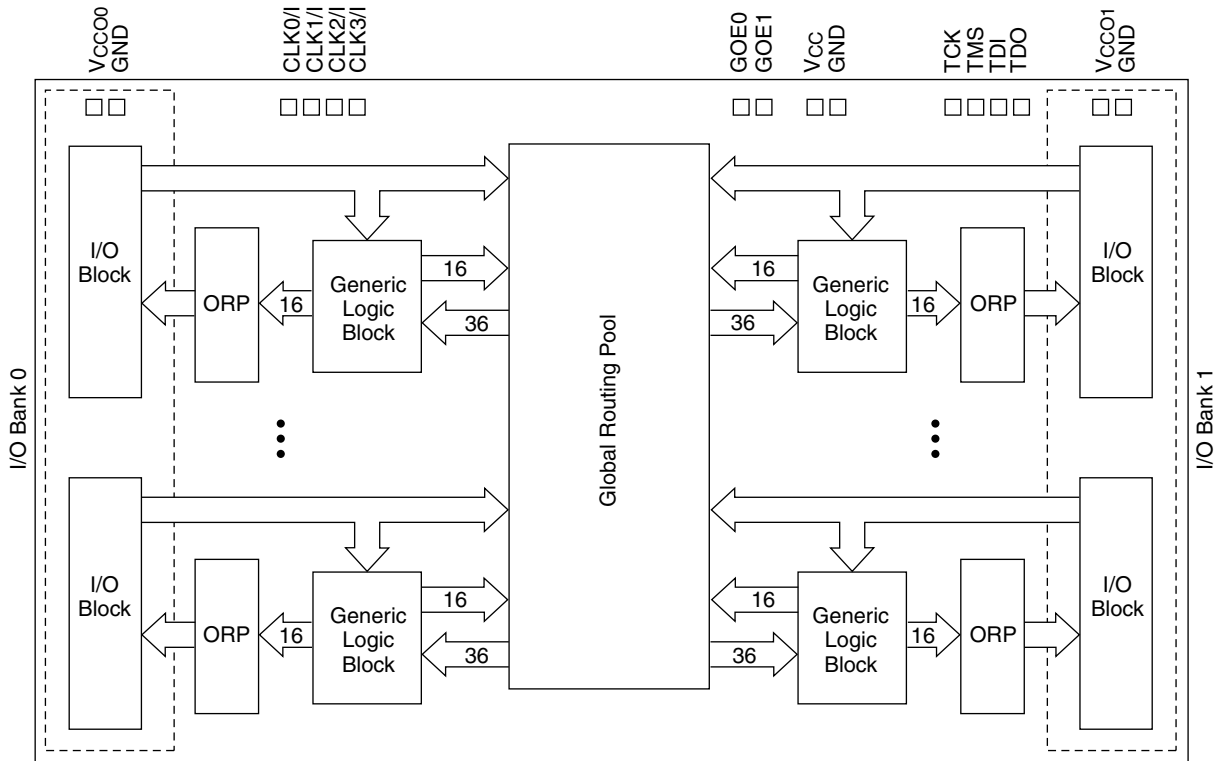
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 130°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064v-75tn100e

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CC0} of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

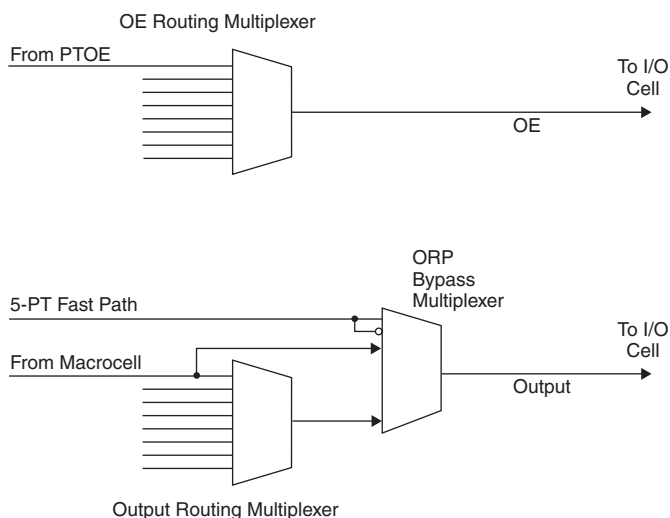
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

- LVTTTL
- LVC MOS 3.3
- LVC MOS 2.5
- LVC MOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 device that has a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except ispMACH 4032



Supply Current, ispMACH 4000V/B/C

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032V/B/C						
ICC ^{1,2,3}	Operating Power Supply Current	V _{CC} = 3.3V	—	11.8	—	mA
		V _{CC} = 2.5V	—	11.8	—	mA
		V _{CC} = 1.8V	—	1.8	—	mA
ICC ⁴	Standby Power Supply Current	V _{CC} = 3.3V	—	11.3	—	mA
		V _{CC} = 2.5V	—	11.3	—	mA
		V _{CC} = 1.8V	—	1.3	—	mA
ispMACH 4064V/B/C						
ICC ^{1,2,3}	Operating Power Supply Current	V _{CC} = 3.3V	—	12	—	mA
		V _{CC} = 2.5V	—	12	—	mA
		V _{CC} = 1.8V	—	2	—	mA
ICC ⁵	Standby Power Supply Current	V _{CC} = 3.3V	—	11.5	—	mA
		V _{CC} = 2.5V	—	11.5	—	mA
		V _{CC} = 1.8V	—	1.5	—	mA
ispMACH 4128V/B/C						
ICC ^{1,2,3}	Operating Power Supply Current	V _{CC} = 3.3V	—	12	—	mA
		V _{CC} = 2.5V	—	12	—	mA
		V _{CC} = 1.8V	—	2	—	mA
ICC ⁴	Standby Power Supply Current	V _{CC} = 3.3V	—	11.5	—	mA
		V _{CC} = 2.5V	—	11.5	—	mA
		V _{CC} = 1.8V	—	1.5	—	mA
ispMACH 4256V/B/C						
I _{CC} ^{1,2,3}	Operating Power Supply Current	V _{CC} = 3.3V	—	12.5	—	mA
		V _{CC} = 2.5V	—	12.5	—	mA
		V _{CC} = 1.8V	—	2.5	—	mA
I _{CC} ⁴	Standby Power Supply Current	V _{CC} = 3.3V	—	12	—	mA
		V _{CC} = 2.5V	—	12	—	mA
		V _{CC} = 1.8V	—	2	—	mA
ispMACH 4384V/B/C						
I _{CC} ^{1,2,3}	Operating Power Supply Current	V _{CC} = 3.3V	—	13.5	—	mA
		V _{CC} = 2.5V	—	13.5	—	mA
		V _{CC} = 1.8V	—	3.5	—	mA
I _{CC} ⁴	Standby Power Supply Current	V _{CC} = 3.3V	—	12.5	—	mA
		V _{CC} = 2.5V	—	12.5	—	mA
		V _{CC} = 1.8V	—	2.5	—	mA
ispMACH 4512V/B/C						
I _{CC} ^{1,2,3}	Operating Power Supply Current	V _{CC} = 3.3V	—	14	—	mA
		V _{CC} = 2.5V	—	14	—	mA
		V _{CC} = 1.8V	—	4	—	mA

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4256ZC						
ICC ^{1,2,3,5}	Operating Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	341	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	361	—	μA
		V _{CC} = 1.9V, T _A = 85°C	—	372	—	μA
		V _{CC} = 1.9V, T _A = 125°C	—	468	—	μA
ICC ^{4,5}	Standby Power Supply Current	V _{CC} = 1.8V, T _A = 25°C	—	13	—	μA
		V _{CC} = 1.9V, T _A = 70°C	—	32	55	μA
		V _{CC} = 1.9V, T _A = 85°C	—	43	90	μA
		V _{CC} = 1.9V, T _A = 125°C	—	135	—	μA

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V _{IL}		V _{IH}		V _{OL} Max (V)	V _{OH} Min (V)	I _{OL} ¹ (mA)	I _{OH} ¹ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTTL	-0.3	0.80	2.0	5.5	0.40	V _{CCO} - 0.40	8.0	-4.0
					0.20	V _{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V _{CCO} - 0.40	8.0	-4.0
					0.20	V _{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V _{CCO} - 0.40	8.0	-4.0
					0.20	V _{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	V _{CCO} - 0.45	2.0	-2.0
					0.20	V _{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	0.35 * V _{CC}	0.65 * V _{CC}	3.6	0.40	V _{CCO} - 0.45	2.0	-2.0
					0.20	V _{CCO} - 0.20	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	0.1 V _{CCO}	0.9 V _{CCO}	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	0.3 * 3.3 * (V _{CC} / 1.8)	0.5 * 3.3 * (V _{CC} / 1.8)	5.5	0.1 V _{CCO}	0.9 V _{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n \cdot 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5	-2.7	-3	-3.5	Units
In/Out Delays						
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	ns
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	ns
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	ns
t_{EN}	Output Enable Time	—	0.96	—	0.96	ns
t_{DIS}	Output Disable Time	—	0.96	—	0.96	ns
Routing/GLB Delays						
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	ns
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	ns
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	ns
Register/Latch Delays						
t_S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	ns
t_H	D-Register Hold Time	0.88	—	0.68	—	ns
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	ns

ispMACH 4000Z Timing Adders ¹

Adder Type	Base Parameter	Description	-35		-37		-42		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Delay Adders									
t _{INDIO}	t _{INREG}	Input register delay	—	1.00	—	1.00	—	1.30	ns
t _{EXP}	t _{MCELL}	Product term expander delay	—	0.40	—	0.40	—	0.45	ns
t _{ORP}	—	Output routing pool delay	—	0.40	—	0.40	—	0.40	ns
t _{BLA}	t _{ROUTE}	Additional block loading adder	—	0.04	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters									
LVTTTL_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVTTTL standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS33_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 3.3 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS25_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 2.5 standard	—	0.60	—	0.60	—	0.60	ns
LVC MOS18_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using LVC MOS 1.8 standard	—	0.00	—	0.00	—	0.00	ns
PCI_in	t _{IN} , t _{GCLK_IN} , t _{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters									
LVTTTL_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS33_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	ns
LVC MOS25_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	ns
LVC MOS18_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	ns
PCI_out	t _{BUF} , t _{EN} , t _{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t _{BUF} , t _{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.2.2

1. Refer to TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#) for information regarding the use of these adders.

**ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections:
44-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A ²	A4	A ²
43	0	A3	A ³	A6	A ³
44	0	A4	A ⁴	A8	A ⁴

**ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections:
48-Pin TQFP**

Pin Number	Bank Number	ispMACH 4032V/B/C/Z		ispMACH 4064V/B/C		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	-	TDI	-	TDI	-	TDI	-
2	0	A5	A ⁵	A10	A ⁵	A8	A ⁵
3	0	A6	A ⁶	A12	A ⁶	A10	A ⁶
4	0	A7	A ⁷	A14	A ⁷	A11	A ⁷
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
7	0	A8	A ⁸	B0	B ⁰	B15	B ⁷
8	0	A9	A ⁹	B2	B ¹	B12	B ⁶
9	0	A10	A ¹⁰	B4	B ²	B10	B ⁵
10	0	A11	A ¹¹	B6	B ³	B8	B ⁴
11	-	TCK	-	TCK	-	TCK	-
12	-	VCC	-	VCC	-	VCC	-
13	-	GND	-	GND	-	GND	-
14	0	A12	A ¹²	B8	B ⁴	B6	B ³
15	0	A13	A ¹³	B10	B ⁵	B4	B ²
16	0	A14	A ¹⁴	B12	B ⁶	B2	B ¹
17	0	A15	A ¹⁵	B14	B ⁷	B0	B ⁰
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
20	1	B0	B ⁰	C0	C ⁰	C0	C ⁰
21	1	B1	B ¹	C2	C ¹	C1	C ¹
22	1	B2	B ²	C4	C ²	C2	C ²
23	1	B3	B ³	C6	C ³	C4	C ³
24	1	B4	B ⁴	C8	C ⁴	C6	C ⁴
25	-	TMS	-	TMS	-	TMS	-
26	1	B5	B ⁵	C10	C ⁵	C8	C ⁵
27	1	B6	B ⁶	C12	C ⁶	C10	C ⁶
28	1	B7	B ⁷	C14	C ⁷	C11	C ⁷
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
31	1	B8	B ⁸	D0	D ⁰	D15	D ⁷
32	1	B9	B ⁹	D2	D ¹	D12	D ⁶

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA (Cont.)

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
K5	0	A15	A ¹⁵	B0	B ⁰
H6	0	CLK1/I	-	CLK1/I	-
K6	1	CLK2/I	-	CLK2/I	-
H7	1	B0	B ⁰	C0	C ⁰
K7	1	B1	B ¹	C1	C ¹
K8	1	B2	B ²	C2	C ²
K9	1	B3	B ³	C4	C ³
K10	1	B4	B ⁴	C6	C ⁴
J10	-	TMS	-	TMS	-
H8	1	B5	B ⁵	C8	C ⁵
H10	1	B6	B ⁶	C10	C ⁶
G10	1	B7	B ⁷	C11	C ⁷
G8	1	GND (Bank 1)	-	GND (Bank 1)	-
F8	1	NC ¹	-	I ¹	-
F10	1	NC ¹	-	I ¹	-
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
E10	1	B8	B ⁸	D15	D ⁷
D8	1	B9	B ⁹	D12	D ⁶
D10	1	B10	B ¹⁰	D10	D ⁵
C10	1	B11	B ¹¹	D8	D ⁴
B10	1	NC ¹	-	I ¹	-
A10	-	TDO	-	TDO	-
A9	-	VCC	-	VCC	-
C8	-	GND	-	GND	-
A8	1	NC ¹	-	I ¹	-
A7	1	B12	B ¹²	D6	D ³
C7	1	B13	B ¹³	D4	D ²
C6	1	B14	B ¹⁴	D2	D ¹
A6	1	B15/GOE1	B ¹⁵	D0/GOE1	D ⁰
C5	1	CLK3/I	-	CLK3/I	-
A5	0	CLK0/I	-	CLK0/I	-
C4	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰
A4	0	A1	A ¹	A1	A ¹
A3	0	A2	A ²	A2	A ²
A2	0	A3	A ³	A4	A ³
A1	0	A4	A ⁴	A6	A ⁴

1. For device migration considerations, these NC pins are input signal pins in ispMACH 4064Z devices.

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C^1	E2	E^1	I6	I^1
43	1	C2	C^2	E4	E^2	I10	I^2
44	1	C3	C^3	E6	E^3	I12	I^3
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
47	1	C4	C^4	E8	E^4	J2	J^0
48	1	C5	C^5	E10	E^5	J6	J^1
49	1	C6	C^6	E12	E^6	J10	J^2
50	1	C7	C^7	E14	E^7	J12	J^3
51	-	GND	-	GND	-	GND	-
52	-	TMS	-	TMS	-	TMS	-
53	1	C8	C^8	F0	F^0	K12	K^3
54	1	C9	C^9	F2	F^1	K10	K^2
55	1	C10	C^10	F4	F^2	K6	K^1
56	1	C11	C^11	F6	F^3	K2	K^0
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
58	1	C12	C^12	F8	F^4	L12	L^3
59	1	C13	C^13	F10	F^5	L10	L^2
60	1	C14	C^14	F12	F^6	L6	L^1
61	1	C15	C^15	F13	F^7	L4	L^0
62*	1	I	-	I	-	I	-
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
64	1	D15	D^15	G14	G^7	M4	M^0
65	1	D14	D^14	G12	G^6	M6	M^1
66	1	D13	D^13	G10	G^5	M10	M^2
67	1	D12	D^12	G8	G^4	M12	M^3
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
69	1	D11	D^11	G6	G^3	N2	N^0
70	1	D10	D^10	G5	G^2	N6	N^1
71	1	D9	D^9	G4	G^1	N10	N^2
72	1	D8	D^8	G2	G^0	N12	N^3
73*	1	I	-	I	-	I	-
74	-	TDO	-	TDO	-	TDO	-
75	-	VCC	-	VCC	-	VCC	-
76	-	GND	-	GND	-	GND	-
77*	1	I	-	I	-	I	-
78	1	D7	D^7	H13	H^7	O12	O^3
79	1	D6	D^6	H12	H^6	O10	O^2
80	1	D5	D^5	H10	H^5	O6	O^1
81	1	D4	D^4	H8	H^4	O2	O^0
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-

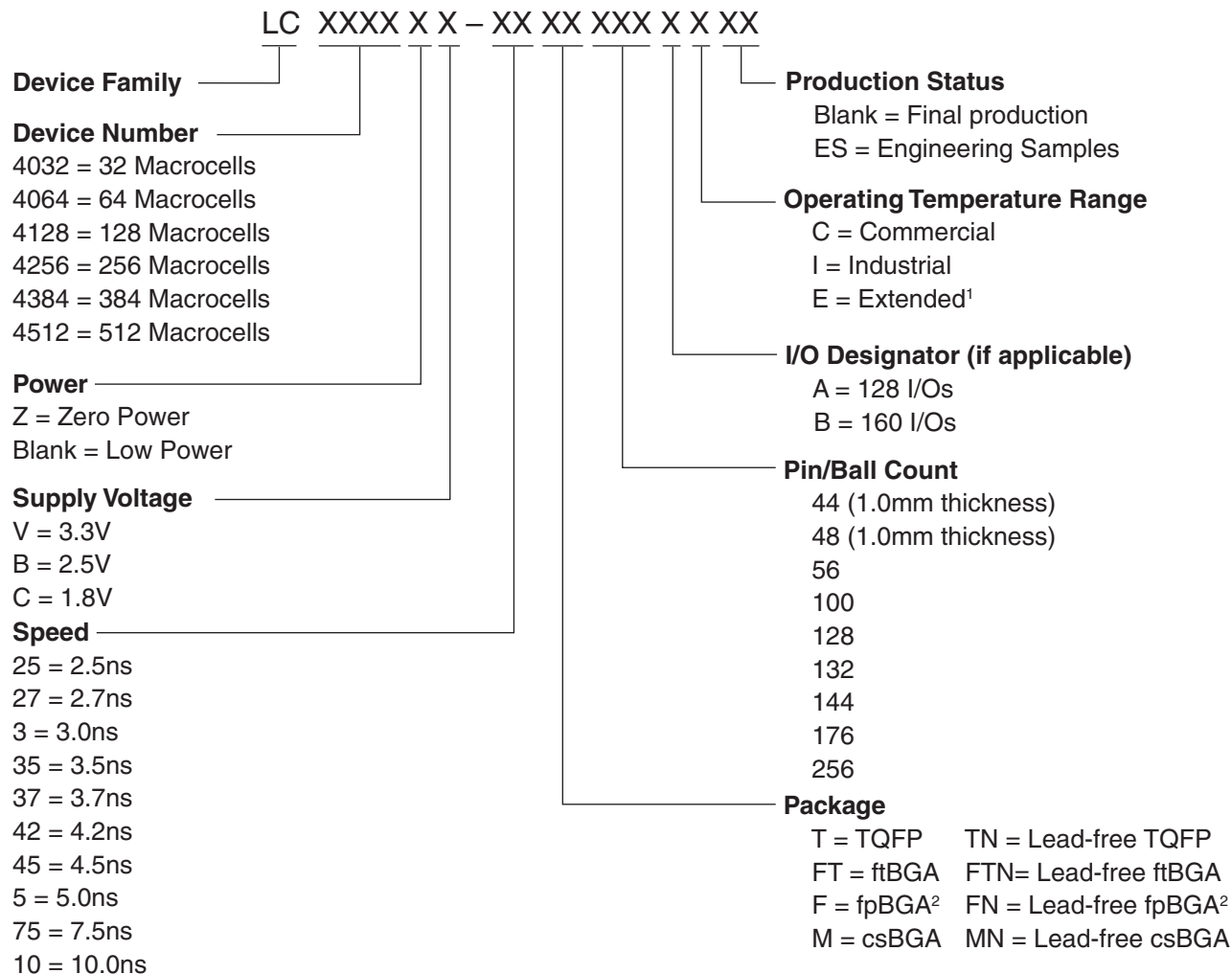
ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
43	0	D9	D [^] 7	G4	G [^] 2
44	0	D8	D [^] 6	G2	G [^] 1
45	0	NC ²	-	I ²	-
46	0	GND (Bank 0)	-	GND (Bank 0)	-
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
48	0	D6	D [^] 5	H12	H [^] 6
49	0	D5	D [^] 4	H10	H [^] 5
50	0	D4	D [^] 3	H8	H [^] 4
51	0	D2	D [^] 2	H6	H [^] 3
52	0	D1	D [^] 1	H4	H [^] 2
53	0	D0	D [^] 0	H2	H [^] 1
54	0	CLK1/I	-	CLK1/I	-
55	1	GND (Bank 1)	-	GND (Bank 1)	-
56	1	CLK2/I	-	CLK2/I	-
57	-	VCC	-	VCC	-
58	1	E0	E [^] 0	I2	I [^] 1
59	1	E1	E [^] 1	I4	I [^] 2
60	1	E2	E [^] 2	I6	I [^] 3
61	1	E4	E [^] 3	I8	I [^] 4
62	1	E5	E [^] 4	I10	I [^] 5
63	1	E6	E [^] 5	I12	I [^] 6
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
65	1	GND (Bank 1)	-	GND (Bank 1)	-
66	1	E8	E [^] 6	J2	J [^] 1
67	1	E9	E [^] 7	J4	J [^] 2
68	1	E10	E [^] 8	J6	J [^] 3
69	1	E12	E [^] 9	J8	J [^] 4
70	1	E13	E [^] 10	J10	J [^] 5
71	1	E14	E [^] 11	J12	J [^] 6
72	1	NC ²	-	I ²	-
73	-	GND	-	GND	-
74	-	TMS	-	TMS	-
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
76	1	F0	F [^] 0	K12	K [^] 6
77	1	F1	F [^] 1	K10	K [^] 5
78	1	F2	F [^] 2	K8	K [^] 4
79	1	F4	F [^] 3	K6	K [^] 3
80	1	F5	F [^] 4	K4	K [^] 2
81	1	F6	F [^] 5	K2	K [^] 1
82	1	GND (Bank 1)	-	GND (Bank 1)	-
83	1	F8	F [^] 6	L14	L [^] 7
84	1	F9	F [^] 7	L12	L [^] 6
85	1	F10	F [^] 8	L10	L [^] 5

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
60	0	H8	H^4	L8	L^4	P8	P^4
61	0	H6	H^3	L6	L^3	P6	P^3
62	0	H4	H^2	L4	L^2	P4	P^2
63	0	H2	H^1	L2	L^1	P2	P^1
64	0	H0	H^0	L0	L^0	P0	P^0
65	-	GND	-	GND	-	GND	-
66	0	CLK1/I	-	CLK1/I	-	CLK1/I	-
67	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
68	1	CLK2/I	-	CLK2/I	-	CLK2/I	-
69	-	VCC	-	VCC	-	VCC	-
70	1	I0	I^0	M0	M^0	AX0	AX^0
71	1	I2	I^1	M2	M^1	AX2	AX^1
72	1	I4	I^2	M4	M^2	AX4	AX^2
73	1	I6	I^3	M6	M^3	AX6	AX^3
74	1	I8	I^4	M8	M^4	AX8	AX^4
75	1	I10	I^5	M10	M^5	AX10	AX^5
76	1	I12	I^6	M12	M^6	AX12	AX^6
77	1	I14	I^7	M14	M^7	AX14	AX^7
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
79	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
80	1	J0	J^0	N0	N^0	BX0	BX^0
81	1	J2	J^1	N2	N^1	BX2	BX^1
82	1	J4	J^2	N4	N^2	BX4	BX^2
83	1	J6	J^3	N6	N^3	BX6	BX^3
84	1	J8	J^4	N8	N^4	BX8	BX^4
85	1	J10	J^5	N10	N^5	BX10	BX^5
86	1	J12	J^6	N12	N^6	BX12	BX^6
87	1	J14	J^7	N14	N^7	BX14	BX^7
88	-	VCC	-	VCC	-	VCC	-
89	-	NC	-	NC	-	NC	-
90	-	GND	-	GND	-	GND	-
91	-	TMS	-	TMS	-	TMS	-
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
93	1	K14	K^7	O14	O^7	CX14	CX^7
94	1	K12	K^6	O12	O^6	CX12	CX^6
95	1	K10	K^5	O10	O^5	CX10	CX^5
96	1	K8	K^4	O8	O^4	CX8	CX^4
97	1	K6	K^3	O6	O^3	CX6	CX^3
98	1	K4	K^2	O4	O^2	CX4	CX^2
99	1	K2	K^1	O2	O^1	CX2	CX^1
100	1	K0	K^0	O0	O^0	CX0	CX^0

Part Number Description



1. For automotive AEC-Q100 compliant devices, refer to the LA-ispMACH 4000V/Z Automotive Family Data Sheet (DS1017).
 2. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000 Family Speed Grade Offering

	-25	-27	-3	-35	-37	-42	-45	-5		-75			-10
	Com	Com	Com	Com	Com	Com	Com	Com	Ind	Com	Ind	Ext	Ind
ispMACH 4032V/B/C												1	
ispMACH 4064V/B/C												1	
ispMACH 4128V/B/C												1	
ispMACH 4256V/B/C													
ispMACH 4384V/B/C													
ispMACH 4512V/B/C													
ispMACH 4032ZC												1	
ispMACH 4064ZC												1	
ispMACH 4128ZC												1	
ispMACH 4256ZC													

1. 3.3V only.

Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispMACH 4000Z devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

Conventional Packaging

ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35M56C	32	1.8	3.5	csBGA	56	32	C
	LC4032ZC-5M56C	32	1.8	5	csBGA	56	32	C
	LC4032ZC-75M56C	32	1.8	7.5	csBGA	56	32	C
	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32	C
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32	C
LC4064ZC	LC4064ZC-37M132C	64	1.8	3.7	csBGA	132	64	C
	LC4064ZC-5M132C	64	1.8	5	csBGA	132	64	C
	LC4064ZC-75M132C	64	1.8	7.5	csBGA	132	64	C
	LC4064ZC-37T100C	64	1.8	3.7	TQFP	100	64	C
	LC4064ZC-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064ZC-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064ZC-37M56C	64	1.8	3.7	csBGA	56	32	C
	LC4064ZC-5M56C	64	1.8	5	csBGA	56	32	C
	LC4064ZC-75M56C	64	1.8	7.5	csBGA	56	32	C
	LC4064ZC-37T48C	64	1.8	3.7	TQFP	48	32	C
	LC4064ZC-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064ZC-75T48C	64	1.8	7.5	TQFP	48	32	C
LC4128ZC	LC4128ZC-42M132C	128	1.8	4.2	csBGA	132	96	C
	LC4128ZC-75M132C	128	1.8	7.5	csBGA	132	96	C
	LC4128ZC-42T100C	128	1.8	4.2	TQFP	100	64	C
	LC4128ZC-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256ZC	LC4256ZC-45T176C	256	1.8	4.5	TQFP	176	128	C
	LC4256ZC-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256ZC-45M132C	256	1.8	4.5	csBGA	132	96	C
	LC4256ZC-75M132C	256	1.8	7.5	csBGA	132	96	C
	LC4256ZC-45T100C	256	1.8	4.5	TQFP	100	64	C
	LC4256ZC-75T100C	256	1.8	7.5	TQFP	100	64	C

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5M56I	32	1.8	5	csBGA	56	32	I
	LC4032ZC-75M56I	32	1.8	7.5	csBGA	56	32	I
	LC4032ZC-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032ZC-75T48I	32	1.8	7.5	TQFP	48	32	I

ispMACH 4000C (1.8V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032C-75T48I	32	1.8	7.5	TQFP	48	32	I
	LC4032C-10T48I	32	1.8	10	TQFP	48	32	I
	LC4032C-5T44I	32	1.8	5	TQFP	44	30	I
	LC4032C-75T44I	32	1.8	7.5	TQFP	44	30	I
	LC4032C-10T44I	32	1.8	10	TQFP	44	30	I
LC4064C	LC4064C-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064C-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064C-10T100I	64	1.8	10	TQFP	100	64	I
	LC4064C-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064C-75T48I	64	1.8	7.5	TQFP	48	32	I
	LC4064C-10T48I	64	1.8	10	TQFP	48	32	I
	LC4064C-5T44I	64	1.8	5	TQFP	44	30	I
	LC4064C-75T44I	64	1.8	7.5	TQFP	44	30	I
LC4128C	LC4128C-5T128I	128	1.8	5	TQFP	128	92	I
	LC4128C-75T128I	128	1.8	7.5	TQFP	128	92	I
	LC4128C-10T128I	128	1.8	10	TQFP	128	92	I
	LC4128C-5T100I	128	1.8	5	TQFP	100	64	I
	LC4128C-75T100I	128	1.8	7.5	TQFP	100	64	I
	LC4128C-10T100I	128	1.8	10	TQFP	100	64	I
LC4256C	LC4256C-5FT256AI	256	1.8	5	ftBGA	256	128	I
	LC4256C-75FT256AI	256	1.8	7.5	ftBGA	256	128	I
	LC4256C-10FT256AI	256	1.8	10	ftBGA	256	128	I
	LC4256C-5FT256BI	256	1.8	5	ftBGA	256	160	I
	LC4256C-75FT256BI	256	1.8	7.5	ftBGA	256	160	I
	LC4256C-10FT256BI	256	1.8	10	ftBGA	256	160	I
	LC4256C-5F256AI ¹	256	1.8	5	fpBGA	256	128	I
	LC4256C-75F256AI ¹	256	1.8	7.5	fpBGA	256	128	I
	LC4256C-10F256AI ¹	256	1.8	10	fpBGA	256	128	I
	LC4256C-5F256BI ¹	256	1.8	5	fpBGA	256	160	I
	LC4256C-75F256BI ¹	256	1.8	7.5	fpBGA	256	160	I
	LC4256C-10F256BI ¹	256	1.8	10	fpBGA	256	160	I
	LC4256C-5T176I	256	1.8	5	TQFP	176	128	I
	LC4256C-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256C-10T176I	256	1.8	10	TQFP	176	128	I
	LC4256C-5T100I	256	1.8	5	TQFP	100	64	I
	LC4256C-75T100I	256	1.8	7.5	TQFP	100	64	I
	LC4256C-10T100I	256	1.8	10	TQFP	100	64	I

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32	I
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32	I
	LC4032B-10T48I	32	2.5	10	TQFP	48	32	I
	LC4032B-5T44I	32	2.5	5	TQFP	44	30	I
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30	I
	LC4032B-10T44I	32	2.5	10	TQFP	44	30	I
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64	I
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64	I
	LC4064B-10T100I	64	2.5	10	TQFP	100	64	I
	LC4064B-5T48I	64	2.5	5	TQFP	48	32	I
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32	I
	LC4064B-10T48I	64	2.5	10	TQFP	48	32	I
	LC4064B-5T44I	64	2.5	5	TQFP	44	30	I
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30	I
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92	I
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92	I
	LC4128B-10T128I	128	2.5	10	TQFP	128	92	I
	LC4128B-5T100I	128	2.5	5	TQFP	100	64	I
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64	I
	LC4128B-10T100I	128	2.5	10	TQFP	100	64	I
LC4256B	LC4256B-5FT256AI	256	2.5	5	ftBGA	256	128	I
	LC4256B-75FT256AI	256	2.5	7.5	ftBGA	256	128	I
	LC4256B-10FT256AI	256	2.5	10	ftBGA	256	128	I
	LC4256B-5FT256BI	256	2.5	5	ftBGA	256	160	I
	LC4256B-75FT256BI	256	2.5	7.5	ftBGA	256	160	I
	LC4256B-10FT256BI	256	2.5	10	ftBGA	256	160	I
	LC4256B-5F256AI ¹	256	2.5	5	fpBGA	256	128	I
	LC4256B-75F256AI ¹	256	2.5	7.5	fpBGA	256	128	I
	LC4256B-10F256AI ¹	256	2.5	10	fpBGA	256	128	I
	LC4256B-5F256BI ¹	256	2.5	5	fpBGA	256	160	I
	LC4256B-75F256BI ¹	256	2.5	7.5	fpBGA	256	160	I
	LC4256B-10F256BI ¹	256	2.5	10	fpBGA	256	160	I
	LC4256B-5T176I	256	2.5	5	TQFP	176	128	I
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
	LC4256B-10T176I	256	2.5	10	TQFP	176	128	I
	LC4256B-5T100I	256	2.5	5	TQFP	100	64	I
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
	LC4256B-10T100I	256	2.5	10	TQFP	100	64	I

ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C ¹	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C ¹	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C ¹	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C ¹	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

ispMACH 4000B (2.5V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128B	LC4128B-5TN128I	128	2.5	5	Lead-Free TQFP	128	92	I
	LC4128B-75TN128I	128	2.5	7.5	Lead-Free TQFP	128	92	I
	LC4128B-10TN128I	128	2.5	10	Lead-Free TQFP	128	92	I
	LC4128B-5TN100I	128	2.5	5	Lead-Free TQFP	100	64	I
	LC4128B-75TN100I	128	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4128B-10TN100I	128	2.5	10	Lead-Free TQFP	100	64	I
LC4256B	LC4256B-5FTN256AI	256	2.5	5	Lead-Free ftBGA	256	128	I
	LC4256B-75FTN256AI	256	2.5	7.5	Lead-Free ftBGA	256	128	I
	LC4256B-10FTN256AI	256	2.5	10	Lead-Free ftBGA	256	128	I
	LC4256B-5FTN256BI	256	2.5	5	Lead-Free ftBGA	256	160	I
	LC4256B-75FTN256BI	256	2.5	7.5	Lead-Free ftBGA	256	160	I
	LC4256B-10FTN256BI	256	2.5	10	Lead-Free ftBGA	256	160	I
	LC4256B-5FN256AI ¹	256	2.5	5	Lead-Free fpBGA	256	128	I
	LC4256B-75FN256AI ¹	256	2.5	7.5	Lead-Free fpBGA	256	128	I
	LC4256B-10FN256AI ¹	256	2.5	10	Lead-Free fpBGA	256	128	I
	LC4256B-5FN256BI ¹	256	2.5	5	Lead-Free fpBGA	256	160	I
	LC4256B-75FN256BI ¹	256	2.5	7.5	Lead-Free fpBGA	256	160	I
	LC4256B-10FN256BI ¹	256	2.5	10	Lead-Free fpBGA	256	160	I
	LC4256B-5TN176I	256	2.5	5	Lead-Free TQFP	176	128	I
	LC4256B-75TN176I	256	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4256B-10TN176I	256	2.5	10	Lead-Free TQFP	176	128	I
	LC4256B-5TN100I	256	2.5	5	Lead-Free TQFP	100	64	I
LC4256B-75TN100I	256	2.5	7.5	Lead-Free TQFP	100	64	I	
LC4256B-10TN100I	256	2.5	10	Lead-Free TQFP	100	64	I	
LC4384B	LC4384B-5FTN256I	384	2.5	5	Lead-Free ftBGA	256	192	I
	LC4384B-75FTN256I	384	2.5	7.5	Lead-Free ftBGA	256	192	I
	LC4384B-10FTN256I	384	2.5	10	Lead-Free ftBGA	256	192	I
	LC4384B-5FN256I ¹	384	2.5	5	Lead-Free fpBGA	256	192	I
	LC4384B-75FN256I ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	I
	LC4384B-10FN256I ¹	384	2.5	10	Lead-Free fpBGA	256	192	I
	LC4384B-5TN176I	384	2.5	5	Lead-Free TQFP	176	128	I
	LC4384B-75TN176I	384	2.5	7.5	Lead-Free TQFP	176	128	I
	LC4384B-10TN176I	384	2.5	10	Lead-Free TQFP	176	128	I
LC4512B	LC4512B-5FTN256I	512	2.5	5	Lead-Free ftBGA	256	208	I
	LC4512B-75FTN256I	512	2.5	7.5	Lead-Free ftBGA	256	208	I
	LC4512B-10FTN256I	512	2.5	10	Lead-Free ftBGA	256	208	I
	LC4512B-5FN256I ¹	512	2.5	5	Lead-Free fpBGA	256	208	I
	LC4512B-75FN256I ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	I
	LC4512B-10FN256I ¹	512	2.5	10	Lead-Free fpBGA	256	208	I
	LC4512B-5TN176I	512	2.5	5	Lead-Free TQFP	176	128	I
	LC4512B-75TN176I	512	2.5	7.5	Lead-Free TQFP	176	128	I
LC4512B-10TN176I	512	2.5	10	Lead-Free TQFP	176	128	I	

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000V (3.3V) Lead-Free Extended Temperature Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032V	LC4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LC4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LC4064V	LC4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LC4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LC4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LC4128V	LC4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LC4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LC4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LC4256V	LC4256V-75TN176E	256	3.3	7.5	Lead-free TQFP	176	128	E
	LC4256V-75TN144E	256	3.3	7.5	Lead-free TQFP	144	96	E
	LC4256V-75TN100E	256	3.3	7.5	Lead-free TQFP	100	64	E

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000V/B/C/Z family:

- TN1004, [ispMACH 4000 Timing Model Design and Usage Guidelines](#)
- TN1005, [Power Estimation in ispMACH 4000V/B/C/Z Devices](#)

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2003	17z	Changed device status for LC4064ZC and LC4128ZC to production release and updated/added AC and DC parameters as well as ordering part numbers for LC4064ZC and LC4128ZC devices.
		Improved leakage current specifications for ispMACH 4000Z. For ispMACH 4000V/B/C IIL, IIH condition now includes 0V and 3.6V end points ($0 \leq V_{IN} \leq 3.6V$).
		Added 132-ball chip scale BGA power supply and NC connections.
		Added 132-ball chip scale BGA logic signal connections for LC4064ZC, LC4128ZC and LC4256ZC devices.
		Added lead-free package designators.
October 2003	18z	Hot socketing characteristics footnote 1. has been enhanced; Insensitive to sequence of VCC or VCCO. However, assumes monotonic rise/fall rates for Vcc and Vcco, provided ($V_{IN} - V_{CCO}$) \leq 3.6V.
		Improved LC4064ZC t _S to 2.5ns, t _{ST} to 2.7ns and f _{MAX} (Ext.) to 175MHz, LC4128ZC t _{CO} to 3.5ns and f _{MAX} (Ext.) to 161MHz (version v.2.1).
		Improved associated internal timing numbers and timing adders (version v.2.1).
		Added ispMACH 4000V/B/C/Z ORP Reference Tables.
		Enhanced ORP information in device pinout tables consistent with the ORP Combinations for I/O Blocks tables (table 6, 7, 8 and 9 in page 9-11).
		Corrected GLB/MC/Pad information in the 256-fpBGA pinouts for the LC4256V/B/C 160-I/O version.
		Added the ispMACH 4000 Family Speed Grade Offering table.
		Added the ispMACH 4128ZC Industrial and Automotive Device OPNs
December 2003	19z	Added the ispMACH 4032ZC and 4064ZC Industrial and Automotive Device OPNs