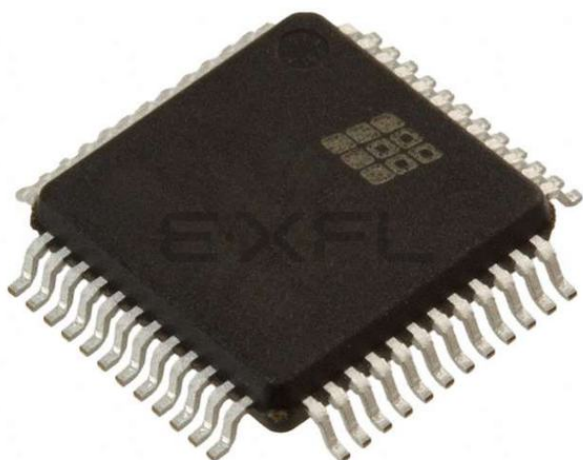




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	3.7 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064zc-37tn48c

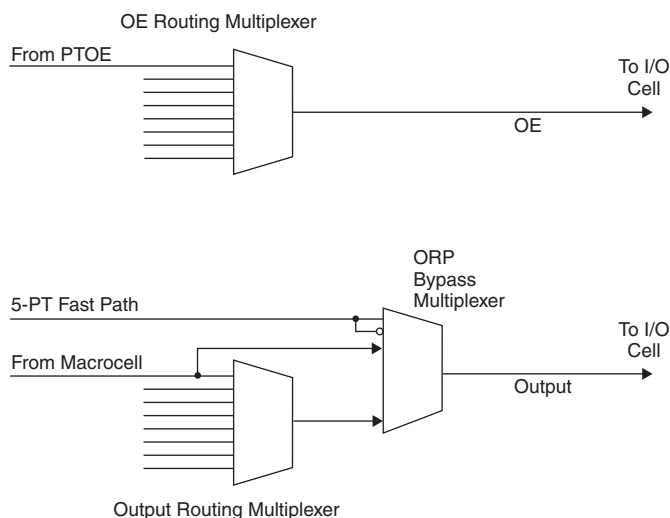
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

I/O Recommended Operating Conditions

Standard	V_{CCO} (V) ¹	
	Min.	Max.
LVTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3 ²	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

2. ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input Leakage Current (ispMACH 4000Z)	$0 \leq V_{IN} < V_{CCO}$	—	0.5	1	μA
I_{IH}^1	Input High Leakage Current (ispMACH 4000Z)	$V_{CCO} < V_{IN} \leq 5.5V$	—	—	10	μA
I_{IL}, I_{IH}^1	Input Leakage Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 3.6V, T_j = 105^\circ C$	—	—	10	μA
		$0 \leq V_{IN} \leq 3.6V, T_j = 130^\circ C$	—	—	15	μA
$I_{IH}^{1,2}$	Input High Leakage Current (ispMACH 4000V/B/C)	$3.6V < V_{IN} \leq 5.5V, T_j = 105^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V^1$	—	—	20	μA
		$3.6V < V_{IN} \leq 5.5V, T_j = 130^\circ C$ $3.0V \leq V_{CCO} \leq 3.6V^1$	—	—	50	μA
I_{PU}	I/O Weak Pull-up Resistor Current (ispMACH 4000Z)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-150	μA
	I/O Weak Pull-up Resistor Current (ispMACH 4000V/B/C)	$0 \leq V_{IN} \leq 0.7V_{CCO}$	-30	—	-200	μA
I_{PD}	I/O Weak Pull-down Resistor Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$	30	—	150	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{BHT}$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \leq V_{IN} \leq V_{CCO}$	—	—	-150	μA
V_{BHT}	Bus Hold Trip Points	—	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
C_1	I/O Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_2	Clock Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_3	Global Input Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \leq V_{CCO} \leq 3.6V$.

3. $T_A = 25^\circ C$, $f = 1.0MHz$

4. I_{IH} excursions of up to 1.5 μA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTTL	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8 (4000C/Z)	-0.3	$0.35 * V_{CC}$	$0.65 * V_{CC}$	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
PCI 3.3 (4000C/Z)	-0.3	$0.3 * 3.3 * (V_{CC} / 1.8)$	$0.5 * 3.3 * (V_{CC} / 1.8)$	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

ispMACH 4000Z External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description ^{1, 2, 3}	-45		-5		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	5-PT bypass combinatorial propagation delay	—	4.5	—	5.0	—	7.5	ns
t _{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.8	—	6.0	—	8.0	ns
t _S	GLB register setup time before clock	2.9	—	3.0	—	4.5	—	ns
t _{ST}	GLB register setup time before clock with T-type register	3.1	—	3.2	—	4.7	—	ns
t _{SIR}	GLB register setup time before clock, input register path	1.3	—	1.3	—	1.4	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	2.6	—	2.6	—	2.7	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	1.3	—	1.3	—	1.3	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	3.8	—	4.2	—	4.5	ns
t _R	External reset pin to output delay	—	7.5	—	7.5	—	9.0	ns
t _{RW}	External reset pulse duration	2.0	—	2.0	—	4.0	—	ns
t _{PTOE/DIS}	Input to output local product term output enable/disable	—	8.2	—	8.5	—	9.0	ns
t _{GPTOE/DIS}	Input to output global product term output enable/disable	—	10.0	—	10.0	—	10.5	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	5.5	—	6.0	—	7.0	ns
t _{CW}	Global clock width, high or low	1.8	—	2.0	—	2.8	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.0	—	2.8	—	ns
t _{WIR}	Input register clock width, high or low	1.8	—	2.0	—	2.8	—	ns
f _{MAX} ⁴	Clock frequency with internal feedback	—	200	—	200	—	168	MHz
f _{MAX} (Ext.)	clock frequency with external feedback, [1 / (t _S + t _{CO})]	—	150	—	139	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

Timing v.2.2

2. Measured using standard switching GRP loading of 1 and 1 output switching.

3. Pulse widths and clock widths less than minimum will cause unknown behavior.

4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5		Units
In/Out Delays										
t _{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.70	ns
t _{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.54	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.28	ns
t _{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.85	ns
t _{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
t _{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.96	ns
Routing/GLB Delays										
t _{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.01	ns
t _{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.65	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.31	ns
t _{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.94	ns
t _{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.94	ns
Register/Latch Delays										
t _S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—	ns
t _{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t _H	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t _{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.52	ns
t _{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—	ns
t _{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—	ns
t _{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—	ns
t _{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.33	ns

ispMACH 4000Z Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-35		-37		-42		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays								
t _{IN}	Input Buffer Delay	—	0.75	—	0.80	—	0.75	ns
t _{GOE}	Global OE Pin Delay	—	2.25	—	2.25	—	2.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	—	1.95	ns
t _{BUF}	Delay through Output Buffer	—	0.75	—	0.90	—	0.90	ns
t _{EN}	Output Enable Time	—	2.25	—	2.25	—	2.50	ns
t _{DIS}	Output Disable Time	—	1.35	—	1.35	—	2.50	ns
Routing/GLB Delays								
t _{ROUTE}	Delay through GRP	—	1.60	—	1.60	—	2.15	ns
t _{MCELL}	Macrocell Delay	—	0.65	—	0.75	—	0.85	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	1.00	—	1.00	ns
t _{FBK}	Internal Feedback Delay	—	0.05	—	0.00	—	0.00	ns
t _{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.40	—	0.40	ns
t _{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	—	0.65	ns
Register/Latch Delays								
t _S	D-Register Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{S_PT}	D-Register Setup Time (Product Term Clock)	1.35	—	1.95	—	1.90	—	ns
t _{ST}	T-Register Setup Time (Global Clock)	1.00	—	1.15	—	1.10	—	ns
t _{ST_PT}	T-register Setup Time (Product Term Clock)	1.55	—	1.75	—	2.10	—	ns
t _H	D-Register Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{HT}	T-Resister Hold Time	1.40	—	1.55	—	1.80	—	ns
t _{SIR}	D-Input Register Setup Time (Global Clock)	0.94	—	0.90	—	1.50	—	ns
t _{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	ns
t _{HIR}	D-Input Register Hold Time (Global Clock)	1.06	—	1.20	—	1.10	—	ns
t _{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	0.65	—	0.70	—	0.65	ns
t _{CES}	Clock Enable Setup Time	1.00	—	2.00	—	2.00	—	ns
t _{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	—	ns
t _{SL}	Latch Setup Time (Global Clock)	0.80	—	0.95	—	0.90	—	ns
t _{SL_PT}	Latch Setup Time (Product Term Clock)	1.55	—	1.95	—	1.90	—	ns
t _{HL}	Latch Hold Time	1.40	—	1.80	—	1.80	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	0.33	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	0.25	ns
t _{SRI}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.28	—	0.28	—	1.27	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	1.80	ns
Control Delays								
t _{BCLK}	GLB PT Clock Delay	—	1.30	—	1.50	—	1.55	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	1.50	—	1.70	—	1.55	ns
t _{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	1.83	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.22	—	2.02	—	1.83	ns

ispMACH 4000V/B/C/Z Power Supply and NC Connections¹

Signal	44-pin TQFP ²	48-pin TQFP ²	56-ball csBGA ³	100-pin TQFP ²	128-pin TQFP ²
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115
VCCO0 VCCO (Bank 0)	6	6	F3	13, 33, 95	3, 17, 30, 41, 122
VCCO1 VCCO (Bank 1)	28	30	E8	45, 63, 83	58, 67, 81, 94, 105
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104
NC	—	—	4032Z: A8, B10, E1, E3, F8, F10, J1, K3	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

**ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C/Z Logic Signal Connections:
100-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 4256V/B/C/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
84	1	D3	D ³	H6	H ³	P12	P ³
85	1	D2	D ²	H4	H ²	P10	P ²
86	1	D1	D ¹	H2	H ¹	P6	P ¹
87	1	D0/GOE1	D ⁰	H0/GOE1	H ⁰	P2/OE1	P ⁰
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	-
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	-
90	-	VCC	-	VCC	-	VCC	-
91	0	A0/GOE0	A ⁰	A0/GOE0	A ⁰	A2/GOE0	A ⁰
92	0	A1	A ¹	A2	A ¹	A6	A ¹
93	0	A2	A ²	A4	A ²	A10	A ²
94	0	A3	A ³	A6	A ³	A12	A ³
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-
97	0	A4	A ⁴	A8	A ⁴	B2	B ⁰
98	0	A5	A ⁵	A10	A ⁵	B6	B ¹
99	0	A6	A ⁶	A12	A ⁶	B10	B ²
100	0	A7	A ⁷	A14	A ⁷	B12	B ³

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B ⁰
5	0	B1	B ¹
6	0	B2	B ²
7	0	B4	B ³
8	0	B5	B ⁴
9	0	B6	B ⁵
10	0	GND (Bank 0)	-
11	0	B8	B ⁶
12	0	B9	B ⁷
13	0	B10	B ⁸
14	0	B12	B ⁹
15	0	B13	B ¹⁰
16	0	B14	B ¹¹
17	0	VCCO (Bank 0)	-
18	0	C14	C ¹¹

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
105	1	VCCO (Bank 1)	-
106	1	H6	H ⁵
107	1	H5	H ⁴
108	1	H4	H ³
109	1	H2	H ²
110	1	H1	H ¹
111	1	H0/GOE1	H ⁰
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A ⁰
117	0	A1	A ¹
118	0	A2	A ²
119	0	A4	A ³
120	0	A5	A ⁴
121	0	A6	A ⁵
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A ⁶
125	0	A9	A ⁷
126	0	A10	A ⁸
127	0	A12	A ⁹
128	0	A14	A ¹¹

**ispMACH 4064Z, 4128Z and 4256Z Logic Signal Connections:
132-Ball csBGA**

Ball Number	Bank Number	ispMACH 4064Z		ispMACH 4128Z		ispMACH 4256Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
B1	-	GND	-	GND	-	GND	-
B2	-	TDI	-	TDI	-	TDI	-
C1	0	NC	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-
C3	0	NC	-	B0	B ⁰	C12	C ⁶
C2	0	A8	A ⁸	B1	B ¹	C10	C ⁵
D1	0	A9	A ⁹	B2	B ²	C8	C ⁴
D3	0	A10	A ¹⁰	B4	B ³	C6	C ³
D2	0	A11	A ¹¹	B5	B ⁴	C4	C ²
E1	0	NC	-	B6	B ⁵	C2	C ¹
E2	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-

**ispMACH 4256V/B/C/Z, 4384V/B/C, 4512V/B/C, Logic Signal Connections:
176-Pin TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4256V/B/C/Z		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
101	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
102	1	L14	L ¹⁴	AX14	AX ¹⁴	GX14	GX ¹⁴
103	1	L12	L ¹²	AX12	AX ¹²	GX12	GX ¹²
104	1	L10	L ¹⁰	AX10	AX ¹⁰	GX10	GX ¹⁰
105	1	L8	L ⁸	AX8	AX ⁸	GX8	GX ⁸
106	1	L6	L ⁶	AX6	AX ⁶	GX6	GX ⁶
107	1	L4	L ⁴	AX4	AX ⁴	GX4	GX ⁴
108	1	L2	L ²	AX2	AX ²	GX2	GX ²
109	1	L0	L ⁰	AX0	AX ⁰	GX0	GX ⁰
110	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
111	1	M0	M ⁰	DX0	DX ⁰	JX0	JX ⁰
112	1	M2	M ²	DX2	DX ²	JX2	JX ²
113	1	M4	M ⁴	DX4	DX ⁴	JX4	JX ⁴
114	1	M6	M ⁶	DX6	DX ⁶	JX6	JX ⁶
115	1	M8	M ⁸	DX8	DX ⁸	JX8	JX ⁸
116	1	M10	M ¹⁰	DX10	DX ¹⁰	JX10	JX ¹⁰
117	1	M12	M ¹²	DX12	DX ¹²	JX12	JX ¹²
118	1	M14	M ¹⁴	DX14	DX ¹⁴	JX14	JX ¹⁴
119	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
120	1	N0	N ⁰	FX0	FX ⁰	NX0	NX ⁰
121	1	N2	N ²	FX2	FX ²	NX2	NX ²
122	1	N4	N ⁴	FX4	FX ⁴	NX4	NX ⁴
123	1	N6	N ⁶	FX6	FX ⁶	NX6	NX ⁶
124	1	N8	N ⁸	FX8	FX ⁸	NX8	NX ⁸
125	1	N10	N ¹⁰	FX10	FX ¹⁰	NX10	NX ¹⁰
126	1	N12	N ¹²	FX12	FX ¹²	NX12	NX ¹²
127	1	N14	N ¹⁴	FX14	FX ¹⁴	NX14	NX ¹⁴
128	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
129	-	TDO	-	TDO	-	TDO	-
130	-	VCC	-	VCC	-	VCC	-
131	-	NC	-	NC	-	NC	-
132	-	NC	-	NC	-	NC	-
133	-	NC	-	NC	-	NC	-
134	-	GND	-	GND	-	GND	-
135	1	O14	O ¹⁴	GX14	GX ¹⁴	OX14	OX ¹⁴
136	1	O12	O ¹²	GX12	GX ¹²	OX12	OX ¹²
137	1	O10	O ¹⁰	GX10	GX ¹⁰	OX10	OX ¹⁰
138	1	O8	O ⁸	GX8	GX ⁸	OX8	OX ⁸
139	1	O6	O ⁶	GX6	GX ⁶	OX6	OX ⁶
140	1	O4	O ⁴	GX4	GX ⁴	OX4	OX ⁴
141	1	O2	O ²	GX2	GX ²	OX2	OX ²

**ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connections:
256-Ball ftBGA/fpBGA (Cont.)**

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH 4512V/B/C	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
R14	1	J10	J ⁵	J10	J ⁷	N10	N ⁵	BX10	BX ⁵
P13	1	J12	J ⁶	J12	J ⁸	N12	N ⁶	BX12	BX ⁶
N13	1	J14	J ⁷	J14	J ⁹	N14	N ⁷	BX14	BX ⁷
M12	1	NC	-	NC	-	P4	P ²	FX0	FX ⁰
T15	1	NC	-	NC	-	P6	P ³	FX2	FX ¹
-	-	VCC	-	VCC	-	VCC	-	VCC	-
-	-	GND	-	GND	-	GND	-	GND	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
P14	-	TMS	-	TMS	-	TMS	-	TMS	-
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
L12	1	NC	-	NC	-	NC	-	FX4	FX ²
R16	1	NC	-	NC	-	P8	P ⁴	FX6	FX ³
N14	1	NC	-	NC	-	P10	P ⁵	FX8	FX ⁴
P15	1	K14	K ⁷	K14	K ⁹	O14	O ⁷	CX14	CX ⁷
L11	1	K12	K ⁶	K12	K ⁸	O12	O ⁶	CX12	CX ⁶
P16	1	K10	K ⁵	K10	K ⁷	O10	O ⁵	CX10	CX ⁵
K11	1	K8	K ⁴	K9	K ⁶	O8	O ⁴	CX8	CX ⁴
M14	1	K6	K ³	K8	K ⁵	O6	O ³	CX6	CX ³
K12	1	K4	K ²	K6	K ⁴	O4	O ²	CX4	CX ²
N15	1	K2	K ¹	K4	K ³	O2	O ¹	CX2	CX ¹
N16	1	K0	K ⁰	K2	K ²	O0	O ⁰	CX0	CX ⁰
M15	1	NC	-	K1	K ¹	BX6	BX ³	HX0	HX ⁰
M13	1	NC	-	K0	K ⁰	BX4	BX ²	HX4	HX ¹
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
M16	1	NC	-	NC	-	NC	-	FX10	FX ⁵
L15	1	NC	-	NC	-	P12	P ⁶	FX12	FX ⁶
L16	1	NC	-	NC	-	P14	P ⁷	FX14	FX ⁷
J11	1	NC	-	L14	L ⁹	BX2	BX ¹	HX8	HX ²
K15	1	NC	-	L12	L ⁸	BX0	BX ⁰	HX12	HX ³
J12	1	L14	L ⁷	L10	L ⁷	AX14	AX ⁷	GX14	GX ⁷
K13	1	L12	L ⁶	L9	L ⁶	AX12	AX ⁶	GX12	GX ⁶
K14	1	L10	L ⁵	L8	L ⁵	AX10	AX ⁵	GX10	GX ⁵
K16	1	L8	L ⁴	L6	L ⁴	AX8	AX ⁴	GX8	GX ⁴
J16	1	L6	L ³	L4	L ³	AX6	AX ³	GX6	GX ³
J15	1	L4	L ²	L2	L ²	AX4	AX ²	GX4	GX ²
H16	1	L2	L ¹	L1	L ¹	AX2	AX ¹	GX2	GX ¹
J13	1	L0	L ⁰	L0	L ⁰	AX0	AX ⁰	GX0	GX ⁰
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-
J14	1	M0	M ⁰	M0	M ⁰	DX0	DX ⁰	JX0	JX ⁰

Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispMACH 4000Z devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

Conventional Packaging

ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-35M56C	32	1.8	3.5	csBGA	56	32	C
	LC4032ZC-5M56C	32	1.8	5	csBGA	56	32	C
	LC4032ZC-75M56C	32	1.8	7.5	csBGA	56	32	C
	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32	C
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32	C
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32	C
LC4064ZC	LC4064ZC-37M132C	64	1.8	3.7	csBGA	132	64	C
	LC4064ZC-5M132C	64	1.8	5	csBGA	132	64	C
	LC4064ZC-75M132C	64	1.8	7.5	csBGA	132	64	C
	LC4064ZC-37T100C	64	1.8	3.7	TQFP	100	64	C
	LC4064ZC-5T100C	64	1.8	5	TQFP	100	64	C
	LC4064ZC-75T100C	64	1.8	7.5	TQFP	100	64	C
	LC4064ZC-37M56C	64	1.8	3.7	csBGA	56	32	C
	LC4064ZC-5M56C	64	1.8	5	csBGA	56	32	C
	LC4064ZC-75M56C	64	1.8	7.5	csBGA	56	32	C
	LC4064ZC-37T48C	64	1.8	3.7	TQFP	48	32	C
	LC4064ZC-5T48C	64	1.8	5	TQFP	48	32	C
	LC4064ZC-75T48C	64	1.8	7.5	TQFP	48	32	C
LC4128ZC	LC4128ZC-42M132C	128	1.8	4.2	csBGA	132	96	C
	LC4128ZC-75M132C	128	1.8	7.5	csBGA	132	96	C
	LC4128ZC-42T100C	128	1.8	4.2	TQFP	100	64	C
	LC4128ZC-75T100C	128	1.8	7.5	TQFP	100	64	C
LC4256ZC	LC4256ZC-45T176C	256	1.8	4.5	TQFP	176	128	C
	LC4256ZC-75T176C	256	1.8	7.5	TQFP	176	128	C
	LC4256ZC-45M132C	256	1.8	4.5	csBGA	132	96	C
	LC4256ZC-75M132C	256	1.8	7.5	csBGA	132	96	C
	LC4256ZC-45T100C	256	1.8	4.5	TQFP	100	64	C
	LC4256ZC-75T100C	256	1.8	7.5	TQFP	100	64	C

ispMACH 4000ZC (1.8V, Zero Power) Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZC	LC4032ZC-5M56I	32	1.8	5	csBGA	56	32	I
	LC4032ZC-75M56I	32	1.8	7.5	csBGA	56	32	I
	LC4032ZC-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032ZC-75T48I	32	1.8	7.5	TQFP	48	32	I

ispMACH 4000C (1.8V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032C	LC4032C-5T48I	32	1.8	5	TQFP	48	32	I
	LC4032C-75T48I	32	1.8	7.5	TQFP	48	32	I
	LC4032C-10T48I	32	1.8	10	TQFP	48	32	I
	LC4032C-5T44I	32	1.8	5	TQFP	44	30	I
	LC4032C-75T44I	32	1.8	7.5	TQFP	44	30	I
	LC4032C-10T44I	32	1.8	10	TQFP	44	30	I
LC4064C	LC4064C-5T100I	64	1.8	5	TQFP	100	64	I
	LC4064C-75T100I	64	1.8	7.5	TQFP	100	64	I
	LC4064C-10T100I	64	1.8	10	TQFP	100	64	I
	LC4064C-5T48I	64	1.8	5	TQFP	48	32	I
	LC4064C-75T48I	64	1.8	7.5	TQFP	48	32	I
	LC4064C-10T48I	64	1.8	10	TQFP	48	32	I
	LC4064C-5T44I	64	1.8	5	TQFP	44	30	I
	LC4064C-75T44I	64	1.8	7.5	TQFP	44	30	I
	LC4064C-10T44I	64	1.8	10	TQFP	44	30	I
LC4128C	LC4128C-5T128I	128	1.8	5	TQFP	128	92	I
	LC4128C-75T128I	128	1.8	7.5	TQFP	128	92	I
	LC4128C-10T128I	128	1.8	10	TQFP	128	92	I
	LC4128C-5T100I	128	1.8	5	TQFP	100	64	I
	LC4128C-75T100I	128	1.8	7.5	TQFP	100	64	I
	LC4128C-10T100I	128	1.8	10	TQFP	100	64	I
LC4256C	LC4256C-5FT256AI	256	1.8	5	ftBGA	256	128	I
	LC4256C-75FT256AI	256	1.8	7.5	ftBGA	256	128	I
	LC4256C-10FT256AI	256	1.8	10	ftBGA	256	128	I
	LC4256C-5FT256BI	256	1.8	5	ftBGA	256	160	I
	LC4256C-75FT256BI	256	1.8	7.5	ftBGA	256	160	I
	LC4256C-10FT256BI	256	1.8	10	ftBGA	256	160	I
	LC4256C-5F256AI ¹	256	1.8	5	fpBGA	256	128	I
	LC4256C-75F256AI ¹	256	1.8	7.5	fpBGA	256	128	I
	LC4256C-10F256AI ¹	256	1.8	10	fpBGA	256	128	I
	LC4256C-5F256BI ¹	256	1.8	5	fpBGA	256	160	I
	LC4256C-75F256BI ¹	256	1.8	7.5	fpBGA	256	160	I
	LC4256C-10F256BI ¹	256	1.8	10	fpBGA	256	160	I
	LC4256C-5T176I	256	1.8	5	TQFP	176	128	I
	LC4256C-75T176I	256	1.8	7.5	TQFP	176	128	I
	LC4256C-10T176I	256	1.8	10	TQFP	176	128	I
	LC4256C-5T100I	256	1.8	5	TQFP	100	64	I
	LC4256C-75T100I	256	1.8	7.5	TQFP	100	64	I
	LC4256C-10T100I	256	1.8	10	TQFP	100	64	I

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96	C
	LC4128V-5T144C	128	3.3	5	TQFP	144	96	C
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96	C
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92	C
	LC4128V-5T128C	128	3.3	5	TQFP	128	92	C
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92	C
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64	C
	LC4128V-5T100C	128	3.3	5	TQFP	100	64	C
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64	C
LC4256V	LC4256V-3FT256AC	256	3.3	3	ftBGA	256	128	C
	LC4256V-5FT256AC	256	3.3	5	ftBGA	256	128	C
	LC4256V-75FT256AC	256	3.3	7.5	ftBGA	256	128	C
	LC4256V-3FT256BC	256	3.3	3	ftBGA	256	160	C
	LC4256V-5FT256BC	256	3.3	5	ftBGA	256	160	C
	LC4256V-75FT256BC	256	3.3	7.5	ftBGA	256	160	C
	LC4256V-3F256AC ¹	256	3.3	3	fpBGA	256	128	C
	LC4256V-5F256AC ¹	256	3.3	5	fpBGA	256	128	C
	LC4256V-75F256AC ¹	256	3.3	7.5	fpBGA	256	128	C
	LC4256V-3F256BC ¹	256	3.3	3	fpBGA	256	160	C
	LC4256V-5F256BC ¹	256	3.3	5	fpBGA	256	160	C
	LC4256V-75F256BC ¹	256	3.3	7.5	fpBGA	256	160	C
	LC4256V-3T176C	256	3.3	3	TQFP	176	128	C
	LC4256V-5T176C	256	3.3	5	TQFP	176	128	C
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128	C
	LC4256V-3T144C	256	3.3	3	TQFP	144	96	C
	LC4256V-5T144C	256	3.3	5	TQFP	144	96	C
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96	C
	LC4256V-3T100C	256	3.3	3	TQFP	100	64	C
	LC4256V-5T100C	256	3.3	5	TQFP	100	64	C
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64	C
LC4384V	LC4384V-35FT256C	384	3.3	3.5	ftBGA	256	192	C
	LC4384V-5FT256C	384	3.3	5	ftBGA	256	192	C
	LC4384V-75FT256C	384	3.3	7.5	ftBGA	256	192	C
	LC4384V-35F256C ¹	384	3.3	3.5	fpBGA	256	192	C
	LC4384V-5F256C ¹	384	3.3	5	fpBGA	256	192	C
	LC4384V-75F256C ¹	384	3.3	7.5	fpBGA	256	192	C
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128	C
	LC4384V-5T176C	384	3.3	5	TQFP	176	128	C
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128	C

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-5FT256AI	256	3.3	5	ftBGA	256	128	I
	LC4256V-75FT256AI	256	3.3	7.5	ftBGA	256	128	I
	LC4256V-10FT256AI	256	3.3	10	ftBGA	256	128	I
	LC4256V-5FT256BI	256	3.3	5	ftBGA	256	160	I
	LC4256V-75FT256BI	256	3.3	7.5	ftBGA	256	160	I
	LC4256V-10FT256BI	256	3.3	10	ftBGA	256	160	I
	LC4256V-5F256AI ¹	256	3.3	5	fpBGA	256	128	I
	LC4256V-75F256AI ¹	256	3.3	7.5	fpBGA	256	128	I
	LC4256V-10F256AI ¹	256	3.3	10	fpBGA	256	128	I
	LC4256V-5F256BI ¹	256	3.3	5	fpBGA	256	160	I
	LC4256V-75F256BI ¹	256	3.3	7.5	fpBGA	256	160	I
	LC4256V-10F256BI ¹	256	3.3	10	fpBGA	256	160	I
	LC4256V-5T176I	256	3.3	5	TQFP	176	128	I
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128	I
	LC4256V-10T176I	256	3.3	10	TQFP	176	128	I
	LC4256V-5T144I	256	3.3	5	TQFP	144	96	I
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96	I
	LC4256V-10T144I	256	3.3	10	TQFP	144	96	I
	LC4256V-5T100I	256	3.3	5	TQFP	100	64	I
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64	I
	LC4256V-10T100I	256	3.3	10	TQFP	100	64	I
LC4384V	LC4384V-5FT256I	384	3.3	5	ftBGA	256	192	I
	LC4384V-75FT256I	384	3.3	7.5	ftBGA	256	192	I
	LC4384V-10FT256I	384	3.3	10	ftBGA	256	192	I
	LC4384V-5F256I ¹	384	3.3	5	fpBGA	256	192	I
	LC4384V-75F256I ¹	384	3.3	7.5	fpBGA	256	192	I
	LC4384V-10F256I ¹	384	3.3	10	fpBGA	256	192	I
	LC4384V-5T176I	384	3.3	5	TQFP	176	128	I
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128	I
	LC4384V-10T176I	384	3.3	10	TQFP	176	128	I
LC4512V	LC4512V-5FT256I	512	3.3	5	ftBGA	256	208	I
	LC4512V-75FT256I	512	3.3	7.5	ftBGA	256	208	I
	LC4512V-10FT256I	512	3.3	10	ftBGA	256	208	I
	LC4512V-5F256I ¹	512	3.3	5	fpBGA	256	208	I
	LC4512V-75F256I ¹	512	3.3	7.5	fpBGA	256	208	I
	LC4512V-10F256I ¹	512	3.3	10	fpBGA	256	208	I
	LC4512V-5T176I	512	3.3	5	TQFP	176	128	I
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128	I
	LC4512V-10T176I	512	3.3	10	TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000C (1.8V) Lead-Free Industrial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256C	LC4256C-5FTN256AI	256	1.8	5	Lead-free ftBGA	256	128	I
	LC4256C-75FTN256AI	256	1.8	7.5	Lead-free ftBGA	256	128	I
	LC4256C-10FTN256AI	256	1.8	10	Lead-free ftBGA	256	128	I
	LC4256C-5FTN256BI	256	1.8	5	Lead-free ftBGA	256	160	I
	LC4256C-75FTN256BI	256	1.8	7.5	Lead-free ftBGA	256	160	I
	LC4256C-10FTN256BI	256	1.8	10	Lead-free ftBGA	256	160	I
	LC4256C-5FN256AI ¹	256	1.8	5	Lead-free fpBGA	256	128	I
	LC4256C-75FN256AI ¹	256	1.8	7.5	Lead-free fpBGA	256	128	I
	LC4256C-10FN256AI ¹	256	1.8	10	Lead-free fpBGA	256	128	I
	LC4256C-5FN256BI ¹	256	1.8	5	Lead-free fpBGA	256	160	I
	LC4256C-75FN256BI ¹	256	1.8	7.5	Lead-free fpBGA	256	160	I
	LC4256C-10FN256BI ¹	256	1.8	10	Lead-free fpBGA	256	160	I
	LC4256C-5TN176I	256	1.8	5	Lead-free TQFP	176	128	I
	LC4256C-75TN176I	256	1.8	7.5	Lead-free TQFP	176	128	I
	LC4256C-10TN176I	256	1.8	10	Lead-free TQFP	176	128	I
	LC4256C-5TN100I	256	1.8	5	Lead-free TQFP	100	64	I
	LC4256C-75TN100I	256	1.8	7.5	Lead-free TQFP	100	64	I
	LC4256C-10TN100I	256	1.8	10	Lead-free TQFP	100	64	I
LC4384C	LC4384C-5FTN256I	384	1.8	5	Lead-free ftBGA	256	192	I
	LC4384C-75FTN256I	384	1.8	7.5	Lead-free ftBGA	256	192	I
	LC4384C-10FTN256I	384	1.8	10	Lead-free ftBGA	256	192	I
	LC4384C-5FN256I ¹	384	1.8	5	Lead-free fpBGA	256	192	I
	LC4384C-75FN256I ¹	384	1.8	7.5	Lead-free fpBGA	256	192	I
	LC4384C-10FN256I ¹	384	1.8	10	Lead-free fpBGA	256	192	I
	LC4384C-5TN176I	384	1.8	5	Lead-free TQFP	176	128	I
	LC4384C-75TN176I	384	1.8	7.5	Lead-free TQFP	176	128	I
	LC4384C-10TN176I	384	1.8	10	Lead-free TQFP	176	128	I
LC4512C	LC4512C-5FTN256I	512	1.8	5	Lead-free ftBGA	256	208	I
	LC4512C-75FTN256I	512	1.8	7.5	Lead-free ftBGA	256	208	I
	LC4512C-10FTN256I	512	1.8	10	Lead-free ftBGA	256	208	I
	LC4512C-5FN256I ¹	512	1.8	5	Lead-free fpBGA	256	208	I
	LC4512C-75FN256I ¹	512	1.8	7.5	Lead-free fpBGA	256	208	I
	LC4512C-10FN256I ¹	512	1.8	10	Lead-free fpBGA	256	208	I
	LC4512C-5TN176I	512	1.8	5	Lead-free TQFP	176	128	I
	LC4512C-75TN176I	512	1.8	7.5	Lead-free TQFP	176	128	I
	LC4512C-10TN176I	512	1.8	10	Lead-free TQFP	176	128	I

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4384B	LC4384B-35FTN256C	384	2.5	3.5	Lead-Free ftBGA	256	192	C
	LC4384B-5FTN256C	384	2.5	5	Lead-Free ftBGA	256	192	C
	LC4384B-75FTN256C	384	2.5	7.5	Lead-Free ftBGA	256	192	C
	LC4384B-35FN256C ¹	384	2.5	3.5	Lead-Free fpBGA	256	192	C
	LC4384B-5FN256C ¹	384	2.5	5	Lead-Free fpBGA	256	192	C
	LC4384B-75FN256C ¹	384	2.5	7.5	Lead-Free fpBGA	256	192	C
	LC4384B-35TN176C	384	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4384B-5TN176C	384	2.5	5	Lead-Free TQFP	176	128	C
	LC4384B-75TN176C	384	2.5	7.5	Lead-Free TQFP	176	128	C
LC4512B	LC4512B-35FTN256C	512	2.5	3.5	Lead-Free ftBGA	256	208	C
	LC4512B-5FTN256C	512	2.5	5	Lead-Free ftBGA	256	208	C
	LC4512B-75FTN256C	512	2.5	7.5	Lead-Free ftBGA	256	208	C
	LC4512B-35FN256C ¹	512	2.5	3.5	Lead-Free fpBGA	256	208	C
	LC4512B-5FN256C ¹	512	2.5	5	Lead-Free fpBGA	256	208	C
	LC4512B-75FN256C ¹	512	2.5	7.5	Lead-Free fpBGA	256	208	C
	LC4512B-35TN176C	512	2.5	3.5	Lead-Free TQFP	176	128	C
	LC4512B-5TN176C	512	2.5	5	Lead-Free TQFP	176	128	C
	LC4512B-75TN176C	512	2.5	7.5	Lead-Free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

ispMACH 4000B (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032B	LC4032B-5TN48I	32	2.5	5	Lead-Free TQFP	48	32	I
	LC4032B-75TN48I	32	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4032B-10TN48I	32	2.5	10	Lead-Free TQFP	48	32	I
	LC4032B-5TN44I	32	2.5	5	Lead-Free TQFP	44	30	I
	LC4032B-75TN44I	32	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4032B-10TN44I	32	2.5	10	Lead-Free TQFP	44	30	I
LC4064B	LC4064B-5TN100I	64	2.5	5	Lead-Free TQFP	100	64	I
	LC4064B-75TN100I	64	2.5	7.5	Lead-Free TQFP	100	64	I
	LC4064B-10TN100I	64	2.5	10	Lead-Free TQFP	100	64	I
	LC4064B-5TN48I	64	2.5	5	Lead-Free TQFP	48	32	I
	LC4064B-75TN48I	64	2.5	7.5	Lead-Free TQFP	48	32	I
	LC4064B-10TN48I	64	2.5	10	Lead-Free TQFP	48	32	I
	LC4064B-5TN44I	64	2.5	5	Lead-Free TQFP	44	30	I
	LC4064B-75TN44I	64	2.5	7.5	Lead-Free TQFP	44	30	I
	LC4064B-10TN44I	64	2.5	10	Lead-Free TQFP	44	30	I

ispMACH 4000V (3.3V) Lead-Free Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256V	LC4256V-3FTN256AC	256	3.3	3	Lead-free ftBGA	256	128	C
	LC4256V-5FTN256AC	256	3.3	5	Lead-free ftBGA	256	128	C
	LC4256V-75FTN256AC	256	3.3	7.5	Lead-free ftBGA	256	128	C
	LC4256V-3FTN256BC	256	3.3	3	Lead-free ftBGA	256	160	C
	LC4256V-5FTN256BC	256	3.3	5	Lead-free ftBGA	256	160	C
	LC4256V-75FTN256BC	256	3.3	7.5	Lead-free ftBGA	256	160	C
	LC4256V-3FN256AC ¹	256	3.3	3	Lead-free fpBGA	256	128	C
	LC4256V-5FN256AC ¹	256	3.3	5	Lead-free fpBGA	256	128	C
	LC4256V-75FN256AC ¹	256	3.3	7.5	Lead-free fpBGA	256	128	C
	LC4256V-3FN256BC ¹	256	3.3	3	Lead-free fpBGA	256	160	C
	LC4256V-5FN256BC ¹	256	3.3	5	Lead-free fpBGA	256	160	C
	LC4256V-75FN256BC ¹	256	3.3	7.5	Lead-free fpBGA	256	160	C
	LC4256V-3TN176C	256	3.3	3	Lead-free TQFP	176	128	C
	LC4256V-5TN176C	256	3.3	5	Lead-free TQFP	176	128	C
	LC4256V-75TN176C	256	3.3	7.5	Lead-free TQFP	176	128	C
	LC4256V-3TN144C	256	3.3	3	Lead-free TQFP	144	96	C
	LC4256V-5TN144C	256	3.3	5	Lead-free TQFP	144	96	C
	LC4256V-75TN144C	256	3.3	7.5	Lead-free TQFP	144	96	C
	LC4256V-3TN100C	256	3.3	3	Lead-free TQFP	100	64	C
	LC4256V-5TN100C	256	3.3	5	Lead-free TQFP	100	64	C
	LC4256V-75TN100C	256	3.3	7.5	Lead-free TQFP	100	64	C
LC4384V	LC4384V-35FTN256C	384	3.3	3.5	Lead-free ftBGA	256	192	C
	LC4384V-5FTN256C	384	3.3	5	Lead-free ftBGA	256	192	C
	LC4384V-75FTN256C	384	3.3	7.5	Lead-free ftBGA	256	192	C
	LC4384V-35FN256C ¹	384	3.3	3.5	Lead-free fpBGA	256	192	C
	LC4384V-5FN256C ¹	384	3.3	5	Lead-free fpBGA	256	192	C
	LC4384V-75FN256C ¹	384	3.3	7.5	Lead-free fpBGA	256	192	C
	LC4384V-35TN176C	384	3.3	3.5	Lead-free TQFP	176	128	C
	LC4384V-5TN176C	384	3.3	5	Lead-free TQFP	176	128	C
	LC4384V-75TN176C	384	3.3	7.5	Lead-free TQFP	176	128	C
LC4512V	LC4512V-35FTN256C	512	3.3	3.5	Lead-free ftBGA	256	208	C
	LC4512V-5FTN256C	512	3.3	5	Lead-free ftBGA	256	208	C
	LC4512V-75FTN256C	512	3.3	7.5	Lead-free ftBGA	256	208	C
	LC4512V-35FN256C ¹	512	3.3	3.5	Lead-free fpBGA	256	208	C
	LC4512V-5FN256C ¹	512	3.3	5	Lead-free fpBGA	256	208	C
	LC4512V-75FN256C ¹	512	3.3	7.5	Lead-free fpBGA	256	208	C
	LC4512V-35TN176C	512	3.3	3.5	Lead-free TQFP	176	128	C
	LC4512V-5TN176C	512	3.3	5	Lead-free TQFP	176	128	C
	LC4512V-75TN176C	512	3.3	7.5	Lead-free TQFP	176	128	C

1. Use ftBGA package. fpBGA package devices have been discontinued via PCN#14A-07.

Revision History (Cont.)

Date	Version	Change Summary
January 2004	20z	ispMACH 4000Z data sheet status changed from preliminary to final. Documents production release of the ispMACH 4256Z device.
		Added new feature - ispMACH 4000Z supports operation down to 1.6V.
		Added lead-free packaging ordering part numbers for the ispMACH 4000Z/C/V devices.
April 2004	21z	Updated I_{PU} (I/O Weak Pull-up Resistor Current) max. specification for the ispMACH 4000V/B/C; -150 μ A to -200 μ A.
November 2004	22z	Added User Electronic Signature section.
		Added ispMACH 4000B (2.5V) Lead-Free Ordering Part Numbers.
December 2004	22z.1	Updated Further Information section.
February 2006	22z.2	Clarification to ispMACH 4000Z Input Leakage (I_{IH}) specification.
March 2007	22.3	Updated ispMACH 4000 Introduction section.
		Updated Signal Descriptions table.
June 2007	22.4	Updated Features bullets to include reference to “LA” automotive data sheet under the “Broad Device Offering” bullet.
		Added footnote 1 to Part Number Description to reference the “LA” automotive data sheet.
		Changed device temperature references from ‘Automotive’ to “Extended Temperature” for non-AEC-Q100 qualified devices.
November 2007	23.0	Added 256-ftBGA package Ordering Part Number information per PCN#14A-07.
May 2009	23.1	Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000Z External Switching Characteristics table.
		Correction to t_{CW} , t_{GW} , t_{WIR} and f_{MAX} parameters in ispMACH 4000V/B/C External Switching Characteristics table.